

CONTROL SIGNAL GENERATOR FOR A DIMMER CIRCUIT

TECHNICAL FIELD

5 The present invention relates to dimmer circuits for controlling loads such as Compact
FlourescentFluorescent Lamps (CFLs).

PRIORITY CLAIM

The present application claims priority from Australian Provisional Patent Application No
10 2010900685 entitled "Control Signal Generator For A Dimmer Circuit", filed on 18 February 2010.

The entire content of this document is hereby incorporated by reference.

INCORPORATION BY REFERENCE

15 The following documents are referred to in the present application:
PCT/AU03/00365 entitled "Improved Dimmer Circuit Arrangement";
PCT/AU03/00366 entitled "Dimmer Circuit with Improved Inductive Load";
PCT/AU03/00364 entitled "Dimmer Circuit with Improved Ripple Control";
PCT/AU2006/001883 entitled "Current Zero Crossing Detector in A Dimmer Circuit";
20 PCT/AU2006/001882 entitled "Load Detector For A Dimmer";
PCT/AU2006/001881 entitled "A Universal Dimmer";
PCT/AU2008/001398 entitled "Improved Start-Up Detection in a Dimmer Circuit";
PCT/AU2008/001399 entitled "Dimmer Circuit With Overcurrent Detection"; and
PCT/AU2008/001400 entitled "Overcurrent Protection in a Dimmer Circuit".

25 The entire content of each of these documents is hereby incorporated by reference.

BACKGROUND

Phase control dimmer circuits (also referred to as dimming circuits or simply dimmers) are used to
30 control the power provided to a load such as a light or electric motor from a power source such as
mains power. Such circuits often use a technique referred to as phase control dimming. This allows
power provided to the load to be controlled by varying the amount of time that a switch connecting the
load to the power source is conducting during a given cycle.

35 For example, if voltage provided by the power source can be represented by a sine wave, then
maximum power is provided to the load if the switch connecting the load to the power source is on at
all times. In this way the, the total energy of the power source is transferred to the load. If the switch is
turned off for a portion of each cycle (both positive and negative), then a proportional amount of the

sine wave is effectively isolated from the load, thus reducing the average energy provided to the load. For example, if the switch is turned on and off half way through each cycle, then only half of the power will be transferred to the load. The overall effect will be, for example in the case of a light, a smooth dimming action resulting in the control of the luminosity of the light.

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Modern phase control dimming circuits generally operate in one of two ways – leading edge or trailing edge.

10 In leading edge technology, the dimmer circuit “chops out” or blocks conduction of electricity by the load in the front part of each half cycle (hence the term “leading edge”). In trailing edge technology, the dimmer circuit “chops out” or blocks conduction of electricity by the load in the back part of each half cycle.

15 Figure 1A shows a representation of the function of a leading edge dimmer, illustrating the current I_L through the load while Figure 1B shows the function of a trailing edge dimmer.

20 Figure 2A shows a typical prior art phase control dimmer circuit (or dimmer circuit) 1 comprising a switch 4 (e.g. a solid state switch such as a triac), which switches current to the load 10 in accordance with timing signals provided by a timing control circuit 3 as will be understood by the person skilled in the art. The timing control circuit 3 determines the angle at which the switch 4 fires into conduction (the firing angle), to allow current to flow into the load 10. The output 5' (provided as a drive signal) of the timing control circuit 3 is controlled by the input 5 of the timing control circuit 3 which is a control voltage. The value of this control voltage 5 may be varied by a user operating a user-settable interface 2 such as a potentiometer or digital switch.

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The higher the user sets the user-settable interface 2, the higher the control voltage 5 applied to the timing control circuit 3, the higher the drive signal 5', and the higher the conduction angle. A higher conduction angle results in a higher brightness of the light. Figure 2B shows a typical user control signal/control signal/control voltage/drive signal vs conduction angle transfer function.

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One type of load that may be used is a Compact Fluorescent Lamp (CFL). Compact Fluorescent Lamps (CFLs) are being increasingly used as a more energy-efficient lighting source over traditional incandescent lamps. One disadvantage of CFLs is that they are much more difficult to control by phase control lighting dimmers as they can be very unstable at low conduction angles. In particular, 35 starting of these load types can be unreliable or in some cases, not possible, with standard dimmers when the dimmer control setting is set to a low level (or low conduction angle). In order to achieve reliable starting of the CFL load, currently, the user must typically ensure that the dimmer control

setting is set to a level beyond approximately 50% of the maximum conduction period, before it is possible to dim to a lower brightness level after the CFL has warmed up.

DRAWINGS

- 5 The various aspects of the present invention will now be described with reference to the following figures in which:
- Figure 1A – shows a representation of the function of a leading edge phase control dimmer;
- Figure 1B – shows a representation of the function of a trailing edge phase control dimmer;
- 10 Figure 2A – shows a typical prior art phase control dimmer arrangement;
- Figure 2B – shows a typical control voltage vs conduction angle transfer function;
- Figure 3 – shows one example of an arrangement of a phase control dimmer circuit according to one aspect of the present invention;
- Figure 4A – shows the arrangement of Figure 3 with a low user setting;
- 15 Figure 4B – shows the load current I_L for the selected user setting of Figure 4A;
- Figure 4C – shows the load current I_L during the “kick-start” or start up period;
- Figure 5A - shows the arrangement of Figure 3 with a high user setting;
- Figure 5B – shows the load current I_L for the selected user setting of Figure 5A;
- Figure 5C – shows the load current I_L output from the control signal generator;
- 20 Figure 6A – shows a graph of Drive Signal vs time during and after the “kick start” or start up period;
- Figure 6B – shows a modified version of the graph of Figure 6A with a ramp up and ramp down period;
- Figure 6C – shows a ramp up period longer than the ramp down period;
- Figure 6D – shows the ramp up period shorter than the ramp down period;
- 25 Figure 6E shows no ramp up period and a ramp down period;
- Figure 6F shows a ramp up period and no ramp down period;
- Figure 6G – shows a ramp up period and a ramp down period using a soft ramp;
- Figure 7 – shows the load current I_L as it changes in accordance with the drive signal of Figure 6B;
- Figure 8 – shows a different arrangement of the phase control dimmer circuit of Figure 3;
- 30 Figure 9 – shows yet another arrangement of the phase control dimmer circuit of Figure 3;
- Figure 10A – shows a general block diagram of one embodiment of a control signal generator;
- Figure 10B – shows a block diagram of another embodiment of a control signal generator;
- Figure 11 – shows a circuit arrangement of one embodiment of the control signal generator;
- Figure 12 – shows a digital implementation of the phase control dimmer circuit of Figure 3;
- 35 Figure 13 – shows a flow chart of the steps performed by the microcontroller as shown in Figure 12;
- Figure 14 – shows a flowchart of a broad method of generating a control signal according to one embodiment; and

Figure 15 -- shows a block diagram of a broad embodiment of a phase control dimmer circuit according to an embodiment described herein.

SUMMARY

5 In a broad aspect, there is provided a control signal generator for use in a phase control dimmer circuit. The control signal generator generates as an output, either a user input if the user input is greater than or equal to a conduction threshold, or a boost signal if the user input is less than the conduction threshold. The output is used to control the firing angle of the dimmer circuit and may be used to control a load such as a compact fluorescent light (CFL).

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In one aspect, there is provided a control signal generator for use in controlling a conduction angle in a phase control dimmer circuit for controlling power delivered to a load, including a compact fluorescent lamp load, the control signal generator comprising:

15 an input for receiving an input signal representative of a user control signal for setting the conduction angle of the phase control dimmer circuit;

a boost signal generator for generating a boost signal at or above a conduction threshold for a start up period if the user control signal is less than the conduction threshold; and

an output for outputting a control signal comprising the boost signal if the boost signal is generated.

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In one embodiment, the output outputs the input signal as the control signal if no boost signal is generated.

In one embodiment, the input signal is the user control signal.

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In one embodiment, the input signal is a drive signal generated by a timing control circuit of the phase control dimmer circuit.

In one embodiment, the start up period is between about 0.5 seconds and about 5 seconds.

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In one embodiment, the start up period is about 2 seconds.

In another embodiment, the start up period is about 4 seconds.

35 In one embodiment, the start up period begins with a ramp up period.

In one embodiment, the start up period finishes with a ramp down period.

In one embodiment, the conduction threshold is determined by a voltage divider of two resistors.

In one embodiment, the start up period is determined by an RC network.

In one embodiment, the control signal generator is provided by a microcontroller.

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In one embodiment, the output is provided as a control signal for input to a timing control circuit of the phase control dimmer circuit.

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In one embodiment, the output is provided as a ~~control~~-switch drive signal for input to a switch of the phase control dimmer circuit.

In one embodiment, the conduction threshold is between about 50% and about 100% of line voltage half cycle period.

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In one embodiment, the conduction threshold is about 80% of line voltage half cycle period.

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In another aspect, there is provided a method of generating a control signal for use in controlling a conduction angle in a phase control dimmer circuit for controlling power delivered to a load including a compact fluorescent lamp load, the method comprising:

receiving an input representative of a user control signal for setting the conduction angle of the phase control dimmer circuit;

generating a boost signal at or above a conduction threshold for a start up period if the user control signal is less than the conduction threshold; and

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outputting a control signal comprising the boost signal if the boost signal is generated.

In one embodiment, the method further comprises outputting the input signal if no boost signal is generated.

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In another embodiment, the start up period is about 2 seconds.

In another embodiment, the start up period is about 4 seconds.

In another embodiment, the start up period is preceded by a ramp up period.

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In another embodiment, the start up period is followed by a ramp down period.

In another aspect, there is provided a phase control dimmer circuit for controlling power delivered to a load including a compact fluorescent lamp load, comprising:

an input for receiving a user control signal from a user control for setting the conduction angle of the phase control dimmer circuit;

- 5 a control signal generator for providing a control signal as the user control signal if the user control signal is greater than or equal to a conduction threshold, or a boost signal that is greater than or equal to the conduction threshold if the user control signal is less than the conduction threshold;
- a timing control circuit for generating a drive signal in response to the control signal; and
- a switch for switching current to the load in response to the drive signal.

DETAILED DESCRIPTION

10 Figure 3 shows a block diagram of a phase control dimmer circuit (or dimmer circuit) 100 comprising a switch 110 (e.g. a solid state switch such as a triac), which switches current to the load 10 from a source 9 in accordance with timing signals provided as a switch drive signal 8 by a timing control circuit 120 as will be understood by the person skilled in the art. The timing control circuit 120 determines the angle at which the switch 110 fires into conduction (the firing or conduction angle), to
 15 allow current to flow into the load 10. The output of the timing control circuit 120 as switch drive signal 8 is controlled by the input of the timing control circuit 120 provided as a control signal 7. The value of this control signal 7 may be varied by a user operating a user control 130 such as a potentiometer or digital switch, producing a user control signal 6.

20 If the load 10 is a compact fluorescent lamp (CFL), then controlling the brightness of this load is difficult if the user sets the user control 130 too low. This will result in the CFL becoming unstable and may flicker, or may not turn on at all.

In accordance with one embodiment of one aspect of the present invention, there is provided a “kick-start” circuit provided in one embodiment, as a control signal generator 140 that will generate or
 25 provide an appropriate boost signal as a control signal 7 that is sufficiently large to avoid this instability.

In one particular example, if the conduction angle represented by the user control signal 6 is less than
 30 a load operating threshold (in one example, about 50% the maximum conduction period), the control signal generator 140 will generate a boost signal or control signal or voltage 7 sufficient to provide a conduction angle equal to or greater than the load operating threshold.

In order to allow the dimmer circuit 100 to control the load in a stable manner, a conduction threshold
 35 is set at or above the load operating threshold. In one example, the conduction threshold is set at about 50% of the line voltage half cycle period. It will be appreciated that the load operating threshold (i.e. the threshold at and above which the CFL will operate in a stable mode), may be different for each load, and this may be determined by experimentation. In one example a conservative approach is to set

the conduction threshold well above the load operating threshold, such as for example, at 80% of the line voltage half cycle period.

5 In another example, the conduction threshold is between about 50% and about 80% of the maximum conduction period. The conduction threshold may be any suitable value including between about 50% and about 100%, about 50% and 60%, about 55%, between about 50% and about 70%, about 60%, between about 50% and about 90%, about 70%, about 80%, about 90%, between about 80% and about 100%, about 85%, and about 95%.

10 It will be appreciated that in 2-wire dimmer applications the maximum conduction period of the dimmer circuit 100 is less than the line voltage half-cycle period. For example, for a 50Hz system with 10ms half-cycle period a maximum dimmer conduction period of 80% (8ms) is typical. In a 3-wire dimmer application a maximum dimmer conduction period of 100% is possible.

15 In a 2-wire dimmer application, using CFL loads, the actual achievable maximum conduction period of the dimmer circuit 100 is limited by the CFL load characteristics, due to the requirement of the dimmer circuit 100 to receive some line voltage to sustain operation in each half-cycle. For example, a poor-case CFL would result in an allowable maximum conduction period of the dimmer circuit 100 to be approximately 6ms. In this example the dimmer half-cycle conduction period during the kick-start event or start up period would be close to 100% of allowable maximum conduction period of the
20 dimmer circuit (i.e. 6ms).

Since the 2-wire application is not applicable to 3-wire dimmer designs, a minimum half-cycle conduction period during the kick-start event or start up period of 50% would be sufficient.

25 Accordingly, the dimmer half-cycle conduction period during the kick-start event or start up period can be within the range of about 65% to about 100% of the dimmer maximum half-cycle conduction period or alternatively it may be stated that the dimmer half-cycle conduction period during the kick-start event or start up period may be about 60% (6ms) of line voltage half-cycle period, for a poor-case
30 CFL load type.

Figure 4A shows the dimmer circuit 100 of Figure 3 with a user control 130 (also represented as a potentiometer dial 131) set at a low setting (for example about 20% of maximum setting). When the light (load 10) being controlled by dimmer circuit 100 is turned on, dimmer circuit 100 would
35 normally apply this user setting to the load 10. In the case where the load 10 is a CFL, the CFL would become unstable since the user setting is well below the load operating threshold of for example 50% of the maximum conduction period or line voltage half cycle conduction period.

Figure 4B shows what the load current I_L would normally be with the 20% user setting, in a trailing edge mode. As can be seen, only a small portion (about 20%) of the full conduction period from 0deg to 180deg is used to deliver current through the load. Figure 4B shows where the load operating threshold for this load is at about 50%, as well as the conduction threshold selected in this case to be about 80%.

Figure 4C shows the equivalent load current I_L upon application of this aspect of the invention in this example, in which control signal generator 140 generates a boost signal control signal (for example control voltage) 7 at a level so as to cause the timing control circuit 120 to generate a switch drive signal 8 to control the switch 110 for a start up period at the selected conduction threshold of about 80%. Figure 4C shows the load current now being passed at a level of about 80%, well above the 50% load operating threshold.

Thus in this application, since a boost signal is generated, the output of control signal generator 140 is the boost signal.

This higher current allows the CFL (load 10) to turn on and operate in a stable mode until it has warmed up sufficiently to remain stable at lower settings or conduction angles.

Figure 5A shows the arrangement of Figure 4A but with the user control 130 (such as potentiometer dial 131) set at about 90% of the maximum setting. Since this setting is above the selected conduction threshold of 80% in this example, meaning that the user selected level at turn on is high enough to control the load (CFL) 10 in a stable manner, control signal generator 140 outputs as control signal 7, a signal that is the same as the input user control signal 6. This output may be the actual input signal or a new signal that is generated by control signal generator 140 that is the same level as the input user control signal 6.

Figure 5B shows what the load current I_L would be with the 90% user setting, in a trailing edge mode. Figure 5B shows where the load operating threshold for this load is at about 50%, as well as the conduction threshold selected in this case to be about 80%. In this case, the load current I_L generated at the user setting is at 90%, well above the selected conduction threshold of 80%.

Figure 5C shows the load current I_L resulting from the output of control signal generator 140. In this case, since the level is above the minimum level to operate the load in a stable manner (i.e. above the selected 80% conduction threshold), no change is required by the control signal generator 140 and so this waveform is the same as the waveform in Figure 5B.

Figure 6A shows one example of how the higher conduction threshold may be applied by increasing the switch drive signal 8 as the boost signal (in one example, by increasing the control signal 7 generated by the control signal generator 140). As can be seen, as the load 10 is switched on by the user, and it is determined that the user control signal 6 is below the selected conduction threshold, the switch drive signal or boost signal is caused to be high (for example 80% of maximum) so as to provide a load current as shown in Figure 4C. This higher drive signal and consequent load current is applied for only a short time (the start up period) after the load is switched on or powered up. This time is selected to be sufficiently long to allow the CFL to warm up sufficiently so as to operate in a stable fashion at low settings or conduction angles. In one example, this is about 5 seconds as shown in Figure 6A. It will be appreciated however, that this period may be less or greater, including about 0.5 seconds, about 1 second, about 1.5 seconds, about 2 seconds, about 2.5 seconds, about 3 seconds, about 3.5 seconds, about 4 seconds, about 4.5 seconds, about 5 seconds, about 5.5 seconds, about 6 seconds, about 6.5 seconds, about 7 seconds, between about 5 seconds and about 10 seconds, or more.

After this selected period of time (the start up period) of applying the boost signal as the switch drive signal 8, the control signal 7 and subsequent switch drive signal 8 is set to the user control signal 6 to cause the dimmer circuit 100 to control the CFL or load 10 at the user selected level (for example, in this case, about 20%). The load current will then appear as shown in Figure 4B, until it is subsequently adjusted again by the user to adopt a desired lighting level as per the normal operation of the dimmer circuit 100. For example, the user may decide to reduce the user setting to provide a user control signal 6 to about 10% maximum setting, thus reducing the brightness of the CFL load 10. Since the CFL has warmed up, it is able to be reduced to any desired setting in a stable manner. In another scenario, the user may decide to increase the user setting to about 50% to increase the brightness of the CFL.

In another embodiment, a refinement to the above example involves providing a ramping effect to achieve the boost signal as a switch drive signal 8, as shown in Figure 6B. Instead of effectively “instantaneously” reaching the selected conduction threshold of for example 80% at turn-on, the boost signal as the drive signal 8 is ramped up from about 0% to about 80% over a ramp up period of for example about 0.5 seconds. It will be appreciated that this ramp up period may be any reasonable period, including anywhere between about 0 seconds and about 1 second, including about 0.1 seconds, about 0.2 seconds, about 0.3 seconds, about 0.4 seconds, about 0.5 seconds, about 0.6 seconds, about 0.7 seconds, about 0.8 seconds, about 0.9 seconds and about 1 second.

Once attained, the boost signal or conduction threshold level may be applied for the selected period as described above in relation to Figure 6A (shown in Figure 6B to be about 4 seconds), and then allowed to ramp down again during a ramp down period to the user selected level as determined by the user control signal 6. In the example, the ramp down period is about the same as the ramp up period of about 0.5 seconds, but this need not be the case. In some embodiments, the ramp up period is longer

than the ramp down period (for example Figure 6C), and in other embodiments, the ramp down period is longer than the ramp up period (for example Figure 6D), or indeed in some other embodiments, there is no ramp up period, only a ramp down period (for example Figure 6E), and in yet other embodiments, there is a ramp up period but no ramp down period (for example Figure 6F).

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In further embodiments, the ramping up and/or ramping down may be provided as a “soft ramp”, having a curved start and a curved end to provide a smoother transition. Figure 6F shows the ramp up as a soft ramp and Figure 6G shows both the ramp up and the ramp down as soft ramps.

10 Figure 7 shows the equivalent schematic of I_L as Figures 4B and 4C but with the ramped application of the boost signal or higher drive signal of Figure 6B. As shown, at initial turn-on, the load current I_L begins to ramp up, starting at about 20% of maximum conduction, then to about 30% in subsequent cycles, then to about 40% until it reaches the selected conduction threshold of (in this example) about 80%. This value is maintained for a period (e.g. about 4 seconds), and then starts to ramp down to
15 about 40%, then about 30% in subsequent cycles, then to about 20%, the user selected level, at which it stays for the remaining subsequent cycles until the user adjusts the dimming level at a later time, at which point the dimmer circuit 100 will respond in the traditional manner as will be understood by the person skilled in the art.

20 It will be understood that the cycles shown in Figure 6 are representational only, and a given conduction angle may be maintained for several cycles before ramping up to the next conduction angle. The number of cycles will be determined by the desired length of time that that conduction angle is required, as will be understood by the person skilled in the art. It will also be understood that the conduction angle may ramp up smoothly to the selected conduction threshold, for example, it may
25 be applied at about 50%, 60%, and 70% before reaching the selected conduction threshold, and may ramp down similarly at about 70%, about 60% and about 50%. These cases are not shown on Figure 7 for simplicity.

It will also be appreciated that many other configurations of the circuit of Figure 3 may be used. For
30 example, in Figure 8, there is shown the control signal generator 140 located between timing control circuit 120 and the switch 110. In this case, the user control signal 6 is input directly into the timing control circuit 120 as in traditional arrangements, and the control signal generator 140 receives the drive signal 8 from timing control circuit 120 as the user control signal 6. In this arrangement, control signal generator 140 still receives as its input, user control signal 6, but in the form of drive signal 8. It
35 will be understood that in this configuration, drive signal 8 is equivalent to, proportional to or representative of user control signal 6 and is representative of the user setting set by the user at user control 130. If control signal generator 140 determines that the switch drive signal 8 generated by timing control circuit 120 is too low (i.e. such that the drive signal would generate a conduction angle

below the selected conduction threshold, as a result of a low user selection at turn on), the control signal generator 140 will generate the boost signal to adjust the input drive signal 8 to generate drive signal 8' to cause the switch 110 to switch at the selected conduction threshold (for example about 80% of maximum conduction) for an initial start up period (for example about 5 seconds) as described above with reference to Figures 6A to 6G.

Figure 9 shows yet another possible configuration in which control signal generator 140 is operationally connected to user control 130 (by wire, wirelessly or a combination of both) and operationally connected to switch 110 (by wire, wirelessly or a combination of both) to provide the required increase in drive signal as the boost signal to drive switch 110 at or above the selected conduction threshold for the initial period, should the user selected level be less than the selected conduction threshold. If the user selected level is equal to or greater than the selected conduction threshold in the initial CFL warm up or start up period, the control signal generator 140 takes no amending action.

In a broad embodiment, the control signal generator 140 comprises an input 141 for receiving an input signal representative of a user control signal, a boost signal generator 142 for generating a boost signal at or above a conduction threshold for a start up period if the user control signal is less than the conduction threshold, and an output 142 for outputting the boost signal if the boost signal is generated.

In one embodiment, the output 142 outputs the input signal if no boost signal is generated.

Figure 10A shows a block diagram of one embodiment of the control signal generator 140. Shown is a control signal generator 140 for use in a phase control dimmer circuit having a conduction period. In this embodiment, the control signal generator 140 comprises an input 141 for receiving an input signal representative of a user control signal (6). The control signal generator 140 also comprises a boost signal generator 142 for generating a boost signal 145 which is at or above the conduction threshold for the start up period if the user control signal 6 is less than the conduction threshold. The control signal generator 140 also comprises an output 142 for outputting either the input signal 6 if no boost signal is generated or the boost signal 145 if the boost signal is generated. The output signal will be provided as control signal 7 described above.

In some embodiments as shown in Figure 10B, control signal generator 140 comprises a comparator 143 for comparing the input user control signal with the selected conduction threshold. If the user control signal is less than the selected conduction threshold, then the boost signal generator 142 will generate the boost signal 145. If the boost signal 145 is generated, then this boost signal 145 will be output from control signal generator 140 at output 142 as the control signal 7. If the boost signal 145 is not generated (e.g. because the user control signal is greater than or equal to the selected conduction

threshold), then the control signal generator 140 will output the user control signal 6 at output 142 as the control signal 7. This determination is made at block 144.

In one embodiment, the start up period is between about 0.5 seconds and about 5 seconds. In another embodiment, the start up period is about 2 seconds. In another embodiment, the start up period is about 4 seconds.

In one embodiment, the start up period begins with a ramp up period. In another embodiment, the start up period ends with a ramp down period.

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Figure 11 shows one example of one embodiment of a circuit embodiment for signal control generator 140. In this circuit implementation of the “kick-start” feature, an RC timing network (R5/C1) is used to temporarily activate a transistor (Q1) for application of increased control voltage. A resistive voltage divider (R2 & R3) determines the conduction threshold setting, as a percentage of the supply voltage V_{CC} . A diode (D1) prevents the voltage divider from adversely loading the control voltage potentiometer (in one example) or user control 130 during normal operation. The control potentiometer wiper series resistor (R1) prevents loading effects on kick-start voltage level.

In one embodiment, components and component values to achieve approximately a 2 second “kick-start” or conduction threshold period are selected as:

20 $R1 = 2M2$

$R2 = 15k$

$R3 = 100k$

$R4 = 220k$

25 $R5 = 1M5$

$C1 = 2.2\mu F$

$VR1 = 500k$

$Q1 = BC858$

$D1 = BAV19$

30 $VCC = 12V$

It is well within the skill of the person skilled in the art to select different values to achieve different periods, such as the 4 or 5 second period described above.

35 In the situation where the user control 130, acting as the input signal representative of the user control signal, is set to near minimum level (for example 10% of maximum conduction period) at first start up or turn on, the circuit acts as follows. Immediately following the power-up event (switched active dimmer) capacitor C1 has zero charge voltage hence base bias current to activate transistor Q1 flows

via R5. Voltage divider resistors R2 & R3 determine the resultant voltage applied to the anode of diode D1, hence the actual voltage (or signal) generated by the control signal generator 140 is reduced by an amount equal to D1 forward voltage drop. In this example, it can be seen that the selected conduction threshold is equivalent to about 80% of the maximum conduction period of the line voltage half cycle conduction period of about 10ms. As will be understood by the person skilled in the art, this may be derived from the voltage applied at the anode of D1 as $(R3/(R2 + R3)) * VCC = ((100/115) * VCC = \text{about } 0.87VCC$. If $VCC = 12V$, the voltage applied to R1 is about 10.44V. Assuming a forward voltage drop of about 0.5V for D1, a voltage of about 9.94V is generated as the output of the circuit. This equates to $9.94/12 = 82\%$ or about 80% of maximum control voltage which equates to about 80% maximum conduction period (or about 6.4ms), selected as the conduction threshold.

As previously described, this generated output signal or boost signal acting in this case as control signal 7, in this embodiment, is be applied to the input of the timing control circuit 120 as shown in Figure 3, or, in other embodiments, the output of control signal generator 140 is applied directly as a modified drive signal 8' as shown in the configurations of Figures 8 and 9. Potentiometer series buffer resistor R1 has sufficiently high value so as to not permit potentiometer resistance from adversely loading the R2/R3 voltage divider. The input impedance of the timing control circuit 120 is significantly greater than the value of R1 so as to not adversely load the potentiometer output voltage during normal operation.

In the situation where the control potentiometer or user control 130 acting as the input representative of the user control signal is set to near the maximum level, such as about 90%, the function of the circuit is as follows. In this situation, the potentiometer output voltage is applied via R1 directly to the timing control circuit since it has a magnitude exceeding that of voltage divider R2/R3, and diode D1 is consequently reverse-biased to create a blocking condition, therefore no "kick-start" event occurs, and the value of the user control signal is generated as the output of the signal control generator 140, either as the control signal 7 or drive signal 8, depending upon the configuration of the dimmer circuit. This point in the circuit provides the comparator 143 and block 144 functions of Figure 10B.

Since the user selected user control signal results in a conduction angle greater than the load operating threshold (and in fact greater than the selected conduction threshold), the CFL will be able to turn on in a stable mode. If the user subsequently adjusts the dimming levels after the CFL has warmed up, the dimmer will be able to operate as normal and dim the CFL in a stable manner.

Figure 12 shows yet a further possible arrangement or embodiment of phase control dimmer circuit 100. In this arrangement, a microcontroller 150 provides the functionality of control signal generator 140 as well as that of timing control circuit 120. The input of microcontroller 150 is the user control

signal 6 acting as the input signal representative of the user control and the output is the boost signal provided as drive signal 8, applied to switch 110.

In practice in some embodiments, microcontroller 150 provides other functions of the dimmer circuit 100, or in other embodiments, simply provides some, such as just that of the control signal generator, as will be appreciated by the person skilled in the art.

Figure 13 illustrates the functionality provided by microcontroller 150 to provide the function of control signal generator 140.

At step 201, the output of the user control 130, being the user control signal 6, acting as the input signal representative of the user control signal, is read at turn on. In step 202, a determination of the level of the input is made. If the level is greater than the selected conduction threshold, this level is generated as the output of microcontroller 150, for example, as a control signal to be applied to the timing control circuit 120 (whether a separate component or provided by the microcontroller itself), or as a drive signal applied directly to switch 110.

If, at step 202, the input level is determined to be less than or equal to the selected conduction threshold, then the level is increased as the boost signal to or above the selected conduction threshold at step 203, maintained at that level for a selected period (the start up period) (for example 0.5 seconds, 1 second, 2 seconds, 3 seconds, 4 seconds or 5 seconds) at step 204, and then returned to the user selected level after the start up period at step 205.

In this particular example as shown in Figure 13, the selected conduction threshold is about 70% of maximum, but of course, as described previously, may take on any suitable value at or above the load operating threshold.

Suitable pseudocode for microcontroller 150 to effect the method outlined above with respect to Figure 13 is as follows:

```
#define NEAR_MAX_CONDUCTION_TIME 7000 // 80% conduction
#define MAX_CONDUCTION_TIME 8000 // 100% conduction
#define BOOST_THRESHOLD 7000 // 80% conduction

#define MAX_HOLD_TIME 200 // 200*10ms (2 seconds)

#define START 1 // first check user selection
#define BOOST_WAIT 2 // waiting at maximum setting
#define CURRENT_SETTING 3 // implements user setting
```

```

unsigned short int user_selected_dimming_level= 2000; // user input 2000..8000
unsigned short int current_conduction_time = 2000; // conduction time
5 unsigned char half_cycle_timer = 0;
unsigned char current_mode = START;

// executed once every half-cycle
10 user_selected_dimming_level = get_user_input(); // get user setting and translate to conduction time

if ( current_mode == START)
{
15 if ( user_selected_dimming_level <= BOOST_THRESHOLD)
{
current_conduction_time = NEAR_MAX_CONDUCTION_TIME; // give a boost start
current_mode = BOOST_WAIT;
half_cycle_timer = 0;
20 }
}
else if ( current_mode == BOOST_WAIT)
{
if ( half_cycle_timer >= MAX_HOLD_TIME)
25 current_mode = CURRENT_SETTING;
}
else if ( current_mode == CURRENT_SETTING)
{
current_conduction_time = user_selected_dimming_level;
30 }

half_cycle_timer++; // increment timer

```

35 In the above pseudocode example, the threshold conduction is selected to be about 80%. It will be appreciated that these steps need only be performed at turn on, and not after the load has warmed up. Subsequent user setting changes may be applied directly. There are numerous ways of determining whether the load is being turned on, as will be appreciated by the person skilled in the art.

40 In one embodiment of another aspect, a broad method of generating a control signal for use in a phase control dimmer circuit is provided. In this embodiment, the method comprises receiving an input representative of a user control signal, generating a boost signal at or above a conduction threshold for a start up period if the user control signal is less than the conduction threshold and outputting the boost signal if the boost signal is generated. In another embodiment, the method also comprises outputting the input signal if no boost signal is generated.

45 In another embodiment, a broad method of generating a control signal for use in a phase control dimmer circuit is provided. As shown in Figure 14, in step 301, an input representative of a user control signal is received. In step 302, a boost signal at or above a conduction threshold is generated for a start up period if the user control signal is less than the conduction threshold; and at step 303, the

control signal is output as either the input signal if no boost signal is generated or the boost signal if the boost signal is generated.

5 In one embodiment, the start up period is between about 0.5 seconds and about 5 seconds. In another embodiment, the start up period is about 2 seconds. In another embodiment, the start up period is about 4 seconds.

10 In one embodiment, the start up period begins with a ramp up period. In another embodiment, the start up period ends with a ramp down period.

In another aspect, as shown in Figure 15, there is also broadly provided a phase control dimmer circuit 100 for controlling power delivered to a load. In this embodiment, dimmer circuit 100 comprises an input 101 for receiving a user control signal 6 from a user control (not shown in this view); a control signal generator 140 for providing a control signal 7 as either the user control signal 6 if the user control signal 6 is greater than or equal to a conduction threshold, or a boost signal that is greater than or equal to the conduction threshold if the user control signal 6 is less than the conduction threshold. In this embodiment, dimmer circuit 100 also comprises a timing control circuit 120 for generating a drive signal 8 in response to the control signal 7; and a switch 110 for switching current to the load (not shown in this view) in response to the drive signal 8.

20 The various aspects described above may be applied to, or incorporated within, any suitable phase control dimming circuits, including leading edge, trailing edge and universal dimmers, and including those described in detail in PCT/AU03/00365 entitled “Improved Dimmer Circuit Arrangement”; PCT/AU03/00366 entitled “Dimmer Circuit with Improved Inductive Load”; PCT/AU03/00364 entitled “Dimmer Circuit with Improved Ripple Control”; PCT/AU2006/001883 entitled “Current Zero Crossing Detector in A Dimmer Circuit”; PCT/AU2006/001882 entitled “Load Detector For A Dimmer”; PCT/AU2006/001881 entitled “A Universal Dimmer”; PCT/AU2008/001398 entitled “Improved Start-Up Detection in a Dimmer Circuit”; PCT/AU2008/001399 entitled “Dimmer Circuit With Overcurrent Detection”; and PCT/AU2008/001400 entitled “Overcurrent Protection in a Dimmer Circuit”.

35 Throughout the specification and the claims that follow, unless the context requires otherwise, the words “comprise” and “include” and variations such as “comprising” and “including” will be understood to imply the inclusion of a stated integer or group of integers, but not the exclusion of any other integer or group of integers.

The reference to any prior art in this specification is not, and should not be taken as, an acknowledgement of any form of suggestion that such prior art forms part of the common general knowledge.

CLAIMS

1. A control signal generator for use in controlling a conduction angle in a phase control dimmer circuit for controlling power delivered to a load, including a compact fluorescent lamp load, the control signal generator comprising:
 - an input for receiving an input signal representative of a user control signal for setting the conduction angle of the phase control dimmer circuit;
 - a boost signal generator for generating a boost signal at or above a conduction threshold for a start up period if the user control signal is less than the conduction threshold; and
 - an output for outputting a control signal comprising the boost signal if the boost signal is generated.
2. A control signal generator as claimed in claim 1 wherein the output outputs the input signal as the control signal if no boost signal is generated.
3. A control signal generator as claimed in claim 1 or 2 wherein the input signal is the user control signal.
4. A control signal generator as claimed in claim 1 or 2 wherein the input signal is a drive signal generated by a timing control circuit of the phase control dimmer circuit.
5. A control signal generator as claimed in any one of claims 1 to 4 wherein the start up period is between about 0.5 seconds and about 5 seconds.
6. A control signal generator as claimed in claim 5 wherein the start up period is about 2 seconds.
7. A control signal generator as claimed in claim 5 wherein the start up period is about 4 seconds.
8. A control signal generator as claimed in any one of claims 5 to 7 wherein the start up period begins with a ramp up period.
9. A control signal generator as claimed in any one of claims 5 to 8 wherein the start up period finishes with a ramp down period.
10. A control signal generator as claimed in any one of claims 1 to 9 wherein the conduction threshold is determined by a voltage divider of two resistors.

11. A control signal generator as claimed in any one of claims 1 to 10 wherein the start up period is determined by an RC network.

5 12. A control signal generator as claimed in any one of claims 1 to 9 wherein the control signal generator is provided by a microcontroller.

13. A control signal generator as claimed in claim 1 wherein the output is provided as a control signal for input to a timing control circuit of the phase control dimmer circuit.

10

14. A control signal generator as claimed in claim 1 wherein the output is provided as a ~~control~~ switch drive signal for input to a switch of the phase control dimmer circuit.

15

15. A control signal generator as claimed in any one of claims 1 to 14 wherein the conduction threshold is between about 50% and about 100% of line voltage half cycle period.

16. A control signal generator as claimed in any one of claims 1 to 15 wherein the conduction threshold is about 80% of line voltage half cycle period.

20

17. A method of generating a control signal for use in controlling a conduction angle in a phase control dimmer circuit for controlling power delivered to a load including a compact fluorescent lamp load, the method comprising:

receiving an input representative of a user control signal for setting the conduction angle of the phase control dimmer circuit;

25

generating a boost signal at or above a conduction threshold for a start up period if the user control signal is less than the conduction threshold; and

outputting a control signal comprising the boost signal if the boost signal is generated.

30

18. A method as claimed in claim ~~17~~¹⁸ further comprising outputting the input signal if no boost signal is generated.

19. A method of generating a control signal as claimed in claim 17 wherein the start up period is between about 0.5 seconds and about 5 seconds.

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20. A method of generating a control signal as claimed in claim 17 wherein the start up period is about 2 seconds.

21. A method of generating a control signal as claimed in claim 17 wherein the start up period is about 4 seconds.
22. A method of generating a control signal as claimed in any one of claims 17 to 20 wherein the
5 start up period is preceded by a ramp up period.
23. A method of generating a control signal as claimed in any one of claims 17 to 21 wherein the start up period is followed by a ramp down period.
- 10 24. A phase control dimmer circuit for controlling power delivered to a load including a compact fluorescent lamp load, comprising:
 an input for receiving a user control signal from a user control for setting the conduction angle of the phase control dimmer circuit;
 a control signal generator for providing a control signal as the user control signal if the user
 15 control signal is greater than or equal to a conduction threshold, or a boost signal that is greater than or equal to the conduction threshold if the user control signal is less than the conduction threshold;
 a timing control circuit for generating a drive signal in response to the control signal; and
 a switch for switching current to the load in response to the drive signal.