

PERSONAL COMPUTER WITH ANTICIPATORY MEMORY CONTROL SIGNALLING

ABSTRACT

This invention relates to personal computers, and more particularly to personal computers in which arbitration for control over a data handling bus occurs among a plurality of "master" devices coupled directly to the bus and memory address signals are varied in response to such arbitration. The personal computer system has a high speed local processor data bus, an input/output data bus, a microprocessor coupled directly to the local processor bus, volatile memory coupled to the local processor bus for volatile storage of data, and a bus interface controller coupled directly to the local processor bus and directly to the input/output data bus for providing communications between the buses. The bus interface controller provides for arbitration among devices directly coupled to the input/output data bus for access to the input/output data bus and to the local processor bus, and for arbitration among the input/output data bus and said microprocessor for access to the local processor bus. The bus interface controller is also coupled to the volatile memory for supplying row address select signals to the volatile memory and thereby selecting data storage areas to be accessed, and responds to a change in access granted to the local bus by changing the row address select signal supplied to the volatile memory in preparation for access to potentially different data storage areas of the volatile memory.

This Sheet Has Been Replaced

