Claims:

1. A method of forming an electrical contact in a semiconductor structure, comprising:

performing a pre-clean process on exposed surfaces of a plurality of first semiconductor regions and a plurality of second semiconductor regions formed on a substrate, wherein the exposed surfaces of the plurality of first and second semiconductor regions are each disposed within openings formed in a dielectric layer disposed over the substrate;

performing a first selective epitaxial deposition process to form a first contact layer on the exposed surfaces of the first semiconductor regions and a second contact layer on the exposed surface of the second semiconductor regions;

performing a patterning process to form a patterned stack, wherein the patterned stack comprises a patterned layer that comprises openings formed over the first contact layer disposed within each opening in the dielectric layer and a portion of the patterned layer that is disposed over each second contact layer disposed within each opening in the dielectric layer; and

performing a selective removal process to remove the first contact layer selectively to the plurality of first semiconductor regions, the dielectric layer, and the patterned layer.

2. The method of claim 1, wherein

the first semiconductor regions formed on the substrate comprises silicon,

the second semiconductor regions formed on the substrate comprises silicon germanium, and

the first contact layer and the second contact layer comprise silicon germanium.

3. The method of claim 1, wherein

the patterning stack comprises material selected from organic dielectric layer, silicon anti-reflective coating, and photoresist.

4. The method of claim 1, wherein the selective removal process is performed at:

a temperature of between -20°C and 60°C,

a pressure of between 1 Torr and 50 Torr,

a flow rate of a fluorine-containing precursor of between about 5 sccm and 40 sccm,

a flow rate of argon (Ar) of between 4 sccm and 1500 sccm,

a flow rate of helium (He) of between 100 sccm and 5000 sccm, and

a flow rate of nitrogen (N_2) of between 100 sccm and 5000 sccm.

5. The method of claim 1, further comprising:

subsequent to the selective removal process, performing an ashing process to remove the patterning stack.

6. The method of claim 5, further comprising:

subsequent to the ashing process, performing a second deposition process to form a metal layer on an exposed surface of the first semiconductor regions and an exposed surface of the second contact layer formed on the second semiconductor regions.

7. The method of claim 6, wherein

the metal layer comprises material selected from titanium (Ti) silicide, cobalt (Co) silicide, nickel (Ni) silicide, molybdenum (Mo) silicide, and tantalum (Ta) silicide.

8. A method of forming a contact layer in a semiconductor structure, the method comprising:

performing a pre-clean process on exposed surfaces of a plurality of first semiconductor regions and a plurality of second semiconductor regions formed on a substrate, wherein the exposed surfaces of the plurality of first and second semiconductor regions are each disposed within openings formed in a dielectric layer disposed over the substrate;

performing a first selective epitaxial deposition process to simultaneously form a first contact layer having a first thickness on the exposed surface of the first semiconductor regions and a second contact layer having a second thickness on the exposed surface of the second semiconductor regions, wherein the second thickness is larger than the first thickness; and

performing a selective removal process to remove the first contact layer and the second contact layer selectively to the plurality of first semiconductor regions, and the dielectric layer until the first contact layer is substantially removed from the first semiconductor regions and a portion of the second contact layer remains on the second semiconductor regions.

9. The method of claim 8, wherein

the first semiconductor regions formed on the substrate comprises silicon,

the second semiconductor regions formed on the substrate comprises silicon germanium, and

the first contact layer and the second contact layer comprise silicon germanium.

10. The method of claim 8, wherein the selective removal process is performed at:

a temperature of between -20°C and 60°C,

a pressure of between 1 Torr and 50 Torr,

a flow rate of a fluorine-containing precursor of between about 5 sccm and 40 sccm,

a flow rate of argon (Ar) of between 4 sccm and 1500 sccm,

a flow rate of helium (He) of between 100 sccm and 5000 sccm, and

a flow rate of nitrogen (N_2) of between 100 sccm and 5000 sccm.

11. The method of claim 8, further comprising:

performing a second selective epitaxial deposition process to form a metal layer on an exposed surface of the first semiconductor regions and an exposed surface of the second contact layer formed on the second semiconductor regions.

12. The method of claim 11, wherein

the metal layer comprises material selected from titanium (Ti) silicide, cobalt (Co) silicide, nickel (Ni) silicide, molybdenum (Mo) silicide, and tantalum (Ta) silicide.

13. A processing system, comprising:

a first processing chamber;

a second processing chamber;

a third processing chamber; and

a system controller configured to:

perform, in the first processing chamber, a pre-clean process on exposed surfaces of a plurality of first semiconductor regions and a plurality of second semiconductor regions formed on a substrate;

perform, in the second processing chamber, a first selective deposition process to epitaxially form a first contact layer on the exposed surfaces of the first semiconductor regions and a second contact layer on the exposed surface of the second semiconductor regions of the substrate; and

perform, in the third processing chamber, a selective removal process to remove the first contact layer selectively to the first semiconductor regions.

14. The processing system of claim 13, wherein the system controller is further configured to transfer the substrate among the first, second, and third processing chambers without breaking vacuum environment.

15. The processing system of claim 13, wherein

the first semiconductor regions formed on the substrate comprises silicon,

the second semiconductor regions formed on the substrate comprises silicon germanium, and

the first contact layer and the second contact layer comprise silicon germanium.

16. The processing system of claim 13, wherein the selective removal process in the third processing chamber is performed at:

a temperature of between -20°C and 60°C,

a pressure of between 1 Torr and 50 Torr,

a flow rate of a fluorine-containing precursor of between about 5 sccm and 40 sccm,

a flow rate of argon (Ar) of between 4 sccm and 1500 sccm,

a flow rate of helium (He) of between 100 sccm and 5000 sccm, and

a flow rate of nitrogen (N_2) of between 100 sccm and 5000 sccm.

17. The processing system of claim 13, further comprising:

a fourth processing chamber, wherein the system controller is further configured to:

perform, in the fourth processing chamber, a second deposition process to form a metal layer on an exposed surface of the first semiconductor regions and an exposed surface of the second contact layer formed on second semiconductor regions formed on the substrate, the metal layer comprising material selected from titanium (Ti) silicide, cobalt (Co) silicide, nickel (Ni) silicide, molybdenum (Mo) silicide, and tantalum (Ta) silicide.

18. The processing system of claim 17, further comprising:

a fifth processing chamber, wherein the system controller is further configured to:

perform, in the fifth processing chamber, a conformal deposition process to form a barrier metal layer on the metal layer, the barrier metal layer comprising material selected from titanium nitride (TiN) and tantalum nitride (TaN)..

19. The processing system of claim 18, further comprising:

a sixth processing chamber,

wherein the system controller is further configured to perform, in the sixth processing chamber, prior to the second deposition process in the fourth processing chamber and subsequent to the selective removal process in the third processing chamber, performing an ashing process to remove a patterning stack.