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DATA COMMUNICATION RECEIVER HAVING BURST ERROR PROTECTED DATA SYNCHRONIZATION

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION:

The present invention relates generally to the field of data communication receivers, and more particularly to a data communication receiver having burst error protected data synchronization.

DESCRIPTION OF THE PRIOR ART:

There are numerous data communication devices available in the marketplace today. An example of one such data communication device is a data communication receiver, such as an alphanumeric paging receiver. Such paging receivers have previously provided data communication capability by utilizing well known paging signaling protocols, such as the the POCSAG signaling protocol. While the POCSAG signaling protocol has provided a satisfactory level of performance for short message data transmission, there are encountered several problems with respect to long message data transmissions. Among these problems are early cancellation of message reception due to burst errors encountered on the transmission channel which corrupts the received data, and a limited battery saving duty cycle. When long messages are to be routinely processed, it is more desirable to extend operating battery life by increasing the battery saving duty cycle, i.e. the ratio of the time the receiver is off to the time the receiver is on. However, by providing longer receiver operating battery lives by increasing the battery saving duty cycle, the problem of burst error corruption of the received data makes it more difficult for the data receiver to obtain synchronization with the transmitted message information, even in satisfactory signal conditions. There

is a need to provide a data communication receiver which has burst error protected data synchronization within a signaling protocol which offers improved receiver operational battery life and long message transmission capability.

SUMMARY OF THE INVENTION

In accordance with one aspect of the present invention, a data communication receiver which provides burst error protected data synchronization comprises a receiver portion for receiving and detecting data synchronization and message information, the data synchronization information comprising at least first and second synchronization code words separated by a predetermined time interval, a correlator, coupled to the receiver portion, correlates the detected first and second synchronization code words, and generates in response thereto first and second coded correlation detection signals. A block start signal generator responsive to the first coded correlation detection signal, generates a first block start signal, and in the absence of the first coded correlation detection signal is responsive to the second coded correlation detection signal for generating a second block start signal. A message decoder is responsive to the first and second block start signals for decoding the detected message information. A display is coupled to the message decoder for displaying the decoded message information.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an electrical block diagram of a data transmission system in accordance with the preferred embodiment of the present invention.

FIG. 2 is an electrical block diagram of a terminal for processing and transmitting message information in accordance with the preferred embodiment of the present invention.

FIGS. 3-5 are timing diagrams illustrating the transmission format of the signaling protocol utilized in accordance with the preferred embodiment of the present invention.

FIGS. 6 and 7 are timing diagrams illustrating the synchronization signals utilized in accordance with the preferred embodiment of the present invention.

FIG. 8 is an electrical block diagram of a data communication receiver in accordance with the preferred embodiment of the present invention.

FIG. 9 is an electrical block diagram of a threshold level extraction circuit utilized in the data communication receiver of FIG. 8.

FIG. 10 is an electrical block diagram of a 4-level decoder utilized in the data communication receiver of FIG. 8.

FIG. 11 is an electrical block diagram of a symbol synchronizer utilized in the data communication receiver of FIG. 8.

FIG. 12 is an electrical block diagram of a 4-level to binary converter utilized in the data communication receiver of FIG. 8.

FIG. 13 is an electrical block diagram of a synchronization correlator utilized in the data communication receiver of FIG. 8.

FIG. 14 is an electrical block diagram of a phase timing generator utilized in the data communication receiver of FIG. 8.

FIG. 15 is a flow chart illustrating the synchronization correlation sequence in accordance with the preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is an electrical block diagram of a data transmission system 100, such as a paging system, in accordance with the preferred embodiment of the present invention In such a data transmission system 100, messages originating either from a phone, as in a system providing numeric data transmission, or from a message entry device, such as an alphanumeric data terminal, are routed through the public switched telephone network (PSTN) to a paging terminal 102 which processes the numeric or alphanumeric message information for transmission by one or more transmitters 104 provided within the system. When multiple transmitters are utilized, the transmitters 104 preferably simulcast transmit the message information to data communication receivers 106. Processing of the numeric and alphanumeric information by the paging terminal 102, and the protocol utilized for the transmission of the messages is described below.

FIG. 2 is an electrical block diagram of the paging terminal 102 utilized for processing and controlling the transmission of the message information in accordance with the preferred embodiment of the present invention. Short messages, such as tone-only and numeric messages which can be readily entered using a Touch-Tone telephone are coupled to the paging terminal 102 through a telephone interface 202 in a manner well known in the art. Longer messages, such as alphanumeric messages which require the use of a data entry device are coupled to the paging terminal 102 through a modem 206 using any of a number of well known modem transmission protocols. When a call to place a message is received, a controller 204 handles the processing of the message. The controller 204 is preferably a microcomputer, such as an MC68000 or equivalent, which is manufactured by Motorola Inc., and which runs various pre-programmed routines for controlling such terminal operations as voice prompts to direct the caller to enter the message, or the handshaking protocol to

enable reception of messages from a data entry device. When a call is received, the controller 204 references information stored in the subscriber database 208 to determine how the message being received is to be processed. The subscriber data base 208 includes, but is not limited to such information as addresses assigned to the data communication receiver, message type associated with the address, and information related to the status of the data communication receiver, such as active or inactive for failure to pay the bill. A data entry terminal 240 is provided which couples to the controller 204, and which is used for such purposes as entry, updating and deleting of information stored in the subscriber data base 208, for monitoring system performance, and for obtaining such information as billing information.

The subscriber database 208 also includes such information as to what transmission frame and to what transmission phase the data communication receiver is assigned, as will be described in further detail below. The received message is stored in an active page file 210 which stores the messages in queues according to the transmission phase assigned to the data communication receiver. In the preferred embodiment of the present invention, four phase queues are provided in the active page file 210. The active page file 210 is preferably a dual port, first in first out random access memory, although it will be appreciated that other random access memory devices, such as hard disk drives, can be utilized as well. Periodically the message information stored in each of the phase queues is recovered from the active page file 210 under control of controller 204 using timing information such as provided by a real time clock 214, or other suitable timing source. The recovered message information from each phase queue is sorted by frame number and is then organized by address, message information, and any other information required for transmission, and then batched into frames based upon message size by frame batching controller 212. The batched frame information for

each phase queue is coupled to frame message buffers 216 which temporarily store the batched frame information until a time for further processing and transmission. Frames are batched in numeric sequence, so that while a current frame is being transmitted, the next frame to be transmitted is in the frame message buffer 216, and the next frame thereafter is being retrieved and batched. At the appropriate time, the batched frame information stored in the frame message buffer 216 is transferred to the frame encoder 218, again maintaining the phase queue relationship. The frame encoder 218 encodes the address and message information into address and message code words required for transmission, as will be described below. The encoded address and message code words are ordered into blocks and then coupled to a block interleaver 220 which interleaves preferably eight code words at a time for transmission in a manner well known in the art. The interleaved code words from each block interleaver 220 are then serially transferred to a phase multiplexer 221, which multiplexes the message information on a bit by bit basis into a serial data stream by transmission phase. The controller 204 next enables a frame sync generator 222 which generates the synchronization code which is transmitted at the start of each frame transmission. The synchronization code is multiplexed with address and message information under the control of controller 204 by serial data splicer 224, and generates therefrom a message stream which is properly formatted for transmission. The message stream is next coupled to a transmitter controller 226, which under the control of controller 204 transmits the message stream over a distribution channel 228. The distribution channel 228 may be any of a number of well known distribution channel types, such as wire line, an RF or microwave distribution channel, or a satellite distribution link. The distributed message stream is transferred to one or more transmitter stations 104, depending upon the size of the communication system. The message stream is first transferred into a dual port buffer

230 which temporarily stores the message stream prior to transmission. At an appropriate time determined by timing and control circuit 232, the message stream is recovered from the dual port buffer 230 and coupled to the input of preferably a 4-level FSK modulator 234. The modulated message stream is then coupled to the transmitter 236 for transmission via antenna 238.

FIGS. 3, 4 and 5 are timing diagrams illustrating the transmission format of the signaling protocol utilized in accordance with the preferred embodiment of the present invention. As shown in FIG. 3, the signaling protocol enables message transmission to data communication receivers, such as pagers, assigned to one or more of 128 frames which are labeled frame 0 through frame 127. It then will be appreciated that the actual number of frames provided within the signaling protocol can be greater or less than described above. The greater the number of frames utilized, the greater the battery life that may be provided to the data communication receivers operating within the system. The fewer the number of frames utilized, the more often messages can be queued and delivered to the data communication receivers assigned to any particular frame, thereby reducing the latency, or time required to deliver messages.

As shown in FIG. 4, the frames comprise a synchronization code (sync) followed preferably by eleven blocks of message information which are labeled block 0 through block 10. As shown in FIG. 5. each block of message information comprises preferably eight address, control or data code words which are labeled word 0 through word 7 for each phase. Consequently, each phase in a frame allows the transmission of up to eighty-eight address, control and data code words. The address, control and data code words are preferably 31,21 BCH code words with an added thirty-second even parity bit which provides an extra bit of distance to the code word set. It will be appreciated that other code words, such as a 23,12 Golay code word could be utilized as well. Unlike the well known

POCSAG signaling protocol which provides address and data code words which utilize the first code word bit to define the code word type, as either address or data, no such distinction is provided for the address and data code words in the signaling protocol utilized with the preferred embodiment of the present invention. Rather, address and data code words are defined by their position within the individual frames.

FIGS. 6 and 7 are timing diagrams illustrating the synchronization code utilized in accordance with the preferred embodiment of the present invention. In particular, as shown in FIG. 6, the synchronization code comprises preferably three parts, a first synchronization code (sync 1), a frame information code word (frame info) and a second synchronization code (sync 2). As shown in FIG. 7, the first synchronization code comprises first and third portions, labeled bit sync 1 and BS1, which are alternating 1,0 bit patterns which provides bit synchronization, and second and fourth portions, labeled "A" and its complement "A bar", which provide frame synchronization. The second and fourth portions are preferably single 32,21 BCH code words which are predefined to provide high code word correlation reliability, and which are also used to indicate the data bit rate at which addresses and messages are transmitted. The table below defines the data bit rates which are used in conjunction with the signaling protocol.

Bit Rate	"A" Value
1600 bps	A1 and A1 bar
3200 bps	A2 and A2 bar
6400 bps	A3 and A3 bar
Not defined	A4 and A4 bar

As shown in the table above, three data bit rates are predefined for address and message transmission, although it will be appreciated that more or less data bit rates can be predefined as well, depending upon the system

requirements. A fourth "A" value is also predefined for future use.

The frame information code word is preferably a single 32,21 BCH code word which includes within the data portion a predetermined number of bits reserved to identify the frame number, such as 7 bits encoded to define frame number 0 to frame number 127.

The structure of the second synchronization code is preferably similar to that of the first synchronization code described above. However, unlike the first synchronization code which is preferably transmitted at a fixed data symbol rate, such as 1600 bps (bits per second), the second synchronization code is transmitted at the data symbol rate at which the address and messages are to be transmitted in any given frame. Consequently, the second synchronization code allows the data communication receiver to obtain "fine" bit and frame synchronization at the frame transmission data bit rate.

In summary the signaling protocol utilized with the preferred embodiment of the present invention comprises 128 frames which include a predetermined synchronization code followed by eleven data blocks which comprise eight address, control or message code words per phase. The synchronization code enables identification of the data transmission rate, and insures synchronization by the data communication receiver with the data code words transmitted at the various transmission rates.

FIG. 8 is an electrical block diagram of the data communication receiver 106 in accordance with the preferred embodiment of the present invention. The heart of the data communication receiver 106 is a controller 816, which is preferably implemented using an MC68HC05HC11 microcomputer, such as manufactured by Motorola, Inc. The microcomputer controller, hereinafter call the controller 816, receives and processes inputs from a number of peripheral circuits, as shown in FIG. 8, and controls the operation and interaction of the peripheral circuits using software subroutines. The use of a microcomputer controller for

processing and control functions is well known to one of ordinary skill in the art.

The data communication receiver 106 is capable of receiving address, control and message information, hereafter called "data" which is modulated using preferably 2-level and 4-level frequency modulation techniques. The transmitted data is intercepted by an antenna 802 which couples to the input of a receiver section 804. Receiver section 804 processes the received data in a manner well known in the art, providing at the output an analog 4-level recovered data signal, hereafter called a recovered data signal. The recovered data signal is coupled to one input of a threshold level extraction circuit 808, and to an input of a 4-level decoder 810. The threshold level extraction circuit 808 is best understood by referring to FIG. 9, and as shown comprises two clocked level detector circuits 902, 904 which have as inputs the recovered data signal. Level detector 902 detects the peak signal amplitude value and provides a high peak threshold signal which is proportional to the detected peak signal amplitude value, while level detector 904 detects the valley signal amplitude value and provides a valley threshold signal which is proportional to the detected valley signal amplitude value of the recovered data signal. The level detector 902, 904 signal outputs are coupled to terminals of resistors 906, 912, respectively. The opposite resistor terminals 906, 912 provide the high threshold output signal (Hi), and the low threshold output signal (Lo), respectively. The opposite resistor terminals 906, 912 are also coupled to terminals of resistors 908, 910, respectively. The opposite resistor 908, 910 terminals are coupled together to form a resistive divider which provides an average threshold output signal (Avg) which is proportional to the average value of the recovered data signal. Resistors 906, 912 have resistor values preferably of 1R, while resistors 908, 910 have resistor values preferably of 2R, realizing threshold output signal values of 17%, 50% and 83%, and which are utilized to enable

decoding the 4-level data signals as will be described below.

When power is initially applied to the receiver portion, as when the data communication receiver is first turned on, a clock rate selector 914 is preset through a control input (center sample) to select a 128X clock, i.e. a clock having a frequency equivalent to 128 times the slowest data bit rate, which as described above is 1600 bps. The 128X clock is generated by 128X clock generator 844, as shown in FIG. 8, which is preferably a crystal controlled oscillator operating at 204.8 KHz (kilohertz). The output of the 128X clock generator 844 couples to an input of frequency divider 846 which divides the output frequency by two to generate a 64X clock at 102.4 KHz. Returning to FIG. 9, the 128X clock allows the level detectors 902, 904 to asynchronously detect in a very short period of time the peak and valley signal amplitude values, and to therefore generate the low (Lo), average (Avg) and high (Hi) threshold output signal values required for modulation decoding. After symbol synchronization is achieved with the synchronization signal, as will be described below, the controller 816 generates a second control signal (Center Sample) to enable selection of a 1X symbol clock which is generated by symbol synchronizer 812 as shown in FIG. 8.

Returning to FIG. 8, the 4-level decoder 810 operation is best understood by referring to FIG. 10. As shown, the 4-level decoder 810 comprises three voltage comparators 1010, 1020, 1030 and a symbol decoder 1040. The recovered data signal couples to an input of the three comparators 1010, 1020, 1030. The high threshold output signal (Hi) couples to the second input of comparator 1010, the average threshold output signal (Avg) couples to the second input of comparator 1020, and the low threshold output signal (Lo) couples to the second input of comparator 1030. The outputs of the three comparators 1010, 1020, 1030 couple to inputs of symbol decoder 1040. The symbol decoder 1040 decodes the inputs according to the table provided below.

Threshold			Output	
Hi	Avg	Lo	MSB	LSB
RC_{in} <	RC_{in} <	RC_{in} <	0	0
RC_{in} <	RC_{in} <	RC_{in} >	0	1
RC_{in} <	RC_{in} >	RC_{in} >	1	1
RC_{in} >	RC_{in} >	RC_{in} >	1	0

As shown in the table above, when the recovered data signal (RC_{in}) is less than all three threshold values, the symbol generated is 00 (MSB = 0, LSB = 0). Thereafter, as each of the three threshold values is exceeded, a different symbol is generated, as shown in the table above.

The MSB output from the 4-level decoder 810 is coupled to an input of the symbol synchronizer 812 and provides a recovered data input generated by detecting the zero crossings in the 4-level recovered data signal. The positive level of the recovered data input represents the two positive deviation excursions of the analog 4-level recovered data signal above the average threshold output signal, and the negative level represents the two negative deviation excursions of the analog 4-level recovered data signal below the average threshold output signal.

The operation of the symbol synchronizer 812 is best understood by referring to FIG. 11. The 64X clock at 102.4 KHz which is generated by frequency divider 846, is coupled to an input of a 32X rate selector 1120. The 32X rate selector 1120 is preferably a divider which provides selective division by 1 or 2 to generate a sample clock which is thirty-two times the symbol transmission rate. A control signal (1600/3200) is coupled to a second input of the 32X rate selector 1120, and is used to select the sample clock rate for symbol transmission rates of 1600 and 3200 symbols per second. The selected sample clock is coupled to an input of 32X data oversampler 1110 which samples the recovered data signal (MSB) at thirty-two samples per symbol. The symbol samples are coupled to an input of a data edge detector 1130 which generates an

output pulse when a symbol edge is detected. The sample clock is also coupled to an input of a divide-by-16/32 circuit 1140 which is utilized to generate 1X and 2X symbol clocks synchronized to the recovered data signal. The divided-by-16/32 circuit 1140 is preferably an up/down counter. When the data edge detector 1130 detects a symbol edge, a pulse is generated which is gated by AND gate 1150 with the current count of divide-by-16/32 circuit 1140. Concurrently, a pulse is generated by the data edge detector 1130 which is also coupled to an input of the divide-by-16/32 circuit 1140. When the pulse coupled to the input of AND gate 1150 arrives before the generation of a count of thirty-two by the divide-by-16/32 circuit 1140, the output generated by AND gate 1150 causes the count of divide-by-16/32 circuit 1140 to be advanced by one count in response to the pulse which is coupled to the input of divide-by-16/32 circuit 1140 from the data edge detector 1130, and when the pulse coupled to the input of AND gate 1150 arrives after the generation of a count of thirty-two by the divide-by-16/32 circuit 1140, the output generated by AND gate 1150 causes the count of divide-by-16/32 circuit 1140 to be retarded by one count in response to the pulse which is coupled to the input of divide-by-16/32 circuit 1140 from the data edge detector 1130, thereby enabling the synchronization of the 1X and 2X symbol clocks with the recovered data signal. The symbol clock rates generated are best understood from the table below.

Input Clock (Relative)	Control Input (SPS)	Rate Selector Divide Ratio	Rate Selector Output	2X Symbol Clock (BPS)	1X Symbol Clock (BPS)
64X	1600	by 2	32X	3200	1600
64X	3200	by 1	64X	6400	3200

As shown in the table above, the 1X and 2X symbol clocks are generated 1600, 3200 and 6400 bits per second and are synchronized with the recovered data signal.

The 4-level binary converter 814 is best understood by referring to FIG. 12. The 1X symbol clock is coupled to a first clock input of a clock rate selector 1210. A 2X symbol clock also couples to a second clock input of the clock rate selector 1210. The symbol output signals (MSB, LSB) are coupled to inputs of an input data selector 1230. A selector signal (2L/4L) is coupled to a selector input of the clock rate selector 1210 and the selector input of the input data selector 1230, and provides control of the conversion of the symbol output signals as either 2-level FSK data, or 4-level FSK data. When the 2-level FSK data conversion (2L) is selected, only the MSB output is selected which is coupled to the input of a parallel to serial converter 1220. The 1X clock input is selected by clock rate selector 1210 which results in a single bit binary data stream to be generated at the output of the parallel to serial converter 1220. When the 4-level FSK data conversion (4L) is selected, both the LSB and MSB outputs are selected which are coupled to the inputs of the parallel to serial converter 1220. The 2X clock input is selected by clock rate selector 1210 which results in a serial two bit binary data stream to be generated at 2X the symbol rate, which is provided at the output of the parallel to serial converter 1220.

Returning to FIG. 8, the serial binary data stream generated by the 4-level to binary converter 814 is coupled to inputs of a synchronization word correlator 818 and a demultiplexer 820. The synchronization word correlator is best understood with reference to FIG. 13. Predetermined "A" word synchronization patterns are recovered by the controller 816 from a code memory 822 and are coupled to an "A" word correlator 1310. When the synchronization pattern received matches one of the predetermined "A" word synchronization patterns within an acceptable margin of

error, an "A" or "A-bar" output is generated and is coupled to controller 816. The particular "A" or "A-bar" word synchronization pattern correlated provides frame synchronization to the start of the frame ID word, and also defines the data bit rate of the message to follow, as was previously described.

The serial binary data stream is also coupled to an input of the frame word decoder 1320 which decodes the frame word and provides an indication of the frame number currently being received by the controller 816. During sync acquisition, such as following initial receiver turn-on, power is supplied to the receiver portion by battery saver circuit 848, shown in FIG. 8, which enabled the reception of the "A" synchronization word, as described above, and which continues to be supplied to enable processing of the remainder of the synchronization code. The controller 816 compares the frame number currently being received with a list of assigned frame numbers stored in code memory 822. Should the currently received frame number differ from an assigned frame numbers, the controller 816 generates a battery saving signal which is coupled to an input of battery saver circuit 848, suspending the supply of power to the receiver portion. The supply of power will be suspended until the next frame assigned to the receiver, at which time a battery saver signal is generated by the controller 816 which is coupled to the battery saving circuit 848 to enable the supply of power to the receiver portion to enable reception of the assigned frame.

Returning to the operation of the synchronization correlator shown in FIG. 13, a predetermined "C" word synchronization pattern is recovered by the controller 816 from a code memory 822 and is coupled to a "C" word correlator 1330. When the synchronization pattern received matches the predetermined "C" word synchronization pattern with an acceptable margin of error, a "C" or "C-bar" output is generated which is coupled to controller 816. The particular "C" or "C-bar" synchronization word correlated

provides "fine" frame synchronization to the start of the data portion of the frame.

Returning to FIG. 8, the start of the actual data portion is established by the controller 816 generating a block start signal (Blk Start) which is coupled to inputs of a word de-interleaver 824 and a data recovery timing circuit 826. The data recovery timing circuit 826 is best understood by referring to FIG. 14. A control signal (2L / 4L) is coupled to an input of clock rate selector 1410 which selects either 1X or 2X symbol clock inputs. The selected symbol clock is coupled to the input of a phase generator 1430 which is preferably a clocked ring counter which is clocked to generate four phase output signals (Ø1-Ø4). A block start signal is also coupled to an input of the phase generator 1430, and is used to hold the ring counter in a predetermined phase until the actual decoding of the message information is to begin. When the block start signal releases the phase generator 1430, the phase generator 1430 begins generating clocked phase signals which are synchronized with the incoming message symbols.

Referring back to FIG. 8, the clocked phase signal outputs are coupled to inputs of a phase selector 828. During operation, the controller 816 recovers from the code memory 822, the transmission phase number to which the data communication receiver is assigned. The phase number is transferred to the phase select output (Ø Select) of the controller 816 and is coupled to an input of phase selector 828. A phase clock, corresponding to the transmission phase assigned, is provided at the output of the phase selector 828 and is coupled to clock inputs of the demultiplexer 820, block de-interleaver 824, and address and data decoders 830 and 832, respectively. The demultiplexer 820 is used to select the binary bits associated with the assigned transmission phase which are then coupled to the input of block de-interleaver 824, and clocked into the de-interleaver array on each corresponding phase clock. The de-interleaver array is an 8x32 bit array which de-interleaves eight interleaved address, control or

message code words, corresponding to one transmission block. The de-interleaved address code words are coupled to the input of address correlator 830. The controller 816 recovers the address patterns assigned to the data communication receiver, and couples the patterns to a second input of the address correlator. When any of the de-interleaved address code words matches any of the address patterns assigned to the data communication receiver within an acceptable margin of error, the message information associated with the address is then decoded by the data decoder 832 and stored in a message memory 850 in a manner well known to one of ordinary skill in the art. Following the storage of the message information, a sensible alert signal is generated by the controller 816. The sensible alert signal is preferably an audible alert signal, although it will be appreciated that other sensible alert signals, such as tactile alert signals, and visual alert signals can be generated as well. The audible alert signal is coupled by the controller 816 to an alert driver 834 which is used to drive an audible alerting device, such as a speaker or a transducer 836. The user can override the alert signal generation through the use of user input controls 838 in a manner well known in the art.

Following the detection of an address associated with the data communication receiver, the message information is coupled to the input of data decoder 832 which decodes the encoded message information into preferably a BCD or ASCII format suitable for storage and subsequent display. The stored message information can be recalled by the user using the user input controls 838 whereupon the controller 816 recovers the message information from memory, and provides the message information to a display driver 840 for presentation on a display 842, such as an LCD display.

FIG. 15 is a flow chart describing the operation of the data communication receiver in accordance with the preferred embodiment of the present invention. At step 1502, when the data communication receiver is turned on, the controller operation is initialized, at step 1504.

Power is periodically applied to the receiver portion to enable receiving information present on the assigned RF channel. When data is not detected on the channel in a predetermined time period, battery saver operation is resumed, at step 1508. When data is detected on the channel, at step 1506, the synchronization word correlator begins searching for bit synchronization at step 1510. When bit synchronization is obtained, at step 1510, the "A" word correlation begins at step 1512. When the non-complemented "A" word is detected, at step 1514, the message transmission rate is identified as described above, at step 1516, and because frame synchronization is obtained, the time (T1) to the start of the frame identification code word is identified, at step 1518. When the non-complemented "A" word is not detected, at step 1514, indicating the non-complemented "A" word may have been corrupted by a burst error during transmission, a determination is made whether the complemented "A" bar" is detected, at step 1520. When the "A bar" word is not detected at step 1512, indicating that the "A-bar" word may also have been corrupted by a burst error during transmission, battery saver operation is again resumed, at step 1508. When the "A-bar" word is detected, at step 1520, the message transmission rate is identified as described above, at step 1522, and because frame synchronization is obtained, the time (T2) to the start of the frame identification code word is identified, at step 1524. At the appropriate time, decoding of the frame identification word occurs, at step 1526. When the frame ID detected is not one assigned to the data communication receiver, at step 1528, battery saving is resumed, at step 1508, and remains so until the next assigned frame is to be received. When the decoded frame ID corresponds to an assigned frame ID, at step 1528, the message reception rate is set, at step 1530. An attempt to bit synchronize at the message transmission rate is next made at step 1532. When bit synchronization is obtained, at step 1533, the "C" word correlation begins at step 1534. When the non-complemented

"C" word is detected, at step 1536, frame synchronization is obtained, and the time (T3) to the start of the message information is identified, at step 1538.

When the non-complemented "C" word is not detected, at step 1536, indicating the non-complemented "C" word may have been corrupted by a burst error during transmission, a determination is made whether the complement "C bar" is detected, at step 1540. When the "C bar" word is not detected at step 1540, indicating that the "C-bar" word may also have been corrupted by a burst error during transmission, battery saver operation is again resumed, at step 1508. When the "C-bar" word is detected, at step 1540, frame synchronization is obtained, and the time (T4) to the start of the message information is identified, at step 1542. At the appropriate time, message decoding can begin at step 1544.

In summary, by providing multiple synchronization code words which are spaced in time, the reliability of synchronizing with synchronization information which is subject to burst error corruption is greatly enhanced. The use of a predetermined synchronization code word as the first synchronization code word, and a second predetermined synchronization code word which is the complement of the first predetermined synchronization code word, allows accurate frame synchronization on either the first or the second predetermined synchronization code word. By encoding the synchronization code words, additional information, such as the transmission data rate can be provided, thereby enabling the transmission of message information at several data bit rates. By using a second coded synchronization word pair, "fine" frame synchronization at the actual message transmission rate can be achieved, and again due to spacing in time of the synchronization code words, the reliability of synchronizing at a different data bit rate with synchronization information which is subject to burst error corruption is greatly enhanced, thereby improving the

reliability of the data communication receiver to receive and present messages to the receiver user.

We claim:

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1. A data communication receiver, providing burst error protected data synchronization, comprising:

a receiver portion for receiving and detecting synchronization data and message information, Willarding at least first and second synchronization code words separated by a predetermined transmission time interval;

means, coupled to said receiver portion, for correlating the detected first and second synchronization code words, and for generating in response thereto first and second coded correlation detection signals;

generating means, responsive to the first coded correlation detection signal, for generating a first block start signal, said generating means, being further responsive, in the absence of the first coded correlation detection signal, to the second coded correlation detection signal for generating a second block start signal;

message decoding means, responsive to the first and second block start signals, for decoding the detected message information; and

display means, coupled to said message decoding means, for displaying the decoded message information.

2. The data communication receiver according to claim 1, wherein the second synchronization code word is different than the first synchronization code word.

3. The data communication receiver according to claim 1, wherein the predetermined time interval corresponds substantially to the burst error duration expected on a data channel.

4. The data communication receiver according to claim 1, wherein the first and second block start signals identify a substantially identical point in time where message information decoding is to begin.

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5. The data communication receiver according to claim 1, wherein the message information is transmitted in a sequence of frames including synchronization data and message information, and the synchronization data further includes frame information designating a frame number, and wherein the data communication receiver further comprises:

battery saving means, for controlling the supply of power to said receiver portion;

code memory means, for storing a predetermined frame number to which the data communication receiver is assigned; and

frame word decoder means, responsive to the first and second block start signals and to the detected frame number, for generating a frame decode signal when the detected frame number matches the predetermined frame number,

said battery saving means being responsive to the frame decode signal, for maintaining power to said receiver portion to enable the reception of the message information during the assigned frame.

6. The data communication receiver according to claim 1, wherein the first and second coded synchronization code words are selected from a plurality of synchronization code words which designate message information transmission rates, and wherein said correlation means further generates a data rate signal indicative of the expected message information transmission rate.

7. The data communication receiver according to claim 6 wherein the data synchronization information further includes at least third and fourth synchronization code words separated by a second predetermined transmission time interval, and which are transmitted subsequent to the transmission of the first and second synchronization code words, and wherein the data communication receiver further comprises

second means, responsive to the data rate signal, for correlating the third and fourth synchronization code words at the expected message information transmission rate, and for generating in response thereto third and fourth coded correlation detection signals,

said generating means being further responsive to the third coded correlation detection signal, for further generating a third block start signal, said generating means being further responsive, in the absence of the third coded correlation detection signal, to the fourth coded correlation detection signal for generating a fourth block start signal,

wherein said message decoding means, is further responsive to the third and fourth block start signals, for decoding the detected message information, and wherein said display means displays the decoded message information.

8. The data communication receiver according to claim 7, wherein the third and fourth block start signals identify a substantially identical point in time where message information decoding is to begin.

9. A data communication system providing burst error protected data synchronization, comprising:

transmitting means comprising

means for receiving message information designated for a data communication receiver,

means for generating at least first and second synchronization code words,

means for formatting the first and second synchronization code words with a predetermined time interval therebetween to derive synchronization data, said formatting means further formatting the synchronization data with message information,

means for transmitting the synchronization data and message information on a data channel; and

a data communication receiver comprising

a receiver portion for receiving and detecting the transmitted synchronization data and message information;

means, coupled to said receiver portion, for correlating the detected first and second synchronization code words, and for generating in response thereto first and second coded correlation detection signals;

generating means, responsive to the first coded correlation detection signal, for generating a first block start signal, said generating means, being further responsive, in the absence of the first coded correlation detection signal, to the second coded correlation detection signal for generating a second block start signal;

message decoding means, responsive to the first and second block start signals, for decoding the detected message information; and

display means, coupled to said message decoding means, for displaying the decoded message information.

10. The data communication receiver according to claim 9, wherein the second synchronization code word is different than the first synchronization code word.

11. The data communication receiver according to claim 9, wherein the predetermined time interval corresponds substantially to the burst error duration expected on the data channel.

12. The data communication receiver according to claim 9, wherein the first and second block start signals identify a substantially identical point in time where message information decoding is to begin.

DATA COMMUNICATION RECEIVER HAVING BURST ERROR PROTECTED DATA SYNCHRONIZATION

A data communication receiver (106) providing burst error protected data synchronization comprises a receiver portion (804) for receiving and detecting synchronization data and message information. The synchronization data comprises at least first and second synchronization code words separated by a predetermined transmission time interval. A synchronization correlator (818, 1310 or 1330) correlates for the first synchronization code word, and in the absence of correlating the first synchronization code word, correlates for the second synchronization code word, thereby insuring synchronization with the received message information.

Fig. 8 accompanies this abstract.


102
PAGING TERMINAL
TO PSTN
104
TRANSMITTER
100
106
DATA COMMUNICATION RECEIVER

FIG. 1

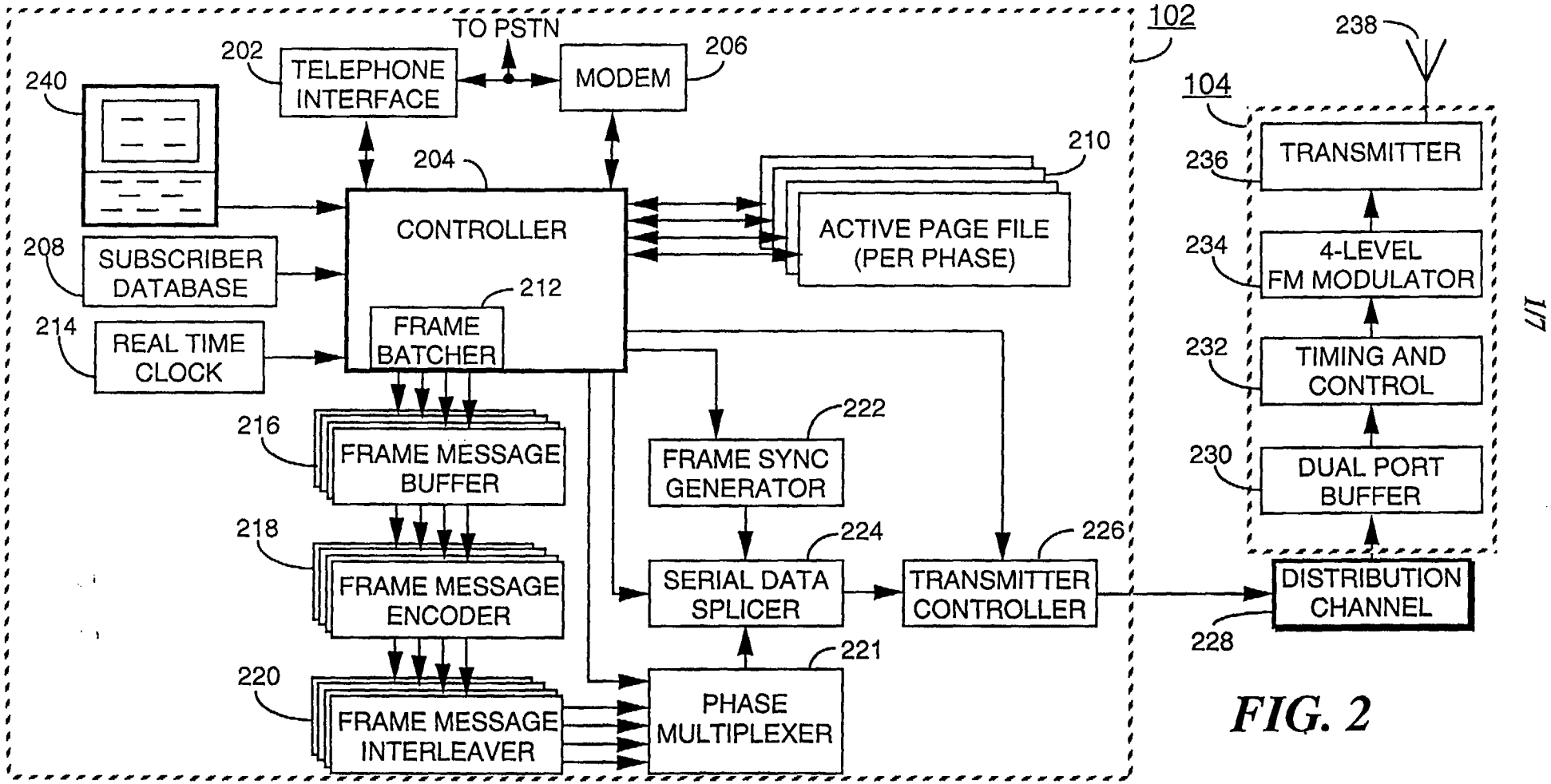

102
TO PSTN
202
TELEPHONE INTERFACE
206
MODEM
240
204
CONTROLLER
210
ACTIVE PAGE FILE (PER PHASE)
208
SUBSCRIBER DATABASE
212
FRAME BATCHER
214
REAL TIME CLOCK
216
FRAME MESSAGE BUFFER
222
FRAME SYNC GENERATOR
218
FRAME MESSAGE ENCODER
224
SERIAL DATA SPLICER
226
TRANSMITTER CONTROLLER
221
220
FRAME MESSAGE INTERLEAVER
PHASE MULTIPLEXER
238
104
TRANSMITTER
236
4-LEVEL FM MODULATOR
234
TIMING AND CONTROL
232
DUAL PORT BUFFER
230
DISTRIBUTION CHANNEL
228

FIG. 2

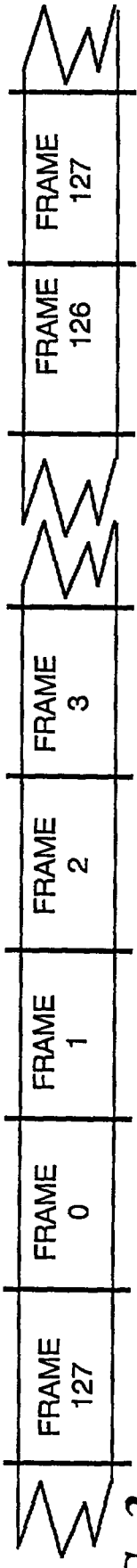


FIG. 3

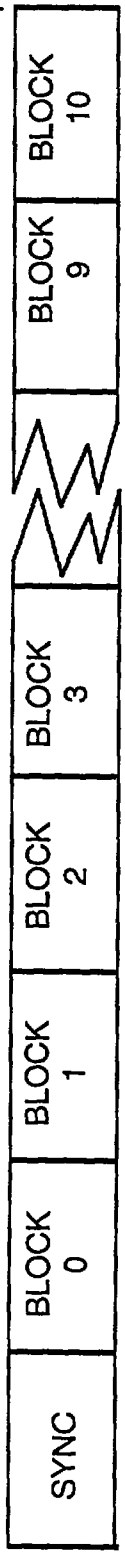


FIG. 4

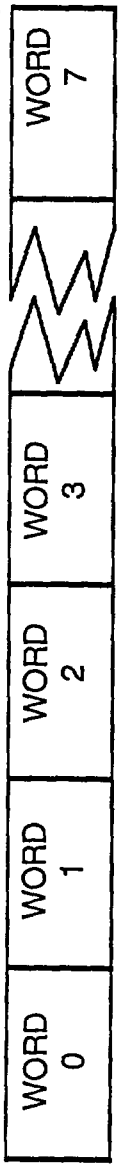


FIG. 5

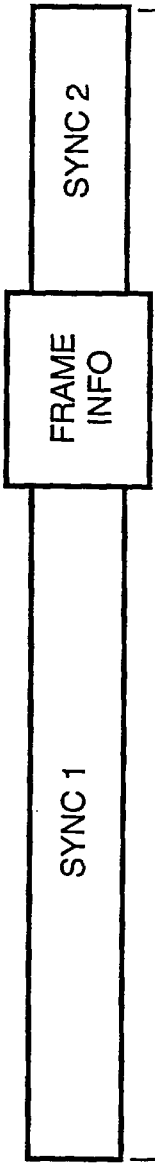


FIG. 6

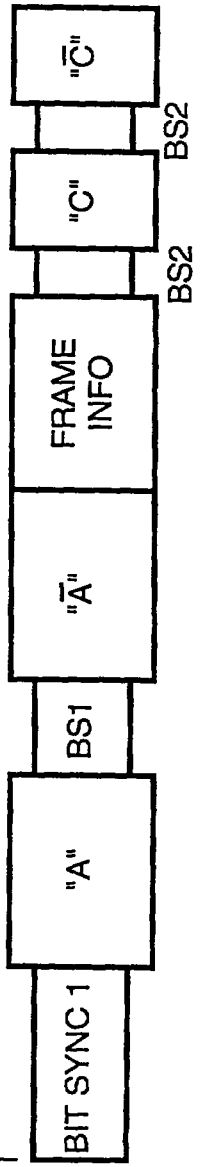
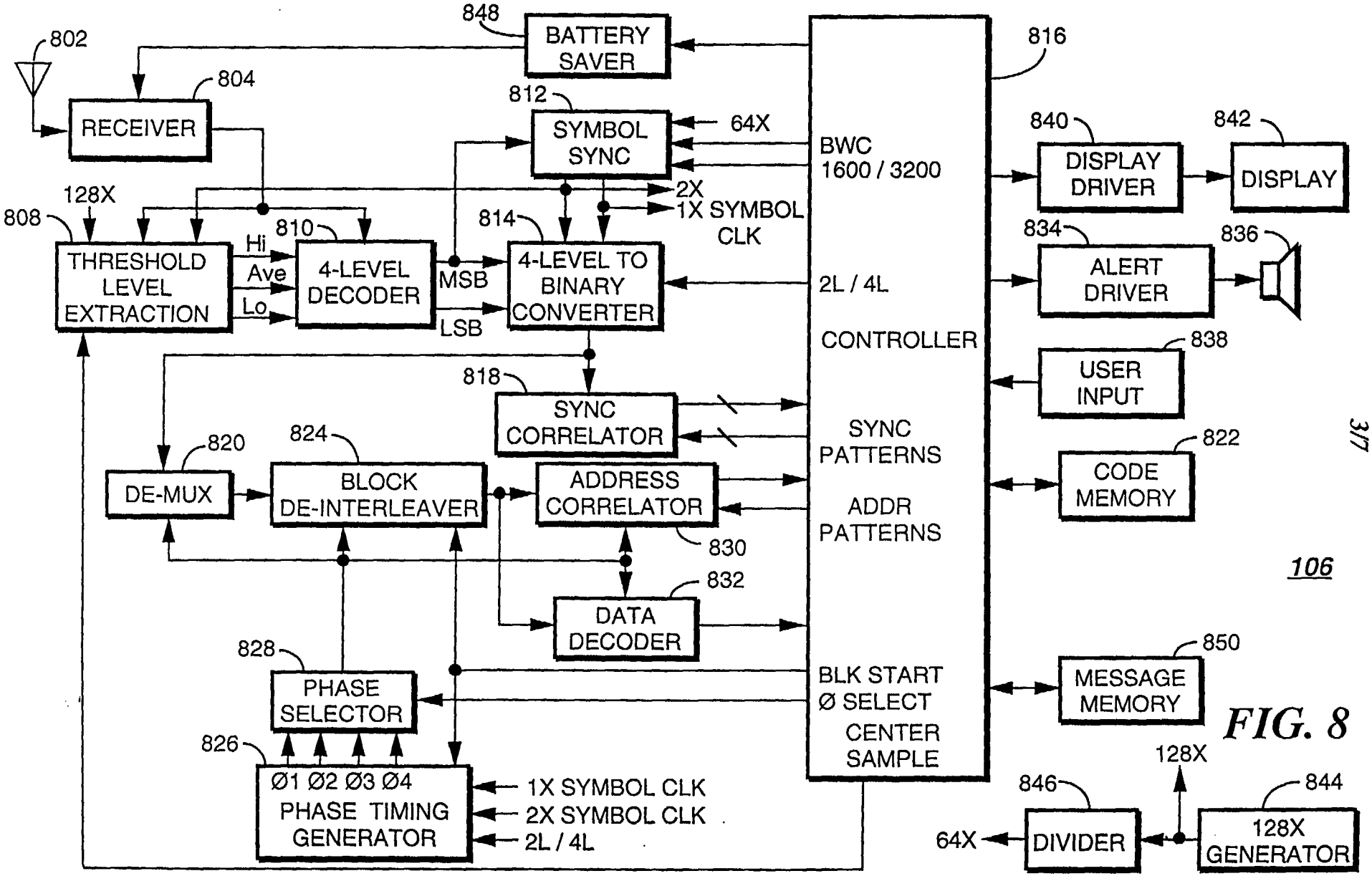


FIG. 7


802
848
BATTERY SAVER
816
804
RECEIVER
812
SYMBOL SYNC
64X
BWC 1600 / 3200
840
DISPLAY DRIVER
842
DISPLAY
128X
808
2X
1X SYMBOL CLK
THRESHOLD LEVEL EXTRACTION
Hi
Ave
Lo
810
4-LEVEL DECODER
MSB
LSB
814
4-LEVEL TO BINARY CONVERTER
2L / 4L
834
ALERT DRIVER
836
CONTROLLER
838
USER INPUT
818
SYNC CORRELATOR
SYNC PATTERNS
820
824
822
DE-MUX
BLOCK DE-INTERLEAVER
ADDRESS CORRELATOR
CODE MEMORY
ADDR PATTERNS
830
832
DATA DECODER
828
850
PHASE SELECTOR
BLK START
Ø SELECT
CENTER SAMPLE
MESSAGE MEMORY
826
Ø1 Ø2 Ø3 Ø4
PHASE TIMING GENERATOR
1X SYMBOL CLK
2X SYMBOL CLK
2L / 4L
128X
846
844
64X
DIVIDER
128X GENERATOR
106
FIG. 8
3/7

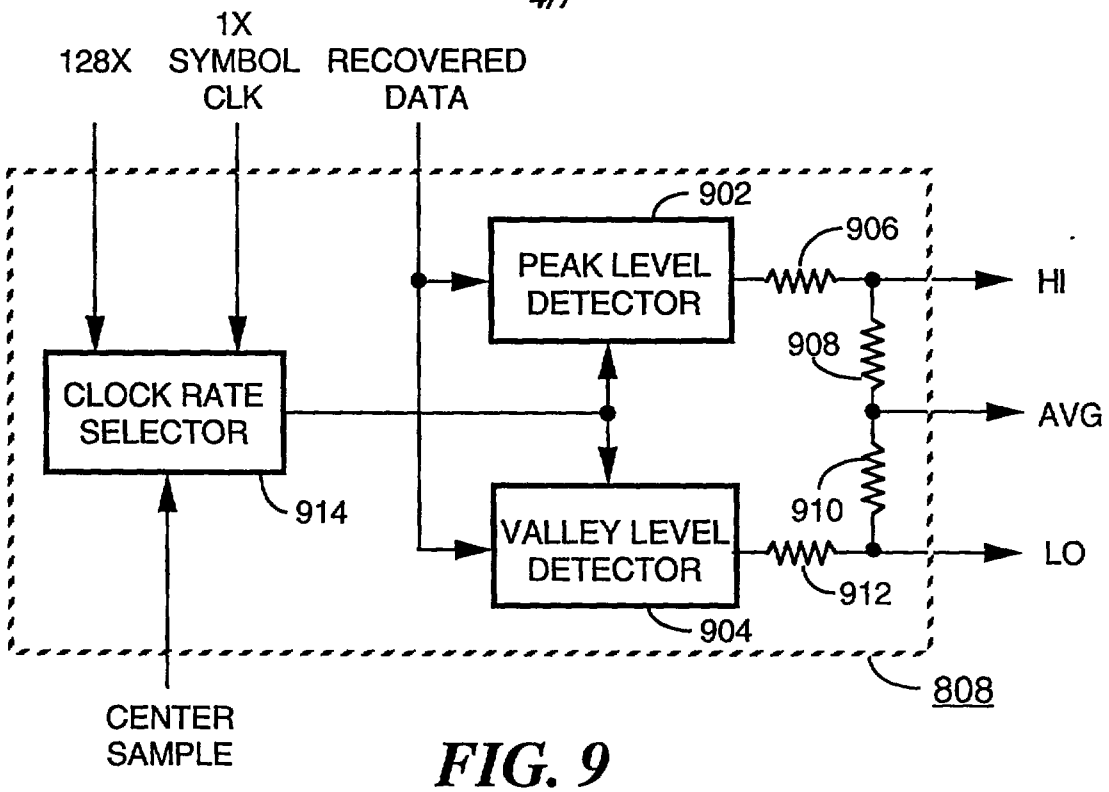

1X
128X
SYMBOL
CLK
RECOVERED
DATA
902
906
PEAK LEVEL
DETECTOR
HI
908
CLOCK RATE
SELECTOR
AVG
914
910
VALLEY LEVEL
DETECTOR
LO
912
904
808
CENTER
SAMPLE

FIG. 9

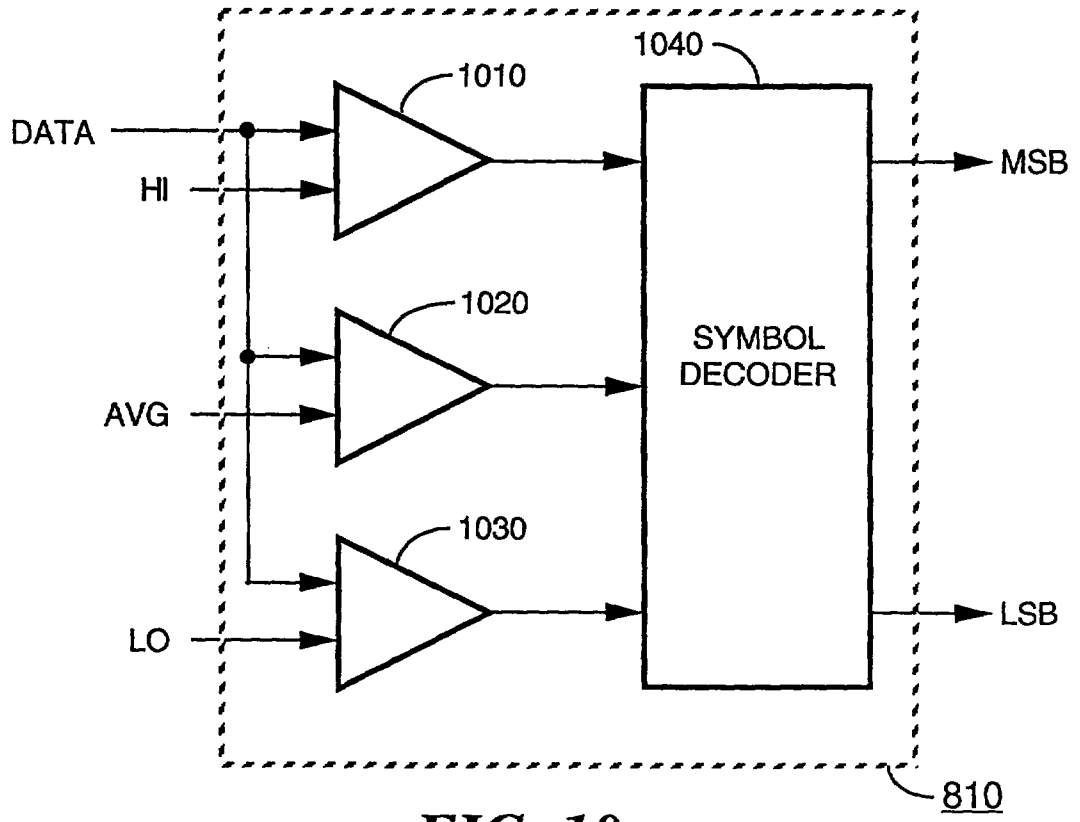

1040
1010
DATA
HI
MSB
1020
SYMBOL
DECODER
AVG
1030
LO
LSB
810

FIG. 10

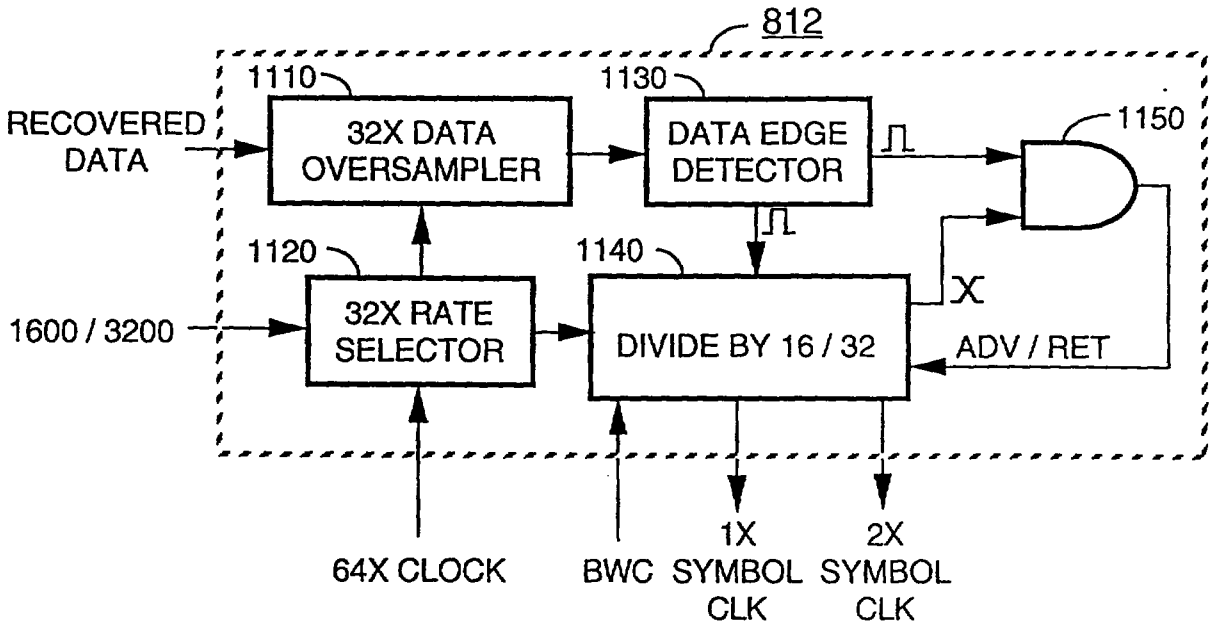

812
1110
1130
RECOVERED DATA
32X DATA OVERSAMPLER
DATA EDGE DETECTOR
1150
1120
1140
1600 / 3200
32X RATE SELECTOR
DIVIDE BY 16 / 32
X
ADV / RET
64X CLOCK
BWC
1X SYMBOL CLK
2X SYMBOL CLK

FIG. 11

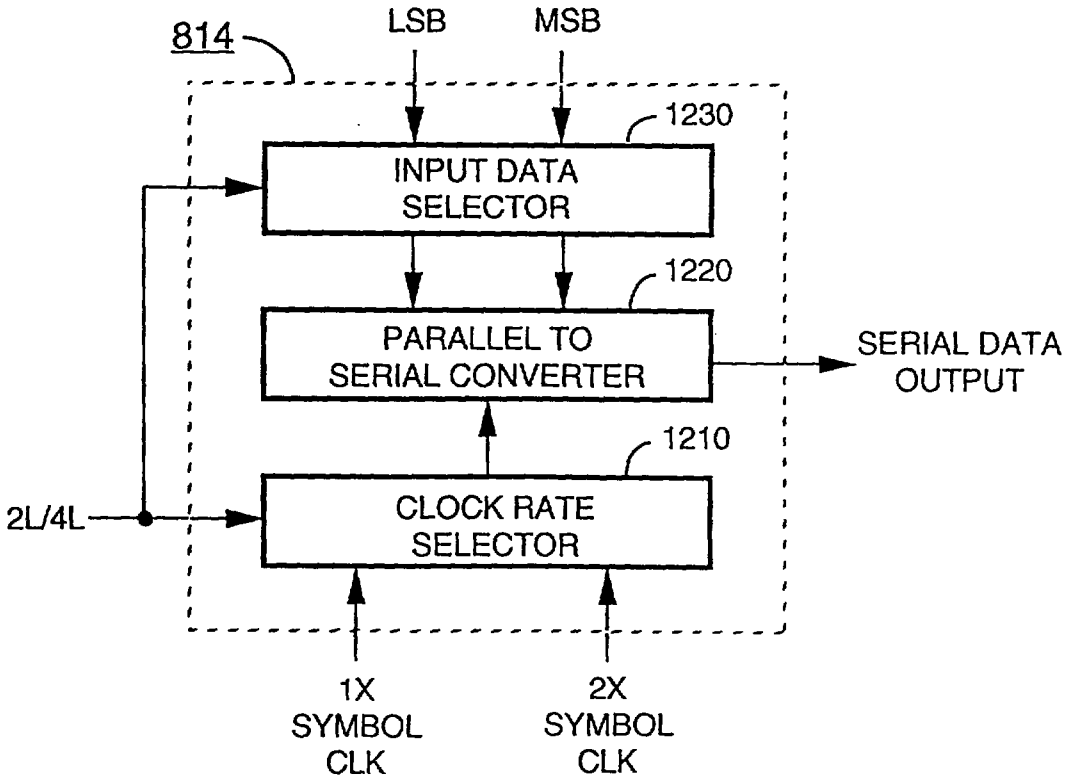

814
LSB
MSB
1230
INPUT DATA SELECTOR
1220
PARALLEL TO SERIAL CONVERTER
SERIAL DATA OUTPUT
1210
2L/4L
CLOCK RATE SELECTOR
1X SYMBOL CLK
2X SYMBOL CLK

FIG. 12

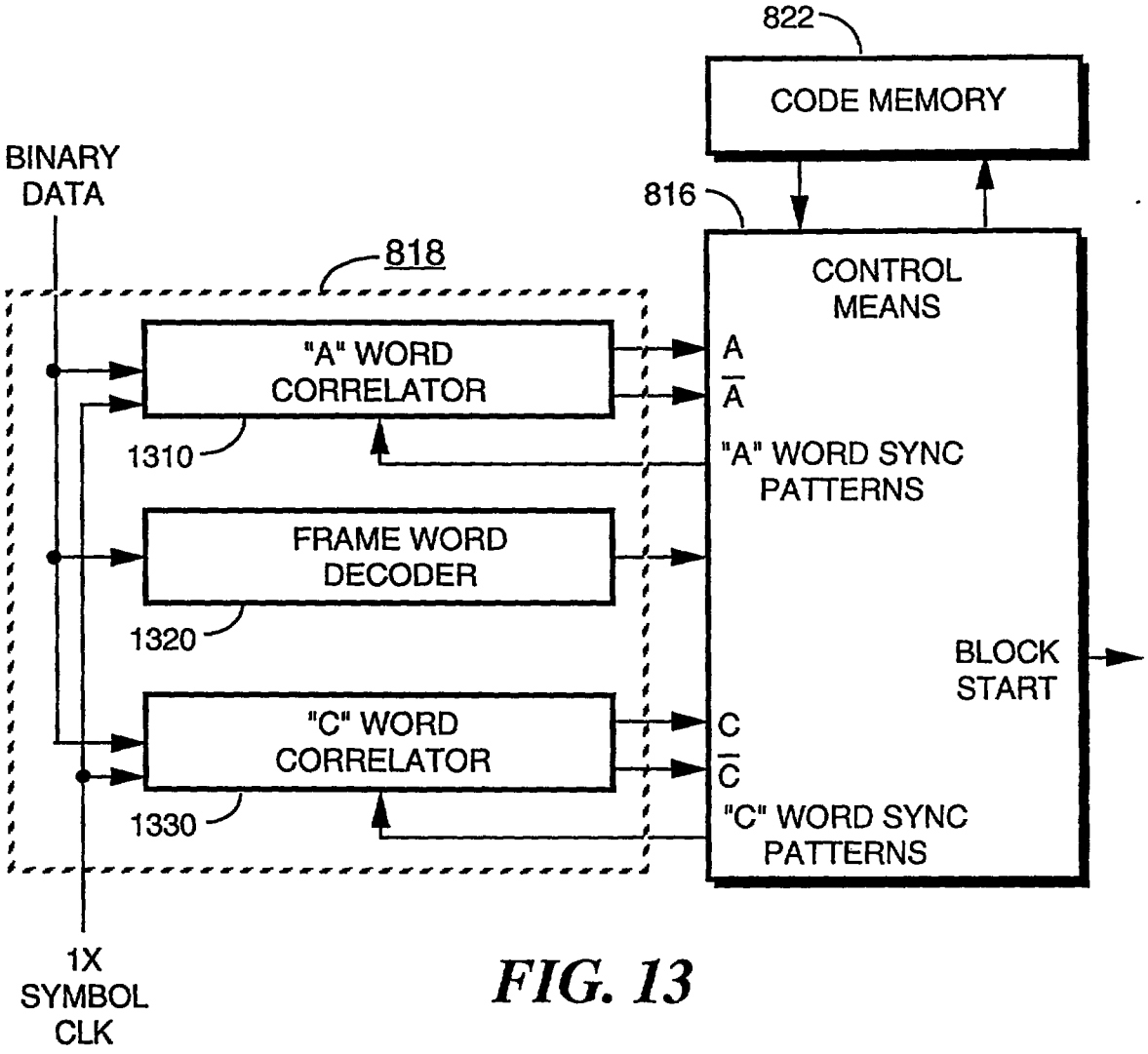

822
CODE MEMORY
BINARY DATA
816
818
CONTROL MEANS
"A" WORD CORRELATOR
A
$\overline{A}$
1310
"A" WORD SYNC PATTERNS
FRAME WORD DECODER
1320
BLOCK START
"C" WORD CORRELATOR
C
$\overline{C}$
1330
"C" WORD SYNC PATTERNS
1X SYMBOL CLK

FIG. 13

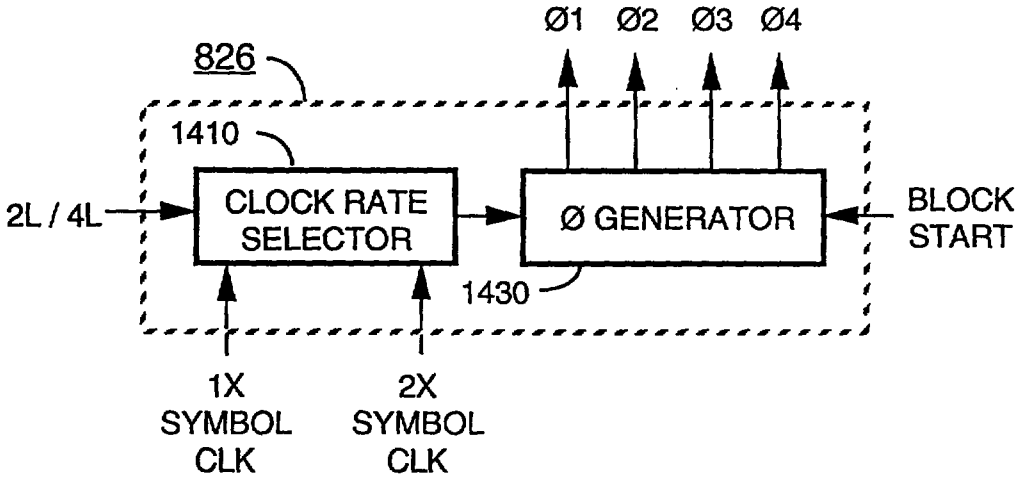

Ø1 Ø2 Ø3 Ø4
826
1410
2L / 4L
CLOCK RATE SELECTOR
Ø GENERATOR
BLOCK START
1430
1X SYMBOL CLK
2X SYMBOL CLK

FIG. 14

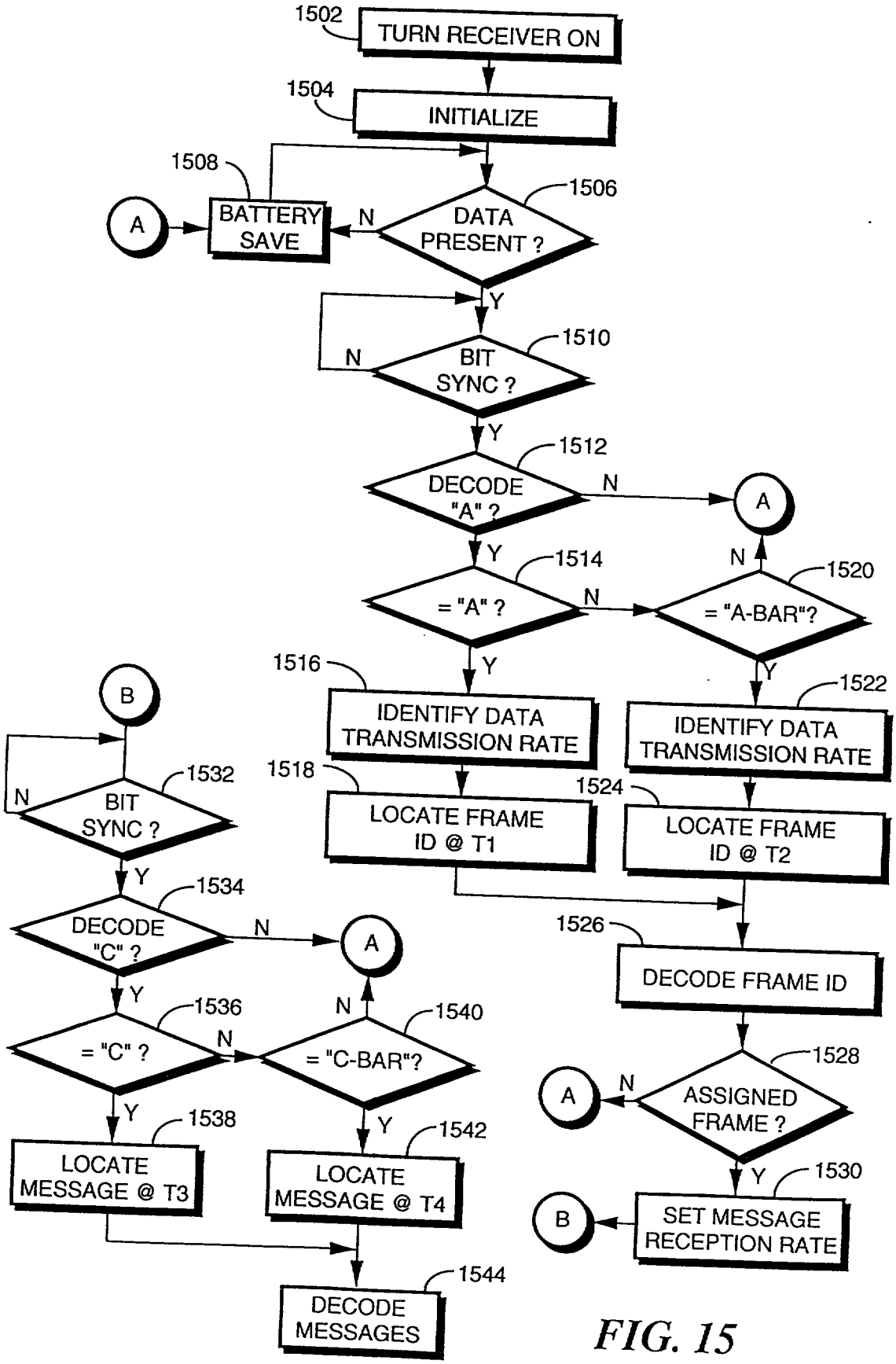

1502
TURN RECEIVER ON
1504
INITIALIZE
1508
BATTERY SAVE
A
N
1506
DATA PRESENT ?
Y
N
1510
BIT SYNC ?
Y
1512
DECODE "A" ?
N
A
Y
1514
= "A" ?
N
N
1520
= "A-BAR"?
Y
1516
IDENTIFY DATA TRANSMISSION RATE
Y
1522
IDENTIFY DATA TRANSMISSION RATE
B
1518
LOCATE FRAME ID @ T1
1524
LOCATE FRAME ID @ T2
N
1532
BIT SYNC ?
Y
1534
DECODE "C" ?
N
A
1526
DECODE FRAME ID
Y
1536
= "C" ?
N
N
1540
= "C-BAR"?
1528
A
N
ASSIGNED FRAME ?
Y
1538
LOCATE MESSAGE @ T3
Y
1542
LOCATE MESSAGE @ T4
Y
1530
B
SET MESSAGE RECEPTION RATE
1544
DECODE MESSAGES

FIG. 15

REPLACEMENT SHEET
22 JAN 2002

1. A data communication receiver, providing burst error protected data synchronization, comprising:

a receiver portion for receiving and detecting synchronization data and message information, having at least first and second synchronization code words separated by a predetermined transmission time interval;

means, coupled to said receiver portion, for correlating the detected first and second synchronization code words, and for generating in response thereto first and second coded correlation detection signals;

generating means, responsive to the first coded correlation detection signal, for generating a first block start signal, said generating means, being further responsive, in the absence of the first coded correlation detection signal, to the second coded correlation detection signal for generating a second block start signal;

message decoding means, responsive to the first and second block start signals, for decoding the detected message information; and

display means, coupled to said message decoding means, for displaying the decoded message information.

2. The data communication receiver according to claim 1, wherein the second synchronization code word is different than the first synchronization code word.

3. The data communication receiver according to claim 1, wherein the predetermined time interval corresponds substantially to the burst error duration expected on a data channel.

4. The data communication receiver according to claim 1, wherein the first and second block start signals identify a substantially identical point in time where message information decoding is to begin.