

Abstract:

An information processing system comprises several sub-circuits (10, 20, 30), each performing a part of the processing of the information or data. The operation of the sub-circuits is synchronised with clock signals applied to clock inputs (11, 21, 31) of the sub-circuits. The clock signals are derived from a system clock (60) and transferred to each sub-circuit (30) via the sub-circuit or sub-circuits (10, 20) preceding that sub-circuit in processing the data. To avoid deterioration of clock pulses while transferring the interconnects between the sub-circuits, clock regeneration circuitry is arranged in the chain of sub-circuits. The clock regeneration circuitry is preferably integrated together with the data-processing sub-circuits.

(Figure 1)

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