

CLAIMS

What is claimed is:

- 1 1. A method, comprising:
2 initializing a counter in a controller coupled with a memory array;
3 activating at least a portion of a first group of memory cells of the memory
4 array by applying a read voltage to the memory array;
5 determining that a set of memory cells has been activated based at least in part
6 on applying the read voltage;
7 updating the counter to a first value based at least in part on determining that
8 the set of memory cells has been activated;
9 comparing the first value of the updated counter to a threshold stored at the
10 controller; and
11 reading one or more memory cells of the memory array based at least in part
12 on the comparison.
- 1 2. The method of claim 1, wherein the comparing further comprises:
2 determining that the first value satisfies the threshold stored at the controller;
3 and
4 stopping application of the read voltage to the memory array based at least in
5 part on the determination that the first value satisfies the threshold, wherein the one or more
6 memory cells are read after application of the read voltage has stopped.
- 1 3. The method of claim 1, wherein the comparing further comprises:
2 determining that the first value does not satisfy the threshold stored at the
3 controller;
4 maintaining application of the read voltage to the memory array based at least
5 in part on the determination that the first value does not satisfy the threshold;
6 determining that a second set of memory cells has been activated based at least
7 in part on maintaining application of the read voltage; and
8 updating the counter to a second value based at least in part on determining
9 that the second set of memory cells has been activated, wherein the one or more memory
10 cells are read based at least in part on updating the counter to the second value.

1 4. The method of claim 1, further comprising:
2 determining that the set of memory cells that has been activated corresponds to
3 a first logic state.

1 5. The method of claim 4, wherein the first logic state corresponds to a
2 first set of threshold voltages that is less than a second set of threshold voltages associated
3 with a second logic state.

1 6. The method of claim 1, wherein the first group of memory cells are
2 configured with a predetermined number of memory cells having a first logic state.

1 7. The method of claim 1, wherein the first group of memory cells are
2 configured with a fixed number of memory cells independent of a total number of memory
3 cells in the first group.

1 8. The method of claim 1, wherein a first half of the first group of
2 memory cells corresponds to a first logic state and a second half of the first group of memory
3 cells corresponds to a second logic state.

1 9. The method of claim 1, wherein each memory cell of the set of
2 memory cells corresponds to a first logic state.

1 10. The method of claim 1, wherein the set of memory cells is half of the
2 first group of memory cells.

1 11. The method of claim 6, wherein the threshold is equal to the
2 predetermined number of memory cells having the first logic state.

1 12. The method of claim 1, wherein the threshold is read from a second
2 group of memory cells of the memory array.

1 13. The method of claim 1, wherein the read voltage comprises a plurality
2 of constant voltages each having a different value over a duration.

1 14. A method, comprising:
2 receiving, at a controller, a first set of bits of an input vector from a host
3 device;

4 allocating a block of memory to store the first set of bits of the input vector
5 and a second set of bits based at least in part on a total number bits of the first set of bits;
6 generating the second set of bits based at least in part on a number of bits of
7 the first set of bits having a first logic state; and
8 writing the first set of bits and the second set of bits at the block of memory.

1 15. The method of claim 14, wherein:
2 the second set of bits comprises multiple couples of bits representative of the
3 number of bits of the first set of bits having the first logic state.

1 16. The method of claim 14, wherein generating the second set of bits
2 comprises:
3 determining the number of bits of the first set of bits having the first logic
4 state; and
5 generating a set of bit values corresponding to the determined number of bits.

1 17. A method, comprising:
2 initializing a first counter and a second counter in a controller coupled with a
3 memory array that comprises a first portion of memory cells and a second portion of memory
4 cells;
5 activating a first subset of the first portion of memory cells by applying a first
6 read voltage to the memory array and a second subset of the second portion of memory cells
7 by applying a second read voltage to the memory array;
8 updating the first counter to a first value based at least in part on activating the
9 first subset of memory cells and the second counter to a second value based at least in part on
10 activating the second subset of memory cells; and
11 reading one or more memory cells of the first portion of memory cells based at
12 least in part on updating the first counter and the second counter.

1 18. The method of claim 17, further comprising:
2 comparing the second value of the updated second counter to a threshold
3 stored at the controller, wherein reading one or more memory cells of the first portion of
4 memory cells is based at least in part on comparing the second value of the updated second
5 counter to the threshold.

1 19. The method of claim 18, wherein the comparing further comprises:

2 determining that the second value satisfies the threshold stored at the
3 controller;
4 stopping application of the second read voltage based at least in part on the
5 determination that the second value satisfies the threshold; and
6 identifying, from the second portion of memory cells, a total number of
7 memory cells of the first portion having a first logic state based at least in part on the
8 determination that the second value satisfies the threshold.

1 20. The method of claim 19, further comprising:
2 determining that the first value corresponds to the identified total number; and
3 stopping application of the first read voltage based at least in part on the
4 determination that the first value corresponds to the identified total number, wherein the one
5 or more memory cells of the first portion of memory cells are read after application of the
6 first read voltage has stopped.

1 21. The method of claim 19, further comprising:
2 determining that the first value does not correspond to the identified total
3 number; and
4 maintaining application of the first read voltage based at least in part on the
5 determination that the first value does not correspond to the identified total number.

1 22. The method of claim 18, wherein the comparing further comprises:
2 determining that the second value does not satisfy the threshold stored at the
3 controller; and
4 maintaining application of the second read voltage based at least in part on the
5 determination that the second value does not satisfy the threshold.

1 23. The method of claim 17, wherein the first read voltage and the second
2 read voltage are a same single read voltage.

1 24. The method of claim 17, wherein the first read voltage is configured to
2 have a time offset with respect to the second read voltage.

1 25. The method of claim 17, wherein the first read voltage is configured to
2 have a different rate of voltage change with respect to the second read voltage.

- 1 26. The method of claim 19, further comprising:
2 setting a flag in the controller based at least in part on identifying the total
3 number of memory cells of the first portion having the first logic state.
- 1 27. A method, comprising:
2 initializing a counter in a controller coupled with a memory array that
3 comprises a first portion of memory cells and a second portion of memory cells, wherein the
4 second portion of memory cells comprises a plurality of pairs of memory cells, each pair of
5 the plurality of pairs associated with a respective flag value;
6 activating a first subset of the first portion of memory cells by applying a first
7 read voltage to the memory array;
8 activating at least one cell of each pair of the plurality of pairs by applying a
9 second read voltage to the memory array;
10 setting an indicator in the controller based at least in part on activation of the
11 at least one cell; and
12 reading one or more memory cells of the first portion of memory cells based at
13 least in part on the indicator.
- 1 28. The method of claim 27, wherein setting the indicator comprises:
2 toggling the respective flag value of each pair of the plurality of pairs from a
3 first flag value to a second flag value based at least in part on activation of the at least one
4 cell.
- 1 29. The method of claim 27, further comprising:
2 determining, based at least in part on a set of values of the second portion of
3 memory cells after activation of the at least one cell, a total number of memory cells of the
4 first portion having a first logic state;
5 updating the counter to a first count value based at least in part on activation
6 of the first subset of memory cells; and
7 comparing the first count value to the determined total number, wherein one or
8 more memory cells of the first portion of memory cells are read based at least in part on the
9 comparison.