

Support ring for supporting a semiconductor wafer
composed of monocrystalline silicon during a thermal
treatment, method for the thermal treatment of such a
5 semiconductor wafer, and thermally treated
semiconductor wafer composed of monocrystalline silicon

The claimed invention resides in the field of the
thermal treatment of monocrystalline semiconductor
10 wafers composed of silicon. The thermal treatment is
generally carried out in a vertical furnace ("wafer
boat"). In such a furnace, a multiplicity of
semiconductor wafers are simultaneously heated to high
temperatures over a relatively long time period. In
15 this case, they bear on support rings in a manner
stacked one above another and spaced apart from one
another. Such a support ring ("susceptor ring")
generally consists of silicon carbide and has the task
of supporting the semiconductor wafer lying thereon
20 during the thermal treatment.

The aim of a thermal treatment is to provide a zone
("denuded zone") for electronically active structures
which extends from the surface into the interior of the
25 semiconductor wafer and is free of defects which could
disturb the function of electronic components. Such
defects are, in particular, accumulations of
precipitated oxygen, BMD ("bulk micro defects") and
defects which are formed by accumulations of vacancies
30 and are referred to, inter alia, as COP defects
("crystal originated particles"). As a result of the
thermal treatment, BMD-forming nuclei and COP defects
are resolved and the oxygen concentration in the zone
is decreased below the threshold necessary for BMD
35 formation.

The larger the size of COP defects, the longer the time needed to be able to resolve them by means of a thermal treatment of the semiconductor wafer. Therefore, it is expedient, as early as during the pulling of the single
5 crystal yielding the semiconductor wafers from a crucible, to implement measures which can give rise to COP defects having comparatively small dimensions. For this purpose, two measures are usually taken into consideration, which can also be combined. Firstly,
10 rapid cooling of the single crystal prevents vacancies from remaining mobile long enough to be able to agglomerate in comparatively large COP defects. Secondly, doping the single crystal with nitrogen has the effect that, during the cooling of the single
15 crystal, vacancies become supersaturated later and correspondingly less time is available for the formation of the vacancy accumulations.

At the temperatures in the range of 1050°C to 1300°C
20 which prevail during the thermal treatment, the crystal lattice of monocrystalline silicon is particularly sensitive to disturbances. Temperature gradients, relative movements of semiconductor wafer and support ring owing to different coefficients of thermal
25 expansion of silicon and silicon carbide and the intrinsic weight of the semiconductor wafer pressing onto the support ring can initiate slip in the crystal lattice or cause scratches.

30 Measurements of laser scattered light or measurements of the depolarization of laser light are usually used for the detection of stresses and slip. The measurement method based on the latter option is known by the acronym SIRD, which stands for "Scanning Infrared
35 Depolarization". US 2004/0021097 A1 describes a measurement method employing SIRD which can be used to

detect defects on semiconductor wafers which are caused by the support ring.

DE 10 2005 013 831 A1 discloses that both the
5 temperature during the thermal treatment and the
concentration of nitrogen in the semiconductor wafer
have a particular influence on the upper yield stress
(UYS). The UYS is a characteristic variable for the
resistance of the semiconductor material to the
10 formation of slip. Accordingly, the resistance
decreases significantly in the temperature range of
1000°C to 1350°C, likewise with a reduction of the
nitrogen concentration. In order to obtain thermally
treated semiconductor wafers composed of
15 monocrystalline silicon which exhibit no slip during an
SIRD measurement, the cited document recommends using
the upper yield stress measured at a temperature of
1200°C as a criterion for carrying out the thermal
treatment in a specific manner. Accordingly,
20 comparatively high heating rates in the temperature
range of above 900°C and/or comparatively high cooling
rates in the temperature range up to 900°C and the use
of a closed ring as support ring during the thermal
treatment are suitable rather only for relatively
25 resistive semiconductor wafers.

JP 2003059851 A describes a support ring, comprising an
inner and an outer lateral surface, a horizontal
surface for the placement of the semiconductor wafer
30 and a rounded or beveled edge between the inner lateral
surface and the horizontal placement surface. The
distance R_y between the highest peak and the deepest
valley within a measurement section detecting the
roughness of the edge is not greater than 5 μm .

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EP 1 772 901 A2 contains the description of a two-part
support ring, the surface roughness of which expressed

in the form of the averaged roughness depth R_z is intended to be not more than 15 μm . A semiconductor wafer composed of silicon, which was heated on such a support ring at a temperature of 1200°C over a time period of 600 min, exhibited, after the thermal treatment, no slip detectable by means of laser scattered light or depolarization of laser light.

The inventors of the present invention have found, however, that semiconductor wafers composed of monocrystalline silicon, with the use of known support rings during a thermal treatment, are exposed to stresses which can adversely affect the nanotopography of the front side of the semiconductor wafer.

Therefore, embodiments of the present invention seek to present an improved support ring, to disclose a better method for the thermal treatment of a semiconductor wafer composed of monocrystalline silicon and to provide an improved thermally treated semiconductor wafer composed of monocrystalline silicon.

According to the first aspect of the invention, there is provided a support ring for supporting a semiconductor wafer comprising monocrystalline silicon during a thermal treatment of the semiconductor wafer, the support ring having an external diameter and an internal diameter, comprising a ring having an outer and an inner lateral surface and a curved surface extending from the outer to the inner lateral surface, the curved surface serving for placement of a semiconductor wafer, wherein the curved surface has a radius of curvature of not less than 6000 mm and not more than 9000 mm, if the curved surface is designed for placement of a semiconductor wafer having a diameter of 300 mm, or has a radius of curvature of not less than 9000 mm and not more than 14,000 mm, if the curved surface is designed for the placement of a semiconductor wafer having a diameter of 450 mm, and wherein the curved surface has a material proportion $R_{mr}(t)$ of not less than 85% at a material depth t of 2 μm .

According to the second aspect of the invention, there is provided a method for the thermal treatment of a semiconductor wafer of monocrystalline silicon, comprising placing the semiconductor wafer on a support ring having an external diameter and an internal diameter, comprising a ring having an outer and

an inner lateral surface and a curved surface extending from the outer to the inner lateral surface, the curved surface serving for placement of a semiconductor wafer, wherein the curved surface has a radius of curvature of not less than 6000 mm and not more than 9000 mm, if the curved surface is designed for placement of a semiconductor wafer having a diameter of 300 mm, or has a radius of curvature of not less than 9000 mm and not more than 14,000 mm, if the curved surface is designed for the placement of a semiconductor wafer having a diameter of 450 mm, and wherein the curved surface has a material proportion $R_{mr}(t)$ of not less than 85% at a material depth t of 2 μm and heating the semiconductor wafer positioned on the support ring to a temperature of not less than 1050° C. and not more than 1300° C. for a time period of not less than 30 min and not more than 180 min.

According to the third aspect of the invention, there is provided an uncoated semiconductor wafer having a front side and a back side, composed of monocrystalline silicon having a denuded zone on at least one surface thereof, formed by a heat treatment, the silicon wafer having a nitrogen concentration of not less than 1×10^{13} atoms/cm³ and not more than 8×10^{14} atoms/cm³ and having a nanotopography of the front side of the semiconductor wafer of less than 20 nm relative to a circular measurement window having a diameter of 4 mm, and less than 40 nm relative to a circular measurement window having a diameter of 20 mm.

In accordance with a first embodiment of the invention, there is provided a support ring for supporting a semiconductor wafer composed of monocrystalline silicon during a thermal treatment of the semiconductor wafer, comprising an outer and an inner lateral surface and a curved surface extending from the outer to the inner lateral surface and serving for the placement of the semiconductor wafer with a radius of curvature of not less than 6000 mm and not more than 9000 mm, if the surface is designed for the placement of a semiconductor wafer having a diameter of 300 mm, or with a radius of curvature of not less than 9000 mm and not more than 14 000 mm, if the surface is designed for the placement of a semiconductor wafer having a diameter of 450 mm.

A semiconductor wafer composed of silicon placed on a support ring sags on account of its own weight because the support by the support ring is absent in the
5 central region.

The inventors of the present invention have found that it is unfavorable to use a support ring having a horizontal surface for the placement of a semiconductor
10 wafer, even if the inner edge between the horizontal placement surface and the inner lateral surface is rounded. The sagging of the semiconductor wafer leads, in particular in the region of the inner edge of the support ring, to a stress field that regularly brings
15 about slip. The thermal treatment of the semiconductor wafer simultaneously also effects partial smoothing of the unevennesses brought about by slip. Therefore, such slip often cannot be detected. However, it leads to an impairment of the nanotopography of the semiconductor
20 wafer and, if appropriate, to defocusing problems during the exposure of the front side of the semiconductor wafer in the course of the fabrication of electronic components. The nanotopography describes flatness deviations in a measurement range with a
25 spatial wavelength of 0.2 to 20 mm. An expedient measurement method for determining the nanotopography is optical interferometry. Measuring devices based thereon are commercially available. In the context of the invention, the nanotopography of the front side of
30 the semiconductor wafer is measured in order to characterize the flatness of the front side and in order to be able to estimate the effect of the thermal treatment on the flatness. The front side of the semiconductor wafer is the side provided for the
35 integration of electronic structures.

Figure 1 shows, in a sectional illustration, a support ring associated with the prior art. This support ring is characterized by a horizontal surface 1 for the placement of a semiconductor wafer.

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Figure 2 shows a support ring embodied according to the invention. This support ring is a closed ring and is distinguished by a concavely curved surface 4 for the placement of the semiconductor wafer. The concavely curved placement surface extends from the outer lateral surface 2 to the inner lateral surface 3 and therefore does not have a horizontally situated portion. It has a cross section forming concavely from the outer to the inner lateral surface. The radius of curvature of the placement surface 4 is not less than 6000 mm and not more than 9000 mm, if the placement surface is designed for the placement of a semiconductor wafer having a diameter of 300 mm, or not less than 9000 mm and not more than 14 000 mm, if the placement surface is designed for the placement of a semiconductor wafer having a diameter of 450 mm, and preferably corresponds to the radius of the sagging of the semiconductor wafer. As a result, the stress field which acts on the semiconductor wafer during the thermal treatment in the region of the inner edge between placement surface and inner lateral surface of the support ring is significantly lower than with the use of a support ring having a completely or partly horizontal placement surface. The use of a support ring embodied according to the invention affords the advantage of a lower density of defects brought about by stresses, which is also manifested in an improved nanotopography of the front side of the thermally treated semiconductor wafer.

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The external diameter of the support ring is preferably equal to the diameter of the semiconductor wafer placed

on the curved surface for the purpose of the thermal treatment, or greater by up to not more than 2 mm. The internal diameter of the support ring is preferably not less than 60 mm and not more than 100 mm smaller than the external diameter.

The support ring preferably consists of silicon carbide or is coated with silicon carbide.

10 It is furthermore advantageous if the curved surface for the placement of the semiconductor wafer satisfies specific roughness and flatness criteria.

The averaged roughness depth R_z should preferably be not less than 3 μm and not more than 5 μm and the maximum individual roughness depth R_{max} should preferably be not more than 5 μm . The averaged roughness depth R_z corresponds to the arithmetic mean of the individual roughness depths (the difference between highest peak and deepest valley relative to an individual measurement section). The individual roughness depths are determined with the aid of a roughness-mapping profile over a total measurement section subdivided into five individual measurement sections. A roughness characterized by an averaged roughness depth R_z of less than 3 μm is less favorable because it promotes the slipping of the semiconductor wafer on the support ring. A roughness characterized by an averaged roughness depth R_z of over 5 μm entails the risk of local material points adversely affecting the nanotopography of the thermally treated semiconductor wafers.

Furthermore, the material proportion $R_{\text{mr}}(t)$ of the curved placement surface at a cutting depth t of 2 μm should not be less than 85%. The characteristic value is defined in DIN EN ISO 4287 and denotes the

percentage proportion (bearing proportion) made up by the material-comprising sections in the total measurement section at the specified cutting depth. The latter is calculated from the highest peak of the profile. An Rmr (2 μ m) of less than 85%, in particular of less than 50%, is not favorable because the small material proportion is an indicator of the presence of local material points and correspondingly disadvantageously affects the nanotopography of the thermally treated semiconductor wafers. In the case of an Rmr (2 μ m) of not less than 85%, material peaks are wider and rounded rather than tapering to a point.

Ultimately, the support ring should be shaped as ideally as possible. In order that the nanotopography of the front side of thermally treated semiconductor wafers reliably remains in the range striven for, the placement surface should deviate by preferably not more than 30 μ m from a geometrically ideally shaped surface, the radius of curvature of which lies in the stated range. The surface form in accordance with the DIN ISO 1101 standard should therefore preferably be not more than 0.03 mm. Accordingly, the placement surface has to lie between two enveloping surfaces, the spacing of which is determined by spheres having a diameter of 30 μ m, wherein the midpoint of the spheres lies on the geometrically ideal surface.

Upon complying with the stated criteria, thermally treated semiconductor wafers composed of monocrystalline silicon have the comparatively best nanotopography of the front side.

In accordance with a second embodiment of the invention, there is provided a method for the thermal treatment of a semiconductor wafer composed of monocrystalline silicon, comprising the

- placement of the semiconductor wafer on a support ring, which has an outer and an inner lateral surface and a curved surface extending from the outer to the inner lateral surface and serving for the placement of the semiconductor wafer, and the heating of the semiconductor wafer placed on the support ring to a temperature of not less than 1050°C and not more than 1300°C for a time period of not less than 30 min and not more than 180 min.
- 10 If the lower temperature limit is not reached or if the time period of the thermal treatment is shorter than 30 min, no "denuded zone" arises or a "denuded zone" arises which does not extend deeply enough into the interior of the semiconductor wafer. If the upper temperature limit is exceeded or if the time period of the thermal treatment is longer than 180 min, the method becomes uneconomic.
- 20 The method is also distinguished by the fact that criteria such as the upper yield stress of the semiconductor wafer material or the heating rate in the temperature range above 900°C or the cooling rate in the temperature range up to 900°C do not have to be taken particularly into account. Thus, even semiconductor wafers having a comparatively low concentration of nitrogen can be thermally treated without the formation of slip.
- 30 It is nevertheless preferred to set the heating rate in the temperature range of above 900°C and the cooling rate in the temperature range up to 900°C to values in the range of 1°C/min to 10°C/min.
- 35 The thermal treatment is preferably carried out in an atmosphere that does not react chemically with silicon under the prevailing conditions or in a reducing

atmosphere. Examples include a thermal treatment in argon or in a mixture of argon and hydrogen.

5 In accordance with a third embodiment of the invention, there is provided an uncoated semiconductor wafer composed of monocrystalline silicon having a "denuded zone", having a nitrogen concentration of not less than 1×10^{13} atoms/cm³ and not more than 8×10^{14} atoms/cm³ and having a nanotopography of less than 20 nm, relative to a circular measurement window having
10 a diameter of 4 mm, and of less than 40 nm, relative to a circular measurement window having a diameter of 20 mm.

The measurement of the nanotopography is effected in accordance with the SEMI standard M78.

15 If the nitrogen concentration is lower than the lower range limit, the semiconductor wafer stabilization based on the presence of nitrogen is too weak in its effect. If the nitrogen concentration exceeds the upper range limit, undesirable defects induced by nitrogen occur to an increased extent.

20 One method suitable for producing the semiconductor wafer is the method in accordance with the second embodiment of the invention.

The "denuded zone" is a zone which extends from the front side of the semiconductor wafer as far as a length of preferably not less than 8 μ m into the interior of the semiconductor wafer and
25 in which no COP defects and BMD can be detected.

The semiconductor wafer preferably has an oxygen concentration of not less than 4×10^{17} atoms/cm³ and not more than 7.5×10^{17} atoms/cm³ (new ASTM) and a

resistivity of 1 ohm cm to 80 ohm cm. The BMD density is preferably 5×10^8 to $2 \times 10^{10} \text{ cm}^{-3}$ outside the "denuded zone".

- 5 The diameter of the semiconductor wafer is preferably 300 mm or 450 mm.

The single crystal yielding the semiconductor wafer is pulled according to the Czochralski method from a melt
10 contained in a crucible, at a pulling rate at which vacancies are formed in excess in relation to silicon interstitials. The single crystal is cooled in the temperature range of 1150°C to 1000°C preferably at a high cooling rate in order to limit the size of COP
15 defects that form.

Example:

Semiconductor wafers composed of monocrystalline
20 silicon having a diameter of 300 mm were subjected to a thermal treatment in a vertical furnace of the type A412 from the manufacturer ASM. The semiconductor wafers were heated in the course of the thermal treatment to a temperature of 1200°C over a time period
25 of 120 min.

The semiconductor wafers were sliced from single crystals which had been pulled in the section of the single crystals that yields the semiconductor wafers at
30 an average pulling rate of 0.86 mm/min from a melt composed of silicon contained in a crucible and doped with nitrogen, according to the Czochralski method, and actively cooled. The cooling rate in the temperature range of 1150 to 1000°C was 2.5 K/min in the center and
35 3.2 K/min at the edge of the respective single crystal.

During the thermal treatment, the semiconductor wafers were situated on support rings composed of silicon carbide which were embodied in the manner illustrated in figure 2. The external diameter of the support rings was 1 nm greater than the diameter of the semiconductor wafers.

The roughness profile of the bearing surface was measured by means of a profiler.

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The averaged roughness depth R_z , in the case of the support rings used, was in the range of 3 μm to 5 μm and the largest measured individual roughness depth R_{max} was not more than 5 μm . Furthermore, the material proportion $R_{\text{mr}}(t)$ of the curved placement surface at a cutting depth t of 2 μm was not less than 85% in any of the support rings.

After a time period of 1000 process passes, not a single failure owing to the exceeding of the upper limit of the permissible nanotopography of the front side of the semiconductor wafer was observed.

The measurement of the nanotopography was carried out in accordance with the SEMI standard M78, with a "fixed quality area" (FQA) of 297 mm, the "key options" NT-CC, the "threshold area" $\times = 0.25\%$ and the "cut-off wavelength" $\lambda_c = 20 \text{ mm}$. The evaluation was effected in accordance with the "deviation metric".

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Under otherwise identical conditions, semiconductor wafers placed on a support ring embodied in accordance with the illustration in figure 1 were also thermally treated. In the case of these semiconductor wafers, failures were observed in significant numbers both after SIRD measurement and after measurement of the nanotopography.

Figures 3 and 4 show typical SIRD images of a failed semiconductor wafer and of a semiconductor wafer according to the invention. The recorded images were
5 created using a measuring device of the type SIRD A300P from the manufacturer PVA TePla. Local SIRD stresses as a reason for the failure of the semiconductor wafer are marked in figure 3. The position of the markings shows
10 that the stresses were brought about by the interaction of semiconductor wafer and inner edge of the support ring.

Figures 5 and 6 show typical nanotopography measurements of the front side of a failed
15 semiconductor wafer and of a semiconductor wafer according to the invention. The recorded images were created using a measuring device of the type WaferSight2 from the manufacturer KLA Tencor. An exceeding of the local nanotopography as a reason for
20 the failure of the semiconductor wafer is marked in figure 5. Its position in the region of the inner edge of the support ring used shows that the form of the support ring is responsible for the exceeding.

25 The semiconductor wafer illustrated in figure 5 had a nanotopography of 8.68 nm, relative to a measurement window having a diameter of 4 nm, and of 55.56 nm, relative to a measurement window having a diameter of 20 nm. In the case of the semiconductor wafer according
30 to the invention as illustrated in figure 6, the corresponding measured values were 4.48 nm, and 10.01 nm, respectively.

Claims

1. A support ring for supporting a semiconductor wafer comprising monocrystalline silicon during a thermal treatment of the semiconductor wafer, the support ring having an external diameter and an internal diameter, comprising
5 a ring having an outer and an inner lateral surface and a curved surface extending from the outer to the inner lateral surface, the curved surface serving for placement of a semiconductor wafer, wherein the curved surface has a radius of curvature of not less than 6000 mm and not more than 9000 mm, if the curved surface is designed for placement of a semiconductor wafer having a diameter of 300 mm, or has
10 a radius of curvature of not less than 9000 mm and not more than 14,000 mm, if the curved surface is designed for the placement of a semiconductor wafer having a diameter of 450 mm, and wherein the curved surface has a material proportion Rmr(t) of not less than 85% at a material depth t of 2 μ m.
2. The support ring of claim 1, wherein the curved surface has an average roughness depth Rz of not less
15 than 3 μ m and not more than 5 μ m and a maximum individual roughness depth Rmax of not more than 5 μ m.
3. The support ring of claim 1, wherein the surface form tolerance of the curved surface is not more than 0.03 mm.
20
4. The support ring of claim 1, wherein the external diameter of the support ring is equal to the diameter of a semiconductor wafer to be treated or is greater by not more than 2 mm, and the internal diameter of the support ring is not less than 60 mm and not more than 100 mm smaller than the external diameter.
- 25 5. The support ring of claim 1, wherein the support ring is constructed from silicon carbide or is coated with silicon carbide.
6. A method for the thermal treatment of a semiconductor wafer of monocrystalline silicon, comprising placing the semiconductor wafer on a support ring having an external diameter and an internal diameter,
30 comprising
a ring having an outer and an inner lateral surface and a curved surface extending from the outer to the inner lateral surface, the curved surface serving for placement of a semiconductor wafer, wherein the curved surface has a radius of curvature of not less than 6000 mm and not more than 9000 mm, if the curved surface is designed for placement of a semiconductor wafer having a diameter of 300 mm, or has
35 a radius of curvature of not less than 9000 mm and not more than 14,000 mm, if the curved surface is designed for the placement of a semiconductor wafer having a diameter of 450 mm, and wherein the curved surface has a material proportion Rmr(t) of not less than 85% at a material depth t of 2 μ m and heating the semiconductor wafer positioned on the support ring to a temperature of not less than 1050° C. and not more than 1300° C. for a time period of not less than 30 min and not more than 180 min.

7. An uncoated semiconductor wafer having a front side and a back side, composed of monocrystalline silicon having a denuded zone on at least one surface thereof, formed by a heat treatment, the silicon wafer having a nitrogen concentration of not less than 1×10^{13} atoms/cm³ and not more than 8×10^{14} atoms/cm³ and having a nanotopography of the front side of the semiconductor wafer of less than 20 nm relative to a circular measurement window having a diameter of 4 mm, and less than 40 nm relative to a circular measurement window having a diameter of 20 mm.
- 5

Abstract

- Support ring for supporting a semiconductor wafer
5 composed of monocrystalline silicon during a thermal
treatment, method for the thermal treatment of such a
semiconductor wafer, and thermally treated
semiconductor wafer composed of monocrystalline silicon
- 10 A support ring for supporting a semiconductor wafer
composed of monocrystalline silicon during a thermal
treatment of the semiconductor wafer, comprising an
outer and an inner lateral surface and a curved surface
15 extending from the outer to the inner lateral surface
and serving for the placement of the semiconductor
wafer with a radius of curvature of not less than
6000 mm and not more than 9000 mm, if the surface is
designed for the placement of a semiconductor wafer
20 having a diameter of 300 mm, or with a radius of
curvature of not less than 9000 mm and not more than
14 000 mm, if the surface is designed for the placement
of a semiconductor wafer having a diameter of 450 mm. A
method for the thermal treatment of such a
semiconductor wafer, and a thermally treated
25 semiconductor wafer composed of monocrystalline
silicon.

Fig. 2