METHOD AND APPARATUS FOR PROCESSING SMALL CORE CELL SIZE SRAM STRUCTURES

ABSTRACT OF THE DISCLOSURE

A method and apparatus for processing small core cell size SRAM structures is disclosed. A high density SRAM core cell fabrication process includes: (1) performing an isolation process such as shallow trench isolation or LOCOS isolation; (2) forming a gate dielectric and depositing a gate material layer; (3) pre-doping selected gate layer regions; (4) depositing a dielectric cap layer; (5) selectively etching the dielectric cap layer to define device regions for salicide processing; (6) selectively etching the dielectric cap layer, the poly-silicon gate layer, and the gate dielectric layer to form gate electrodes; (7) depositing and selectively etching dielectric spacers; (8) depositing metal and annealing to form a silicide layer on all exposed silicon, by a salicide process; (9) etching away unreacted metal; and (10) depositing dielectric, planarizing, and completing standard CMOS processing steps. This process forms a high density CMOS SRAM core cell that includes PMOS and NMOS transistor devices, and does not require horizontal spacing between most gate electrodes and source/drain contact regions. This process also maintains low RC time delay of the core cell by selective silicidization of gate regions that connect to low resistivity peripheral circuits and transport current over long distances.

FIGURE 3