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Semiconductor device having an improved lead arrangement and method for manufacturing the same

This invention concerns a lead frame, a semiconductor device manufactured by using the lead frame, and a method for manufacturing the semiconductor device.

Recently, the demand for high integration of semiconductor devices has increased. On the other hand, there is also a demand for reduction of the external dimensions of the semiconductor device after sealing. Since the semiconductor chip size is becoming larger to meet the demand for high integration, the reduction of the external dimensions is very difficult. Many efforts have been made to reduce the external dimensions.

FIGS.1A to 1E show a conventional lead frame and a semiconductor device produced by using the lead frame, shown in Japanese laid open Patent (Tokkai Sho) No:52-127756. In the prior art, two metalic frame bodies 10 and 20 are used. The first metalic frame body 10 includes a die pad portion 13 and tie bars 12 connecting the die pad portion 13 to a joining band 11. FIG.1C is a cross sectional view along the line A-A' of FIG.1B. The second metalic frame body 20 has projecting portions 23 and a plurality of leads 25 extending from a lead connecting portion 24 to the central portion. A dam bar portion 22 supports the leads 25 (FIG.1B,

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FIG.1C). A semiconductor chip 15 is mounted on the die pad portion 13. (FIG.1D)

The die pad portion 13 is separated from the joining band 11 by cutting along the line B-B'.

The die pad portion 13 having the semiconductor chip 15 is welded to the projecting portion 23, and is fixed to the second frame body 20. (FIG.1E)

Bonding pads (not shown) on the semiconductor chip 15 are electrically connected to the inner lead portions of the leads 25 by bonding wires (not shown).

Since the inner lead portions of the leads 25 overlaps the semiconductor chip 15, it is possible to reduce the external dimensions of the semiconductor device comparing with devices wherein the die pad portion and the leads are produced from a single frame body.

However, in the prior art, the die pad portion 13 is separated from the joining band after the semiconductor chip is mounted thereon. Thus, there is a problem of dust adhering to the semiconductor chip during the separation process. Furthermore, there is a problem in handling the frame bodies due to the projecting portions 23, since the projecting portion 23 serves as a hook when the frame bodies are piled up during the manufacturing process.

Various aspects of the present invention will now be described by way of example only and without limiting the scope of the invention.

Therefore, an object of the present invention is to provide an improved frame body which is free from the dust problem and is easy to handle during the fabrication of the semiconductor devices.

Another object of the present invention is to provide a

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semiconductor device having an improved lead arrangement using the improved frame body.

A further object of the present invention is to provide a method for manufacturing the semiconductor device disclosed herein.

To achieve these objects, this invention provides a frame body for manufacturing a semiconductor device including a semiconductor chip, comprising: first frame means including; a die pad portion having a main surface for supporting the semiconductor chip; a first frame portion having a first surface, surrounding the die pad portion; connecting means for connecting the die pad portion to a predetermined portion of the first frame portion so as to produce an offset between the main surface and the first surface; and second frame means to be combined with the first frame means, including; a second frame portion; a central portion surrounded by the second frame portion; a plurality of lead portions extending from the second frame portion to the central portion so as to overlap the semiconductor chip when the first and the second frame bodies are combined.

Furthermore, this invention provides a semiconductor device comprising: a semiconductor chip having a plurality of bonding pads formed on a main surface thereof; semiconductor chip supporting means, including; a die pad portion having a first surface for supporting the semiconductor chip, a die pad supporting portion having a second surface, a tie bar portion for producing a predetermined offset between the second surface of the die pad supporting portion and the first surface of the die pad portion; a plurality of inner leads, each having third and

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fourth surfaces, the fourth surface being coincident with a plane formed by the second surface of the die pad supporting portion and overlapping the semiconductor chip on the main surface; and a plurality of bonding wires for connecting the third surface of the inner lead to corresponding bonding pad.

Moreover, this invention provides a process for manufacturing a semiconductor device, comprising the steps of: preparing a first frame body, including; a die pad portion for supporting a semiconductor chip; a first frame portion surrounding the die pad portion; and connecting means for connecting the die pad portion to the first frame portion; preparing a second frame body, including; a second frame portion; a central portion surrounded by the second frame portion; a plurality of lead portions extending from the second frame portion to the central portion; mounting a semiconductor chip having a plurality of bonding pads on a main surface thereof on the die pad portion of the first frame body; welding the first and the second frame bodies; connecting the bonding pads on the semiconductor chip to the lead portions of the second lead frame body; and separating the lead portions and the die pad portion from the first and second frame bodies.

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate an embodiment of the invention, and, together with the description, serve to explain the principles of the invention. Referring now to the drawings, like reference

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characters designate like or corresponding parts throughout the several views. Of the drawings:

FIGS.1A to 1E show a conventional frame body.

FIG.2A is a plan view of a semiconductor device according to the present invention, and FIGS.2B and 2C are cross sectional views along the lines A-A' and B-B' in FIG.2A, respectively.

FIG.3 is a cross sectional view showing another embodiment according to the present invention.

FIG.4 is a cross sectional view showing yet another embodiment according to the present invention.

FIG.5A is a plan view showing a still further embodiment according to the present invention, and FIG.5B is a cross secional view along the line A-A' in FIG.5A.

FIG.6A is a plan view of another embodiment according to the present invention, and FIG.6B is a cross secional view along the line B-B' in FIG.6A.

FIGS.7A to 7J are diagrams illustrating a method of manufacturing a semiconductor device according to the present invention.

FIGS.8A to 8D are diagrams for explaining a joint portion between a first frame body and a second frame body.

FIG.9 is a plan view illustrating a preferred arrangement of the bonding pads formed on a semiconductor chip and the inner leads.

FIGS.10A and 10B are diagrams illustrating a problem of contact between the inner leads and the bonding wires.

FIG.11 is a diagram also used to illustrate a contact problem between the inner leads and the bonding wires.

FIGS.12A and 12B are drawings for explaining a preferred

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shape of the inner leads.

FIG.13 illustrates an embodiment according to the present invention, wherein notchs are formed in the frame body.

FIG.14 illustrates yet another embodiment according to the present invention, wherein notchs are formed in the frame body.

FIGS.15A and 15B are drawings for explaining a problem when the tie bar is relatively short.

FIGS.16A and 16B are drawings for explaining the case where the tie bar is relatively long.

FIGS.17 and 18 are cross sectional views for explaining the reason why the dimensions of first and second frame bodies are different in the embodiment of FIG.13.

Referring now to the drawings, the present invention will be explained.

FIG.2A is a plan view of a semiconductor device according to the present invention, with plastic housing 71 removed for ease of explanation. FIGS.2B and 2C are cross sectional views along the lines A-A' and B-B' in FIG.2A, respectively. In the semiconductor device, a semiconductor chip 50 is mounted on a die pad portion 33 and is fixed thereon by a conductive glue (not shown). The die pad portion 33 is formed by depressing and deforming a tie bar 32. A connecting portion 32b of the tie bar 32 produces a predetermined offset h between the surfaces of the die pad portion 33 and a die pad supporting portion 32a. The offset h is established to be equal or greater than the thickness of the semiconductor chip 50.

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A plurality of inner leads 42a are extended inwardly so as to overlap the semiconductor chip 50. In the fabrication of the semiconductor device according to the present invention, two separate frame bodies are used for the inner leads 42a and the die pad 33, respectively. Thus, the lower surface of the inner leads 42a is coincident with the upper surface of the die pad supporting portion 32a. The details of this construction will be provided in the explanation of the method for manufacturing the semiconductor device, given later.

The head portion of the respective inner lead 42a and the corresponding bonding pad 54 formed on the periphery of the semiconductor chip 50 are electrically connected by a bonding wire 51. The device is molded with a plastic resin to form a plastic housing 71.

In the semiconductor device, the relationship between the width N of the plastic housing 71 and the width C of the semiconductor chip 50 is expressed as follows.

$$C < N - \alpha \quad \cdots (1)$$

wherein the α is a margin. Since, the inner leads 42a overlap the semiconductor chip 50, the width C can be made relatively large when compared to a well known conventional device where the inner leads and the die pad are formed from a single frame body.

Furthermore, the distance R from the edge of the plastic housing 71 to the bonding position X of the inner lead 42a can be expressed as follows.

$$R < N - \beta \quad \cdots (2)$$

wherein the β is a margin.

As apparent from the equation (2), the distance R is not

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influenced by the semiconductor chip width C. Thus, it is possible to make the length of the bonding wire longer. Therefore, the path of moisture from the outside to the wire bonding portion becomes longer, and the invasion of moisture can be prevented. Thus, the reliability against moisture domage is increased.

FIG.3 is a cross sectional view of another embodiment according to the present invention. In this embodiment, an insulating tape 57 is formed between the inner leads 42a and the semiconductor chip 50. The insulating tape 57 is made of ,e.g., polyimide, and is pasted on the inner leads 42a. In this embodiment, the bonding process between the inner leads 42a and the bonding pads 54 can be performed in safety, since the insulating tape 57 absorbs the stress caused by the bonding when the bonding wire 51 is bonded to the inner leads 42a. Thus, the passivation layer (not shown) on the semiconductor chip can be protected from problems, such as cracking.

FIG.4 is a cross sectional view of a further embodiment according to the present invention. In this embodiment, an insulating buffer coating 58 is formed on the semiconductor chip 50. The coating 58 is made of insulating material, such as ,e.g., polyimide or polyurethane. The coating is formed by a spin coating on the semiconductor chip having a passivation layer thereon and an etching to expose the bonding pads 54 formed on the semiconductor chip 50, for example. In this embodiment, the coating 58 absorbs the stress on the semiconductor chip when the inner leads 42a contact the semiconductor chip 50 during the wire bonding. Thus, the passivation layer on the semiconductor chip can be

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protected from cracking.

FIGS.5A to 6B are drawings showing examples of patterns of the insulating tape 57. In FIGS.5A and 5B, the insulating tape 57 is formed selectively only on the edge portion serving as a bonding area of the inner leads 42a.

On the other hand, in FIGS.6A and 6B, the insulating tape 57 is relatively wide, and is formed to support all inner leads 42a. Thus, the stress on the semiconductor chip 50 during the bonding process can be reduced, and the wire bonding can be performed safety.

Next, the manufacturing process used to make a semiconductor device having an improved frame body will be explained referring FIGS.7A to 7J.

At first, a first frame body 30 is prepared. The first frame body 30 includes a joining bar 31, supporting bar 36 extending perpendicular from the joining bar 31, and a die pad portion 33 connected to the joining bar 31 by a tie bar 32. The die pad portion 33 is depressed downwardly by at least a semiconductor chip height. The joining bar 31 and the supporting bar 36 formes a closed loop to surround the die pad portion 33. Furthermore, the joining bar 31 is plated with tin 34 at selective locations. It is preferable to form one tin plated portion 34 on each side of the frame body which surrounds the die pad portion 33. The diameter of the tin plated portion is about 3 to 5 mm. The first frame body 30 further includes a plurality of indexing holes 35. (FIG.7A)

Next, semiconductor chips 50 are mounted on the corresponding die pad portions 33.(FIG.7B)

Then, a second frame body 40 is prepared. The second

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frame body 40 includes joining bar 41 and a plurality of leads 42. The leads 42 are supported by dam bar 43, and are extending inwardly from a lead connecting portion 46. The second frame body 40 also has tin plated portions 44 corresponding to the tin plated portions 34 of the first frame body 30 and indexing holes 45 corresponding to the indexing holes 35 of the first frame body 30. (FIG.7C)

Next, the second frame body 40 is put on the first frame body 30 with indexing holes 35 and 45 aligned. Then, a resistance welding is performed at the positions where the tin is plated. (FIG.7D)

In the case where a calking is used for joining of the first and the second frame bodies, the frame bodies are easily deformed. On the other hand, such deformation can be prevented using the above described welding technique. Generally, copper materials are used for the frame body rather than 42 alloy (Fe-Ni(42 %)) for easy processability. However, such copper materials have a good electric conductivity and a low thermal resistance. Thus, the heat generated during the welding is small and the heat is easily dissipated. When a large current is used for the welding to get enough heat, there is a problem of the welding electrode sticking to the frame body.

On the other hand, when the tin is used, it is not necessary to rise the welding temperature so high, since the tin has relatively low melting point. It is preferable to choose the sum of the thickness of the tin of the first and the second frame bodies about 3 to 5 μm. Besides the tin, it is possible to use a material of a low melting point (e.g., 300 ℃), a low electric conductivity, a low thermal

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conductivity and easily forming an alloy with the frame body, such as tin based alloy, e.g., solder (Pb-Sn), Au-Sn.

In this case, it is possible to sandwich a sheet material having the above mentioned characteristic between the first and the second frame bodies, instead of the plating.

Furthermore, it is possible to plate only one of the frame bodies, and also to plate the whole surface of the frame body.

Next, the wire bonding process is performed by connecting the bonding pads on the semiconductor chip 50 and the inner leads 42a by bonding wires 51. (FIG.7E)

FIGS.7F and 7G show the process of wire bonding. A conductive glue52 for fixing the semiconductor chip 50 to the die pad 33 is provided. The die pad 33 is put on a heater block 61. (FIG.7F) Since the inner leads42a are made from the first frame body, namely upper side frame body 40, there is a slight gap between the surface of the heater block 61 and the inner leads 42a. Thus, to perform the wire bonding process safety, the inner leads 42a are fixed to the surface of the heater block 61 by a forcing member 62. After the wire bonding, the forcing member 62 is taken away. The inner leads 42a return to their original position due to the elasticity thereof. Therefore, a gap is formed between the surface of the semicoductor chip 50 and the inner leads 42a.

Then, a molding process is performed using, e.g., a transfer mold method, to achieve a plastic housing 71. (FIG.7H)

Next, a plating of the outer leads 42b with solder, a removal of dam bar 43 and a cutting of the leads from the lead connecting portion are performed. (FIG.7I)

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Then, the outer leads 42b are bent to obtain a final product. FIG.7J)

FIGS.8A to 8D are drawings showing an example of the shape of the tin plated joint portion of the first frame body 30 and the second frame body 40. To simplify the explanation, a joint portion formed in the supporting bar 36 of the first frame body 30 and the lead connecting portion 46 of the second frame body 40 are illustrated as an example. As shown in FIG.8B, the supporting bar 36 of the first frame body 30 has an opening 38 for forming a lateral bar portion 37. The lead connecting portion 46 of the second frame body 40 has an opening 48 for forming a vertical bar portion 47. Thus, when the first and the second frame bodies are joined, the bar portions overlap in cross shape and contact at a relatively small area. Therefore, the heat during the welding may be concentrated at a small area, and the welding can be performed effectively.

It should be noted that in this invention, the first frame body having the semiconductor chip thereon is combined with the second frame body. Namely, there is no cutting process of the tie bar before the molding. Thus, the dust problem due to the cutting, which occured in the prior art, can be prevented.

FIG.9 is a plan view illustrating the relationship between the bonding pads 54 formed on the semiconductor chip 50 and the inner leads 42a. As shown in the drawing, each inner lead 42a extends inwardly through the space between the adjacent bonding pads 54. Each head portion of the respective inner lead 42a is bent towards the bonding pad to be connected electrically therewith.

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FIGS.10A, 10B and 11 are enlarged drawings for explaining why it is preferable to bend the inner leads 42a. In the case where the inner lead 42a is straight, there is a crossing D of the inner lead 42a and the bonding wire 51, as shown in FIG.10A. Thus, in the case where the bonding wire is not long enough, there is a risk of contact between the inner lead 42a and the bonding wire 51 during the wire bonding process between the bonding pads 54 and the head portion 42c of the inner leads 42a, as shown in FIG.11. As previously explained, since the inner leads go back to the original position after the wire bonding process, the bonding wire will be pulled by the inner lead 42a, and is sometimes will be broken due to the pull strength. Therefore, it is preferable to bend the lead 42a at a predetermined portion 42d to avoid the contact.

FIGS.12A and 12B are drawings for explaining the preferred shape of the inner leads. In FIG.12A, the inner lead is angular. On the other hand, the inner lead in FIG.12B is rounded. If the inner leads contact the semiconductor chip during the wire bonding process, a stress will be applied to the semiconductor chip. If the inner leads are rounded, the stress is disperted and the risk of cracks in the passivation layer on the semiconductor chip can be lowered. Thus, it is preferable to round the corners of the inner leads.

FIG.13 is a plan view of another embodiment according to the present invention. In this embodiment, the second frame body 40A having a plurality of leads 42 has a notch 49 to increase the length of the tie bar 32. Furthermore, the inner dimensions of the first frame body 30 and the second

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frame body 40A are different. Namely, the first frame body 30 has wider inner dimension than the second frame body 40A by d.

In FIG.14, the joining bar 31 of the first frame body 30A has a notch 39 to increase the length of the the tie bar 32. The second frame body 40A also includes a notch 49 corresponding to the notch of the first frame body 30. Thus, the tie bar may be lengthened.

FIGS.15A to 16B are drawings for explaining why it is useful for the tie bar to be made longer. When the tie bar 32 is short, i.e., n1 as shown in FIGS.15A and 15B, it is hard to deform the tie bar 32 by pressing the inner lead 32 with the forcing member 42 during the wire bonding process. Thus, in the case where the height d1 from the lower surface of the die pad 33 to the lower surface of the joining bar 31 is higher than the height h1 of the wall of the heater block 61, the frame bodies are not well fixed to the heater block 61 and the forcing member 62. Therefore, the wire bonding may be performed with a gap between the heater block 61 and the forcing member 62.

In FIG.16B, a notch 49 is formed at the joining bar 41 to increase the length of the tie bar 32 to n2. Furthermore, the forcing member 62A has an escape zone 62b, as shown in FIG.15A. When stress is applied to the frame bodies 30 and 40, the deformation of the tie bar is easily achieved, since the tie bar 32 is made longer and the distance between the edge 62c of the forcing member 62A and the deformed point 32c is made longer to ℓ2. Thus, the frame bodies are fixed tightly to the heater block 61 by the forcing member 62A, and the wire bonding is performed in a stabilized condition.

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The escape zone 62b allows the easy deformation of the tie bar 32.

FIGS.17 and 18 are diagrams for explaining the reason why the inside dimensions of the first and the second frame bodies are different in the embodiments of FIG.13 and FIG.14. FIG.17 and 18 correspond to cross sectional views along the line E-E' in FIG.13.

If the inside edges of the molding dies 81 and 82 are coincident with the edge of the first frame body 30 and 40, the mold resin (not shown) injected into the cavity 80 sometimes flows out through the slit between the two frame bodies to form a burr between the adjacent inner leads. Thus, additional steps, such as removing of the burr sticking to the leads, is required. Furthermore, the resin sometimes causes serious problem during the cutting and bending process, or lowers the relaibility of the wire connection.

To prevent the problem, the first frame body 30 is widened by d (corresponding to the length of the notch 49 in FIG.13), e.g.,0.2 mm, with respect to the second frame body 40 in the embodiment of FIG.13. With this arrangement, it is possible to fabricate a projecting portion 83a to hold the second frame body 40 with the upper molding die 81. The projecting portion 83a prevents the flow of the mold resin, and the reliability and the efficiency of the molding process can be increased.

The present invention has been described with respect to a specific embodiment. However, other embodiments based on the principles of the present invention should be obvious to those of ordinary skill in the art. Such embodiments are

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intended to be covered by the claims.

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CLAIMS

1. A frame body for manufacturing a semiconductor device including a semiconductor chip (50), characterized by comprising:

first frame means (30) including;

a die pad portion (33) having a main surface for supporting the semiconductor chip;

a first frame portion (31, 36) having a first surface, surrounding the die pad portion;

connecting means 32) for connecting the die pad portion to a predetermined portion of the first frame portion so as to produce an offset (h) between the main surface and the first surface; and

second frame means (40) to be combined with the first frame means, including;

a second frame portion (41, 46) ;

a central portion surrounded by the second frame portion;

a plurality of lead portions (42) extending from the second frame portion to the central portion so as to overlap the semiconductor chip when the first and the second frame bodies are combined.

2. The frame body according to claim 1, further comprising an insulating buffer layer (57) formed on the lead portions.

3. The frame body according to claim 1, wherein each frame portion is made of a metal having a predetermined melting point, and each frame portion has a specified metal layer (34, 44) which has lower melting point than the predetermined melting point.

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4. The frame body according to claim 3, wherein each frame portion is made of copper based material, and the specified metal layer is made of tin.

5. The frame body according to claim 1, wherein the second frame portion includes a first notch portion (49) at an area corresponding to the predetermined portion of the first frame portion.

6. The frame body according to claim 5, wherein the first frame portion includes a second notch portion (39) for increasing the length of the connecting means (32).

7. The frame body according to claim 1, wherein the first frame portion has a first predetermined inner dimension and the second frame portion has a second predetermined inner dimension, and the first predetermined inner dimension is wider than the second predetermined inner dimension by a predetermined amount (d).

8. A frame body used for fabricating a semiconductor device including a semicoductor chip (50) of predetermined thickness, characterized by comprising:

a frame portion (31, 36) forming a closed loop, having a pair of notches (39) for defining a predetermined position therebetween;

a die pad portion (33) for supporting the semiconductor chip thereon; and

tie bar means (32) for connecting the die pad portion to the predetermined portion of the frame portion.

9. The frame body according to claim 8, wherein the frame portion has a first surface, the die pad portion has a second surface for supporting the semiconductor chip, and the tie bar means produces an offset (h) between the first

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surface and the second surface equal or greater than the thickness of the semiconductor chip.

10. A semiconductor device characterized by comprising:

a semiconductor chip (50) having a plurality of bonding pads (54) formed on a main surface thereof;

semiconductor chip supporting means, including;

a die pad portion (33) having a first surface for supporting the semiconductor chip,

a die pad supporting portion (32a) having a second surface,

a tie bar portion (32b) for producing a predetermined offset (h) between the second surface of the die pad supporting portion and the first surface of the die pad portion;

a plurality of inner leads (42a), each having third and fourth surfaces, the fourth surface being coincident with a plane formed by the second surface of the die pad supporting portion and overlapping the semiconductor chip on the main surface; and

a plurality of bonding wires (51) for connecting the third surface of the inner lead to corresponding bonding pad.

11. The semiconductor device according to claim 10, further comprising an insulating buffer layer (57, 58) between the inner lead and the main surface of the semiconductor chip.

12. The semiconductor device according to claim 10, wherein the insulating buffer layer (57) is formed on the inner lead.

13. The semiconductor device according to claim 10,

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wherein the insulating buffer layer (58) is formed on the main surface of the semiconductor chip.

14. A process for manufacturing a semiconductor device, characaterized by comprising the steps of:

preparing a first frame body (30), including;

a die pad portion (33) for supporting a semiconductor chip;

a first frame portion (31, 36) surrounding the die pad portion; and

connecting means (32) for connecting the die pad portion to the first frame portion;

preparing a second frame body (40), including;

a second frame portion (41, 46);

a central portion surrounded by the second frame portion;

a plurality of lead portions (42) extending from the second frame portion to the central portion;

mounting a semiconductor chip (50) having a plurality of bonding pads (54) on a main surface thereof on the die pad portion of the first frame body;

welding the first and the second frame bodies;

connecting the bonding pads on the semiconductor chip to the lead portions of the second lead frame body; and

separating the lead portions and the die pad portion from the first and second frame bodies.

15. The process according to claim 14, wherein the welding process includes a resistance welding step.

16. The process according to claim 14, further including a step of forming an insulating buffer layer (57, 58)

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between the leads and the main surface of the semiconductor chip.

17. The process according to claim 14, wherein the step of preparing the first frame body includes a step of preparing a first frame means made of a first metal having a predetermined melting point and then plating the first frame means at predetermined locations with a material having a predetermined melting point lower than that of the first frame means.

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