CLAIMS

What is claimed is:

1. A memory device comprising:

a memory cell array comprising a plurality of memory cells;

a voltage generator configured to generate voltages used for a program operation and a verify operation for the memory cells; and

a control logic configured to perform a plurality of program loops while writing data to the memory cell array, such that first to N-th program loops comprising a program operation and a verify operation are performed and at least two program loops are performed in which the verify operation is skipped when a pass/fail determination of the program operation of the N-th program loop indicates a pass,

wherein N is an integer equal to or greater than 1, and

wherein the at least two program loops comprise an (N +1)-th program loop comprising a normal program operation on first memory cells among the memory cells, using a normal program voltage and a forcing program operation on second memory cells among the memory cells, using a forcing program voltage.

2. The memory device of claim 1, wherein the at least two program loops further comprise:

an (N+2)-th program loop comprising a forcing program operation on the first memory cells using the forcing program voltage.

3. The memory device of claim 2, wherein the control logic is configured to control the voltage generator to generate voltages used for the program operation and the verify operation in the first to N-th program loops, and

control the voltage generator to selectively generate voltages used in the program operation in the at least two program loops.

4. The memory device of claim 2 or claim 3, wherein the verify operation comprises an operation for determining coarse on cells and coarse off cells based on a first threshold voltage and an operation for determining fine on cells and fine off cells based on a second threshold voltage, and

the second threshold voltage is greater than the first threshold voltage.

5. The memory device of claim 4, wherein the memory cells having threshold voltage levels lower than the first threshold voltage correspond to the first memory cells, and the memory cells having threshold voltage levels greater than the first threshold voltage and less than the second threshold voltage correspond to the second memory cells.

6. The memory device of claim 4 or claim 5, wherein the pass/fail determination is performed by counting a number of the memory cells having threshold voltage levels lower than the first threshold voltage or the number of the memory cells having threshold voltage levels lower than the second threshold voltage.

7. The memory device of any one of claims 1 to 6, further comprising a page buffer connected to the memory cell array through a plurality of bit lines,

wherein the page buffer receives data read from the memory cell array through the bit lines in relation to the verify operation in the first to N-th program loops, and,

in the at least two program loops, an operation for providing data to the page buffer through the bit lines is skipped.

8. A method of operating a memory device, the method comprising:

performing an N-th program loop comprising a program operation and a verify operation, wherein N is an integer equal to or greater than 1;

determining whether the program operation is pass or fail by counting a number of memory cells of the memory device having threshold voltage levels lower than a predetermined threshold voltage;

when it is determined that the program operation is pass, performing a (N+1)-th program loop comprising a normal program operation using a normal program voltage for first memory cells among the memory cells, and a forcing program operation using a forcing program voltage for second memory cells among the memory cells; and

performing an (N+2)-th program loop comprising a forcing program operation using the forcing program voltage for the first memory cells,

wherein a verify operation is skipped in each of the (N+1)-th program loop and the (N+2)-th program loop.

9. The method of claim 8, wherein the verify operation performed in the N-th program loop comprises an operation for determining coarse on cells and coarse off cells based on a first threshold voltage and an operation for determining fine on cells and fine off cells based on a second threshold voltage, and

the second threshold voltage is greater than the first threshold voltage.

10. The method of claim 9, wherein the memory cells having threshold voltage levels lower than the first threshold voltage correspond to the first memory cells, and the memory cells having threshold voltage levels greater than the first threshold voltage and less than the second threshold voltage correspond to the second memory cells.

11. The method of claim 9 or claim 10, wherein the determination of whether the program operation is a pass or fail is performed by counting the number of the memory cells having threshold voltage levels lower than the first threshold voltage or the number of the memory cells having threshold voltage levels lower than the second threshold voltage.

12. The method of any one of claims 8 to 11, further comprising, in an operation for determining whether the program operation is a pass or fail, when it is determined that the program operation is fail,

performing at least one more program loop comprising a program operation and a verify operation before performing the (N+1)-th program loop.

13. The method of any one of claims 8 to 12, wherein each of the memory cells is connected to a word line and a bit line, and

a voltage level difference between the word line and the bit line of a memory cell on which the normal program operation is performed is greater than a voltage level difference between the word line and the bit line of a memory cell on which the forcing program operation is performed.

14. The method of claim 13, wherein, in the forcing program operation, a voltage of the same level as a voltage applied to the word line during the normal program operation is provided to the word line, and a voltage of a level greater than the voltage set to the bit line during the normal program operation is provided to the bit line.

15. The method of any one of claims 8 to 11, wherein an operation for determining whether the program operation is a pass or fail is performed in parallel with the normal program operation or the forcing program operation in the (N+1)-th program loop.

16. The method of any one of claims 8 to 15, wherein the memory device comprises a page buffer, as the verify operation is performed in the N-th program loop, data read from the memory cells is provided to the page buffer, and,

as the verify operation is skipped in each of the (N+1)-th program loop and the (N+2)-th program loop, data is not provided to the page buffer.

17. A method of operating a memory device, the method comprising:

performing first to N-th program loops each comprising a program operation and a verify operation for memory cells of the memory device, wherein N is an integer equal to or greater than 2;

determining whether the program operation is a pass or a fail based on a programming result in the N-th program loop; and,

when it is determined that the program operation is a pass, performing (N+1)-th to (N+A)-th program loops that do not comprise a verify operation for the memory cells, where A is an integer equal to or greater than 2,

wherein, in each of the (N+1)-th to (N+A)-th program loops, at least one of a normal program operation using a normal program voltage and a forcing program operation using a forcing program voltage is performed, and

wherein the (N+1)-th to (N+A)-th program loops comprise a program loop for performing the normal program operation on first memory cells among the memory cells, using the normal program voltage and the forcing program operation on second memory cells among the memory cells, using the forcing program voltage.

18. The method of claim 17, wherein the memory cells correspond to multilevel cells, each of the program loops comprises a program operation for programming to a plurality of threshold voltage states, and,

in each of the (N+1)-th to (N+A)-th program loops, a verify operation related to at least one of the threshold voltage states is skipped.

19. The method of claim 17 or claim 18, wherein, by the verify operation in the N-th program loop, the first memory cells having threshold voltage levels lower than a first threshold voltage and the second memory cells having threshold voltage levels greater than the first threshold voltage and less than a second threshold voltage are determined.

20. The method of claim 19, wherein the (N+1)-th to (N+A)-th program loops further comprise: a program loop for performing the forcing program operation on the first memory cells.