CLAIMS

What is claimed is:

1. An apparatus, comprising:

a memory controller configured to provide memory instructions;

a memory coupled to the memory controller and configured to receive a memory instruction therefrom and perform a memory operation responsive thereto, the memory further configured to provide an acknowledgement indicative of an end of the variable latency period wherein the acknowledgement includes information related to an acceptance of a memory instruction, the memory further configured to exchange data associated with the memory instruction with the memory controller following the acknowledgement.

2. The apparatus of claim 1 wherein the memory includes a write buffer configured to store write data.

3. The apparatus of claim 1 wherein the memory is further configured to suspend a write operation in progress responsive to receiving a read instruction.

4. The apparatus of claim 1 wherein the memory is configured to receive memory instructions, addresses, and data on shared input/outputs.

5. The apparatus of claim 1 wherein the memory is configured to receive memory instructions and addresses on a shared input, and data on input/outputs.

6. The apparatus of claim 1 wherein the memory is configured to prepare itself for a memory operation during the variable latency period.

7. The apparatus of claim 1 wherein the acknowledgement includes the information that the latency period has ended with further qualifications.

8. The apparatus of claim 1 wherein the acknowledgement includes information that the memory instruction is accepted but there is a warning due to the occurrence of an error during an operation of a previous memory instruction.

9. The apparatus of claim 1 wherein the acknowledgement includes information that the memory instruction is accepted but there is a warning due to the need of a house keeping operation.

10. The apparatus of claim 9 wherein the house keeping operation comprises at least one of wear leveling, refreshing, or combinations thereof.

11. The apparatus of claim 1 wherein the acknowledgement includes information that the memory instruction is rejected.

12. The apparatus of claim 1 wherein the memory is configured to wait a bus turnaround time following the acknowledgement before data is received by the memory.

13. An apparatus, comprising:

a memory array having memory cells; and

a memory operation controller configured to receive memory instructions and decode the same to provide internal signals for performing memory operations for the memory instructions, the memory operation controller further configured to wait a hold-off period before resuming a suspended memory operation.

14. The apparatus of claim 13 wherein the memory operation controller is configured to suspend a write operation in response to receipt of a read instruction and perform a read operation.

15. The apparatus of claim 14, further comprising a register configured to store a maximum hold-off period and the memory operation controller is configured to wait the maximum hold-off period and then resume the suspended write operation.

16. The apparatus of claim 14 wherein the memory operation controller is configured to continue to suspend the write operation responsive to receipt of the read instruction during the hold-off period and to perform the read operation and to restart the hold-off period at the end of the read operation.

17. The apparatus of claim 14 wherein the memory operation controller is configured to resume the suspended write operation in response to receipt of a write instruction.

18. The apparatus of claim 13 wherein the memory cells comprise phase change memory cells.

19. The apparatus of claim 13, further comprising a register configured to store a maximum variable latency period.

20. The apparatus of claim 19 wherein the register is configured to store a maximum variable latency period for write operations and store a maximum variable latency period for read operations.

21. The apparatus of claim 13 wherein the memory operation controller is configured to provide an acknowledgement indicative of an end of a variable latency period for a memory instruction.

22. The apparatus of claim 21 wherein the memory operation controller is configured to manage memory operations during the variable latency period.

23. The apparatus of claim 21 wherein the memory operation controller is configured to prepare memory circuits for performing memory operations during the variable latency period.

24. An apparatus, comprising:

a memory array having memory cells;

a write buffer configured to store write data to be written to the memory array;

a memory operation controller configured to receive memory instructions and decode the same to provide internal signals for performing memory operations for the memory instructions, the memory operation controller further configured to provide an acknowledgement indicative of an end of the variable latency period; and

a register coupled to the memory operation controller and configured to store information related to a hold-off period following completion of a read operation before resuming a suspended write operation.

25. The apparatus of claim 24 wherein the register is configured to store information related to a maximum latency period for read and write operations.

26. The apparatus of claim 25 wherein the memory operation controller is configured to determine whether to suspend a current memory operation in progress or to allow a current memory operation to complete based at least in part on the maximum latency period.

27. The apparatus of claim 24 wherein the register is included in the memory operation controller.

28. The apparatus of claim 24 wherein the memory operation controller is configured to suspend a memory operation in progress to begin performing a new memory operation during the variable latency period based at least in part on stored information related to a maximum latency period.

29. The apparatus of claim 24 wherein the memory operation controller is configured to complete a memory operation during the variable latency period based at least in part on stored information related to a maximum latency period.

30. A method, comprising:

receiving at a memory a write instruction and an address to which write data is to be written;

providing an acknowledgement indicative of an end of the variable latency period;

waiting a bus turnaround time following the acknowledgement; and

receiving the write data for the write instruction.

31. The method of claim 30, further comprising:

performing a write operation for the write instruction;

suspending the write operation responsive to receiving a read instruction during the write operation.

32. The method of claim 30, further comprising:

storing the write data received for the write instruction in a write data buffer.

33. The method of claim 30 wherein the write data for the write instruction is received after the acknowledgement is provided and after a bus turnaround time.

34. The method of claim 30, further comprising:

performing a write operation responsive to receiving the write instruction; and

writing write data to memory that are stored in a write data buffer.

35. The method of claim 34 wherein the write data that are stored in the write data buffer is associated with a plurality of write instructions and the write operation is performed responsive to a last write instruction of the plurality of write instructions.

36. The method of claim 30 wherein the bus turnaround time is measured relative to the acknowledgement.

37. A method, comprising:

receiving at a memory a read instruction and an address from which read data is to be read;

suspending a write operation responsive to the read instruction;

providing an acknowledgement indicative of an end of the variable latency period;

providing the read data for the read instruction; and

continuing to suspend the write operation for a hold-off period following completion of the read operation.

38. The method of claim 37 wherein the read data for the read instruction is provided following providing the acknowledgement.

39. The method of claim 37, further comprising:

receiving another read instruction during the hold-off period;

further suspending the write operation responsive to receiving the another read instruction;

performing a read operation for the another read instruction and restarting the hold-off period at the end of the read operation.

40. The method of claim 37, further comprising:

receiving a write instruction during the hold-off period;

resuming the suspended write operation responsive to receiving the write instruction.

41. The method of claim 37, further comprising:

resuming the suspended write operation responsive to the hold-off period expiring.

42. A method, comprising:

receiving at a memory memory instructions and addresses associated with the memory instruction;

providing an acknowledgement indicative of an end of the variable latency period and including information related to an acceptance of a memory instruction; and

receiving or providing data associated with the memory instruction.

43. The method of claim 42 wherein the memory instructions and addresses associated with the memory instruction are received concurrently.

44. The method of claim 42 wherein the time for a variable latency period for the memory instruction is based at least in part on a current memory operation and the memory instruction.

45. The method of claim 42 wherein the memory instructions comprise a plurality of write instructions, and the method further comprises:

storing write data for the plurality of write instructions in a write data buffer;

responsive to a last write instruction, writing the write data for the plurality of write instructions stored in the write buffer to memory.

46. The method of claim 42, further comprising waiting a bus turnaround time following the acknowledgement before providing data associated with a write instruction.

47. The method of claim 42, further comprising waiting a bus turnaround time following the addresses associated with the memory instruction.

48. The method of claim 42, further comprising:

waiting a bus turnaround time after receiving the addresses.

49. A method, comprising:

providing a memory instruction and an address to a memory;

receiving an acknowledgement indicative of an end of the variable latency period and including information related to acceptance of the memory instruction by the memory; and

exchanging data associated with the memory instruction with the memory.

50. The method of claim 49 wherein the acknowledgement is represented by a combination of logic states of a plurality of signals.

51. The method of claim 49 wherein exchanging data associated with the memory instruction with the memory occurs a bus turnaround time after receiving the acknowledgment for a write instruction.

52. The method of claim 49, further comprising keeping a system bus busy until completion of a memory operation as represented by the received acknowledgment.

53. The method of claim 49, further comprising aborting a memory operation related to the memory instruction to free a system bus and retrying the memory operation again at a later time.

## CLAIMS

1. An apparatus, comprising:

a memory controller configured to provide memory instructions;

a memory coupled to the memory controller and configured to receive a memory instruction therefrom and perform a memory operation responsive thereto, the memory further configured to manage the memory operation during a variable latency period, the memory further configured to provide an acknowledgement indicative of an end of the variable latency period wherein the acknowledgement includes information related to an acceptance of the memory instruction, the memory further configured to exchange data associated with the memory instruction with the memory controller following the acknowledgement; and

a register configured to store a maximum variable latency period, wherein the register is configured to store a maximum variable latency period for write operations and store a maximum variable latency period for read operations.

2. The apparatus of claim 1 wherein the memory includes a write buffer configured to store write data.

3. The apparatus of claim 1 wherein the memory is further configured to suspend a write operation in progress responsive to receiving a read instruction.

4. The apparatus of claim 1 wherein the memory is configured to receive memory instructions, addresses, and data on shared input/outputs.

5. The apparatus of claim 1 wherein the memory is configured to receive memory instructions and addresses on a shared input, and data on input/outputs.

6. The apparatus of claim 1 wherein the memory is configured to prepare itself for a memory operation during the variable latency period.

7. The apparatus of claim 1 wherein the acknowledgement includes the information that the latency period has ended with further qualifications.

8. The apparatus of claim 1 wherein the acknowledgement includes information that the memory instruction is accepted but there is a warning due to the occurrence of an error during an operation of a previous memory instruction.

9. The apparatus of claim 1 wherein the acknowledgement includes information that the memory instruction is accepted but there is a warning due to the need of a house keeping operation.

10. The apparatus of claim 9 wherein the house keeping operation comprises at least one of wear leveling, refreshing, or combinations thereof.

11. The apparatus of claim 1 wherein the acknowledgement includes information that the memory instruction is rejected.

12. The apparatus of claim 1 wherein the memory is configured to wait a bus turnaround time following the acknowledgement before data is received by the memory.

13. An apparatus, comprising:

a memory array having memory cells;

a memory operation controller configured to receive memory instructions and decode the same to provide internal signals for performing memory operations for the memory instructions, the memory operation controller further configured to wait a predetermined hold-off period following performance of the memory operations, to await additional memory instructions, before resuming a suspended memory operation; and

a register configured to store a maximum variable latency period, wherein the register is configured to store a maximum variable latency period for write operations and store a maximum variable latency period for read operations.

14. The apparatus of claim 13 wherein the memory operation controller is configured to suspend a write operation in response to receipt of a read instruction and perform a read operation.

15. The apparatus of claim 14, further comprising a register configured to store a maximum hold-off period and the memory operation controller is configured to wait the maximum hold-off period and then resume the suspended write operation.

16. The apparatus of claim 14 wherein the memory operation controller is configured to continue to suspend the write operation responsive to receipt of the read instruction during the hold-off period and to perform the read operation and to restart the hold-off period at the end of the read operation.

17. The apparatus of claim 14 wherein the memory operation controller is configured to resume the suspended write operation in response to receipt of a write instruction.

18. The apparatus of claim 13 wherein the memory cells comprise phase change memory cells.

19. The apparatus of claim 13 wherein the memory operation controller is configured to provide an acknowledgement indicative of an end of a variable latency period for a memory instruction.

20. The apparatus of claim 19 wherein the memory operation controller is configured to manage memory operations during the variable latency period.

21. The apparatus of claim 19 wherein the memory operation controller is configured to prepare memory circuits for performing memory operations during the variable latency period.

22. An apparatus, comprising:

a memory array having memory cells;

a write buffer configured to store write data to be written to the memory array;

a memory operation controller configured to receive memory instructions and decode the same to provide internal signals for performing memory operations for the memory instructions, the memory operation controller further configured to provide an acknowledgement indicative of an end of the variable latency period;

a register coupled to the memory operation controller and configured to store information related to a hold-off period following completion of a read operation to await additional memory instructions before resuming a suspended write operation and further configured to store a maximum variable latency period, wherein the register is configured to store a maximum variable latency period for write operations and store a maximum variable latency period for read operations.

23. The apparatus of claim 22 wherein the register is configured to store information related to a maximum latency period for read and write operations.

24. The apparatus of claim 23 wherein the memory operation controller is configured to determine whether to suspend a current memory operation in progress or to allow a current memory operation to complete based at least in part on the maximum latency period.

25. The apparatus of claim 22 wherein the register is included in the memory operation controller.

26. The apparatus of claim 22 wherein the memory operation controller is configured to suspend a memory operation in progress to begin performing a new memory operation during the variable latency period based at least in part on stored information related to a maximum latency period.

27. The apparatus of claim 22 wherein the memory operation controller is configured to complete a memory operation during the variable latency period based at least in part on stored information related to a maximum latency period.

28. A method, comprising:

receiving at a memory a read instruction and an address from which read data is to be read;

during a variable latency period for the read instruction, suspending a write operation responsive to the read instruction;

providing an acknowledgement indicative of an end of the variable latency period;

providing the read data for the read instruction;

continuing to suspend the write operation for a hold-off period following completion of the read operation, wherein the memory waits for additional memory instructions during the hold-off period;

receiving another read instruction during the hold-off period;

further suspending the write operation responsive to receiving the another read instruction; and

performing a read operation for the another read instruction and restarting the hold-off period at the end of the read operation.

29. The method of claim 28 wherein the read data for the read instruction is provided following providing the acknowledgement.

30. The method of claim 28, further comprising:

receiving a write instruction during the restarted hold-off period;

resuming the suspended write operation responsive to receiving the write instruction.

31. The method of claim 28, further comprising:

resuming the suspended write operation responsive to the restarted hold-off period expiring.