(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
4 August 2005 (04.08.2005)

PCT

(10) International Publication Number
WO 2005/071738 A3

(51) International Patent Classification[7]: H01L 21/762, 21/336

(21) International Application Number:
PCT/US2004/043107

(22) International Filing Date:
21 December 2004 (21.12.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/755,602 12 January 2004 (12.01.2004) US

(71) Applicant *(for all designated States except US)*: **ADVANCED MICRO DEVICES, INC.** [US/US]; One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **XIANG, Qi** [CN/US]; 1119 Thames Drive, San Jose, CA 95129 (US). **PAN, James, N.** [—/US]; 3 Mountain View Knolls Drive, Apt. D, Fishkill, NY 12524 (US). **GOO, Jung-Suk** [KR/US]; 100 Escondido Village, #D, Stanford, CA 94305 (US).

(74) Agent: **DRAKE, Paul, S.**; One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

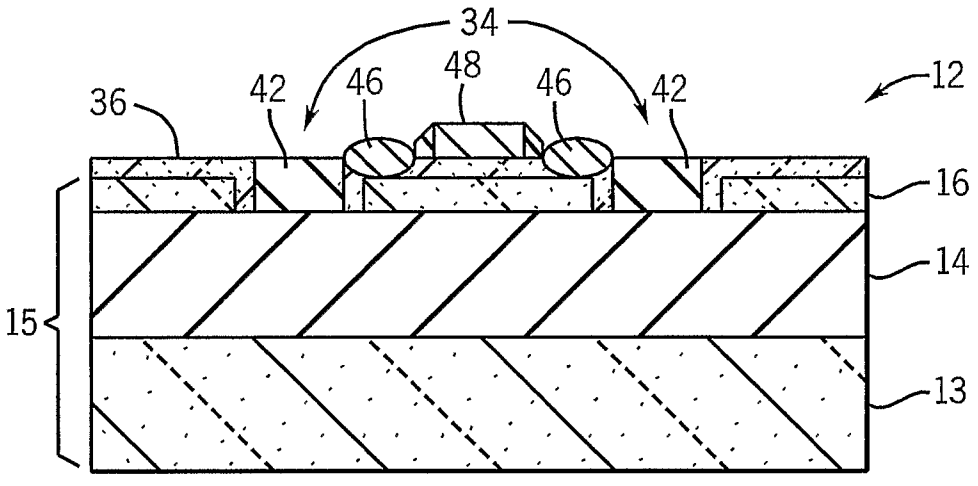
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report:
8 December 2005

[Continued on next page]

(54) Title: SHALLOW TRENCH ISOLATION PROCESS AND STRUCTURE



(57) Abstract: A method of manufacturing an integrated circuit (IC) utilizes a shallow trench isolation (STI) technique. The shallow trench isolation technique is used in strained silicon (SMOS) process. The strained material (36) is formed after the trench (34) is formed. The process can be utilized on a compound semiconductor layer (15) above a buried oxide (Box) layer (14).

WO 2005/071738 A3

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.