INTEGRATED CIRCUIT DEVICE WITH CROSSED POWER STRAP LAYOUT

TECHNICAL FIELD

[0001] The present disclosure relates generally to an integrated circuit device and method for fabrication, and more specifically to an integrated circuit device with straddled interconnects.

BACKGROUND

[0002] An integrated circuit (IC) is formed by creating one or more devices (e.g., circuit components) on a semiconductor substrate using a fabrication process. As fabrication processes and materials improve, semiconductor device geometries have continued to decrease in size since such devices were first introduced several decades ago. For example, current fabrication processes are producing devices having geometry sizes (e.g., the smallest component (or line) that may be created using the process) of less than 90 nm. However, the reduction in size of device geometries frequently introduces new challenges that need to be overcome.

[0003] As microelectronic devices are scaled below 90 nm, the electrical power efficiency and distribution become an issue that impacts device performance. The modern integrated circuit employs a plurality of conductive interconnect layers to provide distribution of electrical power to a plurality of microelectronics devices, however optimal device performance are not achieved with interconnect designs employed in many of the today's microelectronics products.

[0004] Accordingly, what is needed in the art is a integrated circuit device and method thereof that addresses the above discussed issues.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0006] Fig. 1 illustrates a sectional view of one embodiment of a microelectronics integrated circuit device slice constructed according to aspects of the present disclosure.

[0007] Fig. 2 illustrates a sectional view of one embodiment of partitioned cross strap interconnect structure constructed according to aspects of the present disclosure.

[0008] Fig. 3 illustrates a sectional view of another embodiment of partitioned corrugated cross strap interconnect structure constructed according to aspects of the present disclosure.

[0009] Fig. 4 illustrates a sectional view of an embodiment of an integrated circuit device constructed according to aspects of the present disclosure.

[0010] Fig. 5 illustrates a sectional view of another embodiment of an integrated circuit device constructed according to aspects of the present disclosure.

DETAILED DESCRIPTION

[0011] The present disclosure relates generally to an integrated circuit device and method for fabrication, and more specifically to an integrated circuit device with straddled interconnects. It is understood that the following disclosure provides many different embodiments or examples. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0012] Referring to Fig. 1, illustrated is a sectional view of one embodiment of a microelectronics integrated circuit device slice 100 constructed according to aspects of the present disclosure. The slice 100 comprises an interconnect space 110, a bond layer 120, a device layer 140, and a substrate 105.

[0013] The interconnect space 100 comprises a plurality of patterned conductive interconnect layers. The interconnect layers may comprise of conductive materials such as Cu, Al, Mo, MoSi, Ni, NiSi, TiN, TaN, Ti, Ta, SiC, CoSi, WSi, and/or other materials. The interconnect layers may also be encapsulated with low-k dielectric material.

[0014] The bond layer 120 comprises a plurality of conductive pads 130 surrounded by an insulating material. The pads 130 comprise conductive materials such as Pt, Al, Cu, Ag, Au, Ni, Mo, and/or other conductive materials. The pads 130 may also comprise a plurality of subordinate patterned features to provide a reduction in mechanical stress of the surrounding dielectric material. The subordinate patterned features may include a plurality of small blocks substantially smaller than the pads 130. The population of pads within the bond layer 120 may be characterized by the population of microelectronic devices 150, the chip (not shown) dimensions, the minimum device feature dimensions, the minimum device gate thickness, and/or other device parameters. For example, the chip dimensions may range between about 4 mm^2 and about 100 mm^2, the population of the microelectronic devices may range between about 40 million and about 10 billion, while the minimum device feature and thickness may range between about 3 Angstroms and about 800 Angstroms. Therefore, the pads 130 population may be scaled according to the integrated circuit device 100, wherein the pads 130 population may range between about 2 and about 512.

[0015] The device layer 140 comprises a plurality of microelectronics devices 150. The microelectronics devices 150 may be formed from, in or on a common substrate which may be substantially similar in composition and manufacture to the substrate 105. Of course, the integrated circuit device 100 may include other types of substrates 105, or multiple substrates, within the scope of the present disclosure. Each of the microelectronic devices 150 includes at least one electrical contact 160.

[0016] For example, each microelectronic device 150 may include one or more transistors, gates, an electrically programmable read only memory (EPROM) cell, an electrically erasable programmable read only memory (EEPROM) cell, a static random access memory (SRAM) cell, a dynamic random access memory (DRAM) cell and/or other microelectronic devices (hereafter collectively referred to as microelectronic devices).

[0017] The substrate 105, upon which the plurality of microelectronics devices 150 are formed, includes one or more layers of materials, structures, or other features. Each of which

may be formed by various known methods, such as immersion photolithography, maskless photolithography, chemical-vapor deposition (CVD), physical-vapor deposition (PVD), plasma-enhanced CVD (PECVD), atomic layer deposition (ALD) and/or other process techniques. Conventional and/or future-developed lithographic, etching and other processes may be employed to define the integrated circuit device 100 from the deposited layers.

[0018] The substrate 105 may be a silicon-on-insulator (SOI) substrate, and may comprise silicon, gallium arsenide, gallium nitride, strained silicon, silicon germanium, silicon carbide, carbide, diamond and/or other materials.

[0019] Referring to Fig. 2, a partitioned cross-strap interconnect structure 200 includes the device layer 140 and a plurality of interconnect layers 220, 230, 240, ad 250. The layers 220, 230, and 240 include a plurality of conductive interconnect straps 222, 232, and 242. Each of the straps 222, 232, and 242 include a plurality of electrical contacts or vias 224, 234, and 244 to provide contact to the electrical contacts 160, and/or the another strap. The straps 222, 232, and 242 may be formed in a plurality of patterns, such as but not limited to rectangles, circles, or lines. The straps 222, 232, and 242 provide electrical signals or power (collectively power) to the plurality of microelectronic devices 150, wherein at least one strap 222, 232, and 242 may provide an electrical ground potential V_{ss}, and/or an electrical potential V_{cc} of an external power supply (not shown). Therefore, a population of each of the straps 222, 232, and/or 242 may provide the grounding potential V_{ss}, and another population may provide the power supply potential V_{cc}. Additional internal or external power may also be provided. The straps 222, 232, and 242 may be directionally oriented within the layers 220, 230, and 240. For example, the straps 222 may be orthogonal relative to the straps 232 and/or may be congruent with the direction of the straps 242. Each of the straps 222, 232, and/or 242 may further connect to alternating microelectronics devices 150, and/or alternating other straps. Alternatively, the straps 222, 232, and/or 242 may be electrically isolated within the dielectric material encompassing the straps. The electrically isolated or "dummy" straps may provide stress relief and/or an indication of process completion, such as during chemical mechanical processing (CMP).

[0020] In another embodiment, the pads 130 population for the ground potential V_{ss} and/or the power supply potential V_{cc} may scale according to the construction of the straps 222, 232, and 242 of the layers 220, 230, and 240. Therefore, the V_{cc} pads 130 population may range between about 2 and about 512, and/or the V_{ss} pads 130 population for may range between about

2 and about 512. The population increase of the ground potential V_{ss} and/or the power supply potential V_{cc} pads 130 may provide substantial reduction in power leakage and noise reduction, and more specifically, in microelectronics devices 150 with minimum features ranging between about 1500 Angstroms and about 3 Angstroms.

[0021] The layer 220, in one embodiment, includes a plurality of straps 222 electrically connected through vias 224 to the electrical contacts 160 of each of the microelectronics devices 150. This connection is shown in Fig. 2 with the dotted lines 226. Alternatively, the straps 222 may connect to alternating microelectronics devices 150, and may also straddle a plurality of microelectronics devices 150. For example, the strap 222 may connect to alternating microelectronics devices 150, wherein the alternating contact may be positioned horizontal and/or diagonal relative to the plane of the device layer 140. The alternating via 224 contact may be located at multiple alternating contacts 160 of the microelectronics devices 150, wherein the alternating vias 224 may occur every second, third, fourth, eight, twenty-four, thirty-two, sixty-four and/or other multiples within the strap 222. The straps 222 may further have a width ranging between about 1600 Angstroms and about 5 Angstroms.

[0022] The layer 230, in one embodiment, includes a plurality of straps 232 electrically connected through vias 234 to the straps 222. This connection is shown in Fig. 2 with the dotted lines 236. Alternatively, the straps 232 may connect to alternating straps 222, and may also straddle a plurality of microelectronics devices 150 and/or the straps 222. For example, the strap 232 may connect to alternating microelectronics devices 150 and/or straps 222, wherein the alternating contact may be positioned horizontal and/or diagonal relative to the plane of the layer 230. The alternating via 234 contact may be located at multiple alternating straps 222, wherein the alternating vias 234 may occur every second, third, fourth, eight, twenty-four, thirty-two, sixty-four and/or other multiples within the strap 232. The straps 232 may further have a width ranging between about 1800 Angstroms and about 5 Angstroms.

[0023] The layer 240, in one embodiment, includes a plurality of straps 242 electrically connected through vias 244 to the straps 232, and/or the straps 222. This connection is shown in Fig. 2 with the dotted lines 246. Alternatively, the straps 242 may connect to alternating straps 232, and may also straddle a plurality of microelectronics devices 150 and/or the straps 222 and 232. For example, the strap 242 may connect to alternating microelectronics devices 150 and/or straps 222 and 232, wherein the alternating contact may be positioned horizontal and/or diagonal

relative to the plane of the layer 240. The alternating via 244 contact may be located at multiple alternating straps 232 and/or 222, wherein the alternating vias 244 may occur every second, third, fourth, eight, twenty-four, thirty-two, sixty-four and/or other multiples within the strap 242. The straps 242 may further have a width ranging between about 2000 Angstroms and about 5 Angstroms.

[0024] The layer 250, in one embodiment, includes a plurality of V_{ss} pads 252 and V_{cc} pads 254 electrically connected to the straps 242, and/or the straps 232, 222. This connection is shown in Fig. 2 with the dotted lines 256 and 258.

[0025] Referring to Fig. 3, another embodiment of a partitioned corrugated cross strap interconnect structure 300 includes the device layer 140, a plurality of interconnect layers 320, 330, 340, and 350.

[0026] The structure 300 may be configured similar to the structure 200, however the layers 320, 330, and/or 340 may comprise a plurality of corrugated straps 310. The corrugated straps 310 comprises an interconnect, wherein v-shaped grooves and/or valleys may be constructed within the depth of the integrated circuit device 100. The corrugated straps 310 provides for higher via 320-322 density, and further allows for reduced chip dimensions.

[0027] The structure 300 also contemplates the electrical connections between the plurality of interconnect layers 320, 330, 340, and 350. For example, via 320-322 may each be connected to via 334f-334g. In layer 330, via 334 may be connected to via 324a-324g. The electrical connects between layer 320 to the device layer 140 may comprise via 324a-324g may be connected to contacts 160a-160g. Alternatively, there may be multiple via 324d-324e connected to the contacts 160d-160e.

[0028] Referring to Fig. 4, an integrated circuit device 400 is one environment in which the microelectronics devices 150 and the straps 322, 332, and 342 may be incorporated. For example, the integrated circuit device 400 includes a plurality of microelectronics devices 150, wherein one or more of the microelectronics devices 150 may be substantially similar. The substrate 105 may also include one or more uniformly or complementary doped wells 402. While not limited to any particular dopant types or schemes, in one embodiment, the doped wells 402 employ boron as a p-type dopant and deuterium-boron complexes for an n-type dopant. The deuterium-boron complexes may be formed by plasma treatment of boron-doped diamond layers with a deuterium plasma.

[0029] In one embodiment, the doped wells 402 may be formed using a high density plasma source with a carbon-to-deuterium ratio ranging between about 0.1 percent and about 5 percent in a vacuum process ambient. Boron doping may be provided by the mixing of a boron containing gas with a carbon/hydrogen gas. The boron containing gas may include B_2H_6, B_2D_6 and/or other boron containing gases. The concentration of boron doping may depend upon the amount of boron containing gas that may be leaked or added into the process. The process ambient pressure may range between 0.1 mTorr and about 500 Torr. The substrate 105 may be held at a temperature ranging between 150°C and about 1100°C. High density plasma may be produced by a microwave electron cyclotron resonance (ECR) plasma, a helicon plasma, a inductively coupled plasma and/or other high density plasma sources. For example, the ECR plasma may utilize microwave powers ranging between about 800 Watts and about 2500 Watts.

[0030] As described above, the doped wells 402 may also comprise n-type deuterium-boron complex regions of the substrate 105, which may be formed by treating the above-described boron-doped regions employing a deuterium plasma. For example, selected areas of the substrate 105 may be covered by photoresist or another type of mask such that exposed boron-doped regions may be treated with the deuterium containing plasma. The deuterium ions may provide termination of dangling bonds, thereby transmuting the p-type boron-doped regions into n-type deuterium-boron complex regions. Alternatively, deuterium may be replaced with tritium, hydrogen and/or other hydrogen containing gases. The concentration of the n-type regions may generally be controlled by a direct current (DC) or a radio frequency (RF) bias of the substrate 105. The above-described processes may also be employed to form lightly-doped source/drain regions in the substrate 105. Of course, other conventional and/or future-developed processes may also or alternatively be employed to form the source/drain regions.

[0031] The integrated circuit device 400 also includes one or more insulating layers 420, 430 located over the microelectronics devices 150. The first insulating layer 420, which may itself comprise multiple insulating layers, may be planarized to provide a substantially planar surface over the plurality of microelectronics devices 150.

[0032] The integrated circuit device 400 also includes vertical interconnects 440, such as conventional vias or contacts, and horizontal interconnects 450 (all spatial references herein are for the purpose of example only and are not meant to limit the disclosure). The interconnects 440 may extend through one or more of the insulating layers 420, 430, and the interconnects 450

may extend along one of the insulating layers 420, 430 or a trench formed therein. In one embodiment, one or more of the interconnects 440, 450 may have a dual-damascene structure. The interconnects 440, 450 may be formed by etching or otherwise patterning the insulating layers 420, 430 and subsequently filling the pattern with refractive and/or conductive material, such as tantalum nitride, copper and aluminum.

[0033] Referring to Fig. 5, illustrated is a sectional view of one embodiment of an integrated circuit device 500 constructed according to aspects of the present disclosure. The integrated circuit device 500 is another environment in which a microelectronics devices 150, and the straps 222, 232, and 242 may be incorporated. For example, the integrated circuit device 500 includes a plurality of microelectronics devices 150, wherein one or more of the microelectronics devices 150 may be substantially similar. The integrated circuit device 500 may include a plurality of device layers 510 and 520. The layer 510 and 520 may be fabricated by similar methods utilized for fabricating the integrated circuit device 400 and/or 100, as may be well known by one skilled in the art. The integrated circuit device 500 further comprises a stack layer 530.

[0034] The stack layer 530 comprises a plurality of transition interconnects 540 and a plurality of materials for isolating the layers 510 and 520.

[0035] The stack layer 530 may comprise a low-k dielectric material such as SiO_2, SiN, SiC, and/or other materials. The stack layer 530 may also comprise a silicon and/or semiconductor layer to provide the foundation for the fabrication of the layer 520. For example, the stack layer 530 may be formed by a metal-induced lateral crystallization (MILC) process. The MILC process may include the formation of an amorphous silicon layer followed by the deposition of a porous SiO_2 layer, wherein a seed metal layer may be formed over the porous SiO_2 layer. The seed metal may allow for lateral crystallization of the amorphous Si layer at a temperature range of about 400° C and about 600° C. The metal seed layer may comprise Ni, Co, W, Ti, Ta, Mo, and/or other materials. Following the crystallization, the metal seed layer may be removed by plasma and/or chemical etching. The stack layer 530 may further comprise a plurality of low temperature polysilicon layers over the MILC crystallized layer, and may be further subjected to an anneal.

[0036] The transition interconnects 540 comprise a plurality of conductive interconnects and/or straps to interconnect the layers 510 and 520. In one embodiment, one or more of the transition interconnects 540 may have a dual-damascene structure. The transition interconnects

540 may be formed by etching or otherwise patterning the stack layer 530, and subsequently filling the pattern with refractive and/or conductive material, such as tantalum nitride, germanium, doped silicon, copper and/or aluminum.

[0037] Although embodiments of the present disclosure have been described in detail, those skilled in the art should understand that they may make various changes, substitutions and alterations herein without departing from the spirit and scope of the present disclosure. Accordingly, all such changes, substitutions and alterations are intended to be included within the scope of the present disclosure as defined in the following claims. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents, but also equivalent structures.

WHAT IS CLAIMED IS:

1. An integrated circuit device, comprising:

a substrate;

a plurality of microelectronic devices, each comprising a patterned feature located over the substrate, wherein the pattern feature comprises at least one electrical contact;

a plurality of interconnect layers for distributing electrical power to the plurality of microelectronic devices, comprising a plurality of conductive members associated with each interconnect layer, wherein the members of at least one subsequent interconnect layer straddle members of at least one adjacent interconnect layer; and

a plurality of bond pads connected to at least one of the plurality of members of the interconnect layers.

2. The integrated circuit device of claim 1 wherein the members of selected portions of the interconnect layer are electrically connected to a ground potential.

3. The integrated circuit device of claim 1 wherein the members of selected portions of the interconnect layer are electrically connected to an electrical potential.

4. The integrated circuit device of claim 1 wherein the interconnects of the interconnect layer electrically contact at least one contact of each of the microelectronic devices.

5. The integrated circuit device of claim 1 further comprising:

a first layer comprising conductive interconnects electrically contacting at least one microelectronic device;

a second layer comprising conductive lines orthogonally aligned relative to the lines of the first layer, the lines of the second layer electrically contact the lines of the first layer;

a third layer comprising conductive lines orthogonally aligned relative to the lines of the second layer, the lines of the third layer electrically contact the lines of the second layer; and

a plurality of vias for interconnecting the first layer to the second layer, and interconnecting the third layer to the second layer.

6. The integrated circuit device of claim 5 wherein the vias provide alternating contact to contacts of the first level, and wherein the contacts alternate in a range between about one and about sixty-four.

7. The integrated circuit device of claim 2 wherein the population of the plurality of bond pads associated with the ground potential range between about 2 and about 512.

8. The integrated circuit device of claim 3 wherein the population of the plurality of bond pads associated with the electrical potential range between about 2 and about 512.

9. The integrated circuit device of claim 1 wherein the substrate comprises diamond.

10. The integrated circuit device of claim 1 wherein the substrate comprises strained silicon.

11. The integrated circuit device of claim 1 wherein the substrate comprises silicon carbide.

12. A method of manufacturing an integrated circuit device, comprising:

providing a substrate;

forming a plurality of microelectronic devices each comprising a patterned feature located over the substrate, wherein the pattern feature comprises at least one electrical contact;

forming a plurality of interconnect layers for distributing electrical power to the plurality of microelectronic devices, comprising a plurality of conductive members associated with each interconnect layer, wherein the members of at least one subsequent interconnect layer straddle members of at least one adjacent interconnect layer; and

providing a plurality of bond pads connected to at least one of the plurality of members of the interconnect layers.

13. The method of claim 12 wherein the members of selected portions of each of interconnect layers are electrically connected to a ground potential.

14. The method of claim 12 wherein the members of selected portions of each of the interconnect layers are electrically connected to an electrical potential.

15. The method of claim 12 wherein the interconnects of selected portions of the interconnect layers electrically contacts at least one contact of each of the microelectronic devices.

16. The method of claim 12 further comprising:

providing a first layer comprising conductive interconnects electrically contacting at least one microelectronic device;

forming a second layer comprising conductive lines orthogonally aligned relative to the lines of the first layer, the lines of the second layer electrically contact the lines of the first layer;

forming a third layer comprising conductive lines orthogonally aligned relative to the lines of the second layer, the lines of the third layer electrically contact the lines of the second layer; and

providing a plurality of vias for interconnecting the first layer to the second layer, and interconnecting the third layer to the second layer.

17. The method of claim 16 wherein the conductors of the first interconnect layer contact at least one contact of each of the microelectronic devices.

18. The method of claim 12 wherein the substrate comprises diamond.

19. The method of claim 12 wherein the substrate comprises strained silicon.

20. A three-dimensional integrated circuit device, comprising:

a substrate;

a plurality of microelectronic device layers, the layers each comprising a plurality of microelectronic devices, and a plurality of interconnect layers for distributing electrical power to the plurality of microelectronic devices;

a transition interconnect layer comprising a plurality of conductive interconnects for electrically connecting the device layers; and

a plurality of bond pads connected to at least one of the plurality of members of the device layers.

21. The three-dimensional integrated circuit device of claim 20 wherein the microelectronics device includes a patterned feature located within the device layers, wherein the pattern feature comprises at least one electrical contact.

22. The three-dimensional integrated circuit device of claim 20 wherein a plurality of conductive members associated with each of the interconnect layers, wherein the members of at least one subsequent interconnect layer straddle members of at least one adjacent interconnect layer.

23. The three-dimensional integrated circuit device of claim 20 wherein the transition layer further comprises:

a dielectric layer formed substantially over at least one device layer;

a first semiconductor layer comprising silicon;

a conductive seed layer comprising a metal over the first semiconductor layer; and

a second semiconductor layer comprising silicon.