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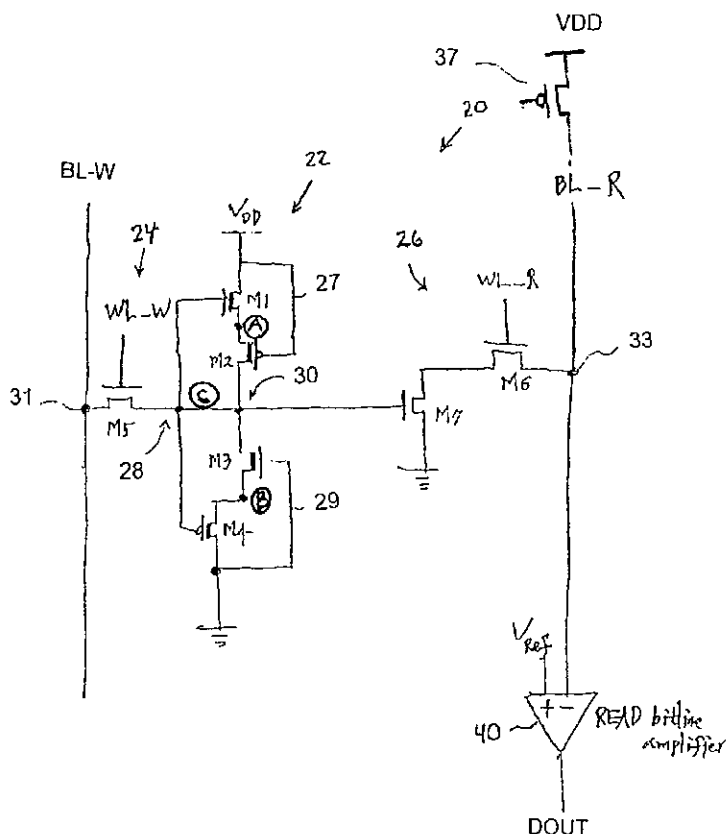
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- (71) Applicant (for all designated States except US): THE REGENTS OF THE UNIVERSITY OF CALIFORNIA [US/US]; 111 Franklin Street, 12th floor, Oakland, CA 94607-5200 (US).
- (74) Agents: DURANT, Stephen, C. et al.; Morrison & Forster LLP, 425 Market Street, San Francisco, CA 94105-2482 (US).
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(54) Title: LOW-POWER HIGH-PERFORMANCE MEMORY CELL AND RELATED METHODS



(57) Abstract: An integrated circuit comprising a first NMOS transistor; a first PMOS transistor; a second NMOS transistor; a second PMOS transistor; a first bias voltage node coupled to a first source/drain of the second PMOS; a third bias voltage node coupled to a gate of the first PMOS transistor; a fourth bias voltage node coupled to a gate of the first PMOS transistor; a pull-up node coupling a second source/drain of the first NMOS transistor to a first source/drain of the first PMOS transistor; a pull-down node coupling a second source/drain of the second NMOS transistor to a first source/drain of the second PMOS transistor; an input node; a storage node coupling a second source/drain of the first PMOS transistor to a second source/drain of the second NMOS transistor; an output node; and input switch coupled to controllably communicate an input data value from the input node to a gate of the first NMOS transistor and to a gate of the second PMOS transistor; and an output switch coupled to controllably communicate a stored data value from the storage node to the output node.

WO 03/083872 A2



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