

MASKING METHODS

TECHNICAL FIELD

5 This invention relates to methods of masking semiconductor substrates in the fabrication of integrated circuitry.

BACKGROUND ART

10 Integrated circuits are typically formed on a semiconductor substrate such as a silicon wafer or other semiconducting material. In general, layers of various materials which are either semiconducting, conducting or insulating are utilized to form the integrated circuits. By way of example, the various materials are doped, ion implanted, deposited, etched, grown, etc. using various processes. A continuing goal in semiconductor processing is to continue to strive to reduce the size of individual
15 electronic components thereby enabling smaller and denser integrated circuitry.

 One technique for patterning and processing semiconductor substrates is photolithography. Such typically includes deposition of a photoresist layer which can then be processed to modify the solubility of such layer in certain solvents. For example, portions of the photoresist layer can be exposed to actinic energy through a mask/reticle
20 to change the solvent solubility of the exposed regions versus the unexposed regions compared to the solubility in the as-deposited state. Thereafter, the exposed or unexposed portions can be removed, depending on the type of photoresist, thereby leaving a masking pattern of the photoresist on the substrate. Adjacent areas of the substrate next to the masked portions can be processed, for example by etching or ion
25 implanting, to effect the desired processing of the substrate adjacent the masking material.

 In certain instances, multiple different layers of photoresist are utilized in a given masking/photolithographic step. Further, the photolithographic masking and patterning might be combined with one or more other layers. One such process forms what is
30 commonly referred to as a "hard mask" over the substrate prior to deposition of the photoresist layer or layers. The resist layer is then patterned, for example as described above, to form masking blocks over the hard mask. The hard mask is then etched using the photoresist as a mask to transfer the pattern of the photoresist to the hard mask. The resist may or may not be removed immediately thereafter. Hard masks such as just
35 described provide a more robust masking pattern than using resist alone, for example should the resist be completely eroded/etched away during an etch.

One material utilized as a hard mask is amorphous carbon. When etching oxide material using amorphous carbon as a hard mask, the etching typically removes the oxide at a rate of about ten times faster than it removes amorphous carbon.

Other masking methods exist in addition to photolithographic processing such as described above. For example, field effect transistors utilize a conductive gate which is typically received over a channel region of semiconductive material. Conductively doped source/drain semiconductive material regions are typically received on opposing sides of the channel region, with the gate overlying or underlying such channel region therebetween. In certain instances, it is desirable that the doping profile across the source/drain region be lighter/lower more proximate the channel region than distal therefrom. One method of processing for providing such dopant profile is to first form a desired conductive gate outline over the desired channel region of a semiconductor substrate. A suitable implant dose of a conductivity enhancing impurity can then be provided into the semiconductive material of the substrate, with the gate construction precluding such implant into the channel region. Then, an insulating layer can be conformally deposited over the gate construction and anisotropically etched to form insulative sidewall spacers over the gate. These sidewall spacers effectively function as a mask which both protects the sidewalls of the gate and precludes a subsequent implant from occurring beneath the spacers just formed. Accordingly, the sidewall spacers can be used as a mask for a subsequent higher dose source/drain implant to complete the formation of the outline of the desired source/drain regions.

While the invention was motivated in addressing the above issues, it is in no way so limited. The invention is only limited by the accompanying claims as literally worded (without interpretative or other limiting reference to the above background art description, remaining portions of the specification or the drawings).

SUMMARY

The invention includes masking methods. In one implementation, a masking material comprising boron doped amorphous carbon is formed over a feature formed on a semiconductor substrate. The masking material comprises at least about 0.5 atomic per cent boron. The masking material is substantially anisotropically etched effective to form an anisotropically etched sidewall spacer comprising the boron doped amorphous carbon on a sidewall of the feature. The substrate is then processed proximate the spacer while using the boron doped amorphous carbon comprising spacer as a mask. After processing the substrate proximate the spacer, the boron doped amorphous carbon comprising spacer is etched from the substrate.

Other aspects and implementations are contemplated.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the
5 following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment at a processing step in accordance with an aspect of the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that depicted by Fig. 1.

10 Fig. 3 is a view of the Fig. 2 wafer fragment at a processing step subsequent to that depicted by Fig. 2.

Fig. 4 is an alternate/addition to that depicted by Fig. 3.

Fig. 5 is another alternate/addition to that depicted by Fig. 3.

Fig. 6 is still another alternate/addition to that depicted by Fig. 3.

15 Fig. 7 is a view of the Fig. 3 wafer fragment at a processing step subsequent to that depicted by Fig. 3.

Fig. 8 is a view of the Fig. 7 wafer fragment at a processing step subsequent to that depicted by Fig. 7.

20 Fig. 9 is a diagrammatic sectional view of another semiconductor wafer fragment at a processing step in accordance with an aspect of the invention.

Fig. 10 is a view of the Fig. 9 wafer fragment at a processing step subsequent to that depicted by Fig. 9.

Fig. 11 is a view of the Fig. 10 wafer fragment at a processing step subsequent to that depicted by Fig. 10.

25 Fig. 12 is a view of the Fig. 11 wafer fragment at a processing step subsequent to that depicted by Fig. 11.

Fig. 13 is a diagrammatic sectional view of yet another semiconductor wafer fragment at a processing step in accordance with an aspect of the invention.

30 Fig. 14 is a view of the Fig. 13 wafer fragment at a processing step subsequent to that depicted by Fig. 13.

Fig. 15 is a view of the Fig. 14 wafer fragment at a processing step subsequent to that depicted by Fig. 14.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

35 Exemplary masking methods in accordance with the invention are initially described with reference to Figs. 1-8. Referring initially to Fig. 1, a semiconductor

substrate fragment is indicated generally with reference numeral 10. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or
5 in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Also in the context of this document, the term "layer" encompasses both the singular and the plural unless otherwise indicated.

10 In the depicted example, substrate 10 comprises a bulk monocrystalline silicon substrate 12. Some feature 14 is formed thereover. Any identifiable structural feature, whether existing or yet-to-be developed, is contemplated. By way of example only, examples include patterned photoresist layers, a partial or complete field effect transistor gate or other circuit construction, an etched region within a substrate, etc. By way of
15 example only, feature 14 in Fig. 1 is depicted as some form of patterned material formed over substrate 12. Such has a sidewall 16 which in the illustrated embodiment is substantially perpendicular in orientation relative to substrate 12. A masking material 18 comprising, consisting essentially of, or consisting of boron doped amorphous carbon is formed over feature 14. Such masking material comprises at least about 0.5 atomic
20 percent boron. An exemplary preferred embodiment includes a boron concentration from about 1.0 atomic per cent to about 16 atomic per cent. Alternate examples, by way of example only, include from 1.0 atomic per cent to 5.0 atomic per cent boron; from greater than 5.0 atomic per cent to 10.0 atomic per cent boron; from greater than 10.0 atomic per cent to 15.0 atomic per cent boron; from greater than 15.0 atomic per cent to 20.0
25 atomic per cent boron; and from greater than 20.0 atomic per cent to 75.0 atomic per cent boron.

In one exemplary embodiment, the feature might comprise amorphous carbon which is not doped with boron. In the context of this document "not doped with boron" would mean not having any detectable level of boron. If at least the outermost portions
30 of feature 14 were amorphous carbon not doped with boron, masking material 18 would be formed thereon (meaning in contact with) such amorphous carbon material.

One preferred example of forming boron doped amorphous carbon material 18 is by chemical vapor deposition (CVD), and which may or may not be plasma enhanced. Further, the boron doping might occur during or after the chemical vapor deposition. In
35 one exemplary preferred embodiment, the chemical vapor depositing uses at least one of C₂H₆, C₂H₄, C₂H₂, C₃H₆ and C₃H₈. Further in one preferred embodiment, the chemical

vapor depositing uses at least one of B_2H_6 , B_4H_{10} and BH_3CO , and thereby would form the amorphous carbon to be in situ boron doped as-deposited.

By way of example only, exemplary chemical vapor deposition tools include the Applied Materials Centura Processor and the Producer Processor available from Applied Materials of Santa Clara, California. Further and by way of example only, the following provides exemplary preferred methods of chemical vapor depositing material 18 utilizing such processors. One exemplary process gas is C_3H_6 at an exemplary flow rate of from 300 sccm to 900 sccm, with 600 sccm being a specific example. B_2H_6 is an exemplary boron source gas which can be flowed with the C_3H_6 , and at an exemplary flow rate of from 100 sccm to 2000 sccm depending on the flow rate of the other gases and depending on the desired boron concentration in the boron doped amorphous carbon layer being formed. Additional exemplary carrier or other reactive or non-reactive gases might also be utilized, for example, He and/or H_2 at from 0 sccm to 500 sccm. An exemplary preferred substrate temperature is from $400^\circ C$ to $650^\circ C$, with an exemplary preferred pressure range being from 3 Torr to 7 Torr. An exemplary preferred spacing from the wafer surface to a gas-emitting showerhead is from 190 mils to 240 mils. An exemplary preferred applied power range in a capacitively coupled, single electrode plasma deposition tool (such as those above) is from 100 watts to 800 watts for a 200mm wafer. Further by way of example only, exemplary non-plasma enhanced CVD parameters include a temperature of from about $500^\circ C$ to $800^\circ C$, pressure at from 50 mTorr to 200 mTorr, C_3H_6 flow at from 50 sccm to 1000 sccm, B_2H_6 flow at from 100 sccm to 2000 sccm, and with or without any He and/or H_2 .

The quantity of boron doping during the deposition has been determined to impact the degree of conformality of the deposition of material 18 over the steps of features. Generally speaking, the higher the boron concentration, the better the step coverage. For example within the above parameter ranges, a B_2H_6 to C_3H_6 volumetric flow rate ratio of 0.4 gave about 26% coverage over vertical steps as compared to horizontal surfaces, while a flow rate ratio of B_2H_6 to C_3H_6 of 2.1 provided 64% coverage over vertical steps as compared to horizontal surfaces. The 0.4 ratio provided an atomic boron concentration in the material 18 of about 3.0% boron, while the 2.1 flow ratio provided about 16% boron. RF power on the electrodes was determined to not be particularly impacting relative to conformality. In one exemplary reduction to practice example, step coverage of about 74% over vertical as compared to horizontal surfaces was achieved with a showerhead/wafer surface spacing of 215 mils, power at 250 watts, and precursor flow rates at 1250 sccm B_2H_6 , C_3H_6 at 650 sccm, substrate temperature of

550°C and chamber pressure of 5 Torr. High degree of conformality may or may not be desired depending on the application.

Referring to Fig. 2, masking material 18 has been substantially anisotropically etched effective to form an anisotropically etched sidewall spacer 20 comprising the boron doped amorphous carbon on sidewall 16 of feature 14. By way of example only, an exemplary process for anisotropically etching such material includes using a combination of CF₄ and/or other fluoride containing gases at from 5 sccm to 20 sccm, SO₂ at from 20 sccm to 60 sccm and O₂ at from 50 sccm to 120 sccm. An exemplary substrate temperature is from 5°C to 75°C, chamber pressure at from 5 mTorr to 15 mTorr, and source plasma power at from 150 to 250 Watts and bias power at from 30 to 100 Watts per 200mm of wafer diameter.

The boron doped amorphous carbon comprising spacer is next utilized as a mask while processing the substrate proximate said spacer. By way of example only, such processing of the substrate using the boron doped amorphous carbon comprising spacer as a mask could include any one or combination of ion implanting into the substrate, etching the substrate and depositing upon the substrate. For example, Fig. 3 depicts exemplary processing in the form of ion implantation to form a diffusion region 22. Fig. 4 depicts exemplary processing in the form of etching to form a recess or trench portion 24 relative to the substrate. Fig. 5 depicts by way of example a deposition process whereby a layer 26 is deposited over substrate 12, with boron doped amorphous carbon comprising spacer 20 serving as a mask to deposition of layer 26 immediately over substrate material 12 covered by spacer 20. Fig. 6 by way of example only depicts some form of selective deposition/processing to form a layer 28 over/from substrate material 12, with boron doped amorphous carbon comprising spacer 20 masking substrate material 12 therebeneath from such processing. By way of example only, such might constitute epitaxial silicon growth and/or thermal processing and/or other selective deposition/formation method whether existing or yet-to-be-developed.

After such processing of the substrate, the boron doped amorphous carbon comprising spacer is etched from the substrate. Fig. 7 depicts exemplary such processing subsequent to the processing depicted by Fig. 3. One most preferred process for etching the boron doped amorphous carbon comprising spacer uses an O₂ comprising plasma. By way of example only, an exemplary preferred process utilizes an O₂ ashing plasma chamber having a substrate temperature of from 300°C to 650°C, a substrate to showerhead spacing of from 400 mils to 800 mils, a pressure of from 4 Torr to 9 Torr, an O₂ gas flow of from 1000 sccm to 2500 sccm, and a plasma power range of from 200 watts to 1000 watts. Processing under such conditions can result in an

essentially isotropic etch of a 1500 Angstrom thick film of a boron doped amorphous carbon comprising spacer constituting 0.5% to 1.0% boron in about 75 seconds.

In conjunction with the above-described processing, it has been discovered that boron doping concentration provides a trade-off between step coverage and ease of isotropic O₂-only plasma etching. While higher boron concentration results in better step coverage, the higher the boron concentration, the more difficult it may be to O₂-only plasma etch such material from the substrate. As boron doping exceeds 10 atomic per cent, O₂-only plasma etching under the above-described conditions might be considered as becoming unacceptably low/slow. By way of example only, an etching gas comprising CF₄ will etch an amorphous carbon comprising spacer independent of the quantity of boron doping.

The capability of using an O₂ comprising plasma in etching a sacrificial spacer from a substrate may provide particular advantage as such etching can be conducted under the above conditions substantially selective to any of silicon dioxide, silicon nitride, monocrystalline silicon, and polycrystalline silicon. Such substantial selectivity in comparative etch rates is at least 2:1 of the boron doped amorphous carbon compared to any of silicon dioxide, silicon nitride, monocrystalline silicon and polycrystalline silicon. Accordingly, if there are any of such materials exposed on the substrate immediately before or during the etching of the sacrificial boron doped amorphous carbon comprising spacer from the substrate, such etching can advantageously be selective to any of such exposed materials.

Referring to Fig. 8, and in but one exemplary implementation, feature 14 (not shown) has also been etched from the substrate. Such could, of course, occur before or after etching boron doped amorphous carbon comprising spacer 20 from the substrate. Alternately, depending upon the structures being formed and perhaps the type of feature being formed, the feature might remain on the substrate for a time or constitute a part of the finished/final circuitry construction.

Alternate exemplary processing by way of example only is described with reference to Figs. 9-12. Fig. 9 depicts a substrate fragment 40 comprising semiconductive substrate material 42. A pair of gate constructions 44 and 46 are formed over substrate material 42. By way of example only, such comprise a gate oxide layer 48, a conductive polysilicon layer 50, a refractory metal or refractory metal silicide layer 52, and an insulative cap 54. Gate constructions 44 and 46 can be considered as a pair of adjacent features over which the above-described masking material can be formed and subsequently processed as described above. In one exemplary considered aspect, features 44 and 46 might be formed by photolithographic processing using a mask

having some minimum open dimension, for example, a dimension "A" corresponding to the separation distance between the closest walls of features 44 and 46. Dimension "A" might be slightly smaller or larger in the mask/reticle than the resultant dimension "A" between the structures shown on Fig. 9, for example depending on photolithographic processing aspects and/or aberrations. In one considered implementation, such minimum opening dimension (for example dimension "A") is ideally the smallest opening dimension utilized in any and all photolithographic processing of the semiconductor substrate before and after the masking method and methods being described herein. For example, the spacing achieved between the features 44 and 46 by photolithographic processing might be the smallest dimension technologically attainable in a production-capable process at the time of processing the substrate. Exemplary diffusion regions 58 have been formed relative to substrate 42.

Referring to Fig. 10, masking material 60 comprising boron doped amorphous carbon is formed over the illustrated features and substrate. Such material preferably has any of the same attributes as described above with respect to masking material 18 of the first described embodiments.

Referring to Fig. 11, masking material 60 has been substantially anisotropically etched effect to form pairs of spaced-adjacent anisotropically etched sidewall spacers 62 and sidewall spacers 64. Adjacent anisotropically etched sidewall spacers 62 are separated by a shortest distance "B" which is thereby less than the smallest opening dimension exemplified by dimension "A" in Fig. 9. Exemplary processing of the substrate proximate the spacers has been conducted in the form of implanting to form regions 66 and proximate the spacers.

Referring to Fig. 12 the boron doped amorphous carbon comprising spacers 62 and 64 have been etched from the substrate, for example, using the processing described above.

An alternate exemplary processing by way of example only is described with reference to Figs. 13-15. Fig. 13 depicts a substrate fragment 70 comprising semiconductive substrate material 72. A layer 74, for example a silicon dioxide, is formed over material 72. Another layer 76, for example amorphous carbon not doped with boron, is received over material 74. An opening 77, having walls 78, is formed through layer 76. Walls 78 can be considered as part of adjacent features of layer 76 which define at least some portion of opening 77. In one exemplary considered aspect, features 78 might be formed by photolithographic processing using a mask having some minimum open dimension, for example, a dimension "C" corresponding to the separation distance between the closest walls which define opening 77. As with dimension "A"

above, dimension "C" might be slightly smaller or larger in the mask/reticle than the resultant dimension "C" between the structures shown on Fig. 13, for example depending on photolithographic processing aspects and/or aberrations. In one considered implementation, such minimum opening dimension (for example dimension "C") is ideally the smallest opening dimension utilized in any and all photolithographic processing of the semiconductor substrate before and after the masking method and methods being described herein. For example, the spacing achieved between the features 78 by photolithographic processing might be the smallest dimension technologically attainable in a production-capable process at the time of processing the substrate.

A masking material 80 comprising boron doped amorphous carbon is formed over the illustrated features and substrate. Such material preferably has any of the same attributes as described above with respect to masking material 18 of the first described embodiments.

Referring to Fig. 14, masking material 80 has been substantially anisotropically etched effective to form pairs of spaced-adjacent anisotropically etched sidewall spacers 82. Adjacent anisotropically etched sidewall spacers 82 are separated by a shortest distance "D" which is thereby less than the smallest opening dimension exemplified by dimension "C" in Fig. 13. Exemplary processing of the substrate proximate the spacers has been conducted in the form of etching of layer 74 to form an opening 84 to substrate material 72 proximate spacers 82.

Referring to Fig. 15 the boron doped amorphous carbon comprising spacers 82 been etched from the substrate, for example, using the processing described above.

U.S. Patent Application Serial Number 10/463,185 filed on June 17, 2003, entitled "Boron-Doped Amorphous Carbon Film For Use As A Hard Etch Mask During The Formation Of A Semiconductor Device", naming Zhiping Yin and Gurtej Sandhu as inventors, is hereby incorporated by reference.

CLAIMS

What is claimed is:

1. A masking method comprising:
 - 5 forming a masking material comprising boron doped amorphous carbon over a feature formed on a semiconductor substrate, the masking material comprising at least about 0.5 atomic per cent boron;
substantially anisotropically etching the masking material effective to form an anisotropically etched sidewall spacer comprising the boron doped amorphous carbon on
10 a sidewall of the feature;
using the boron doped amorphous carbon comprising spacer as a mask while processing the substrate proximate the spacer; and
after said processing of the substrate, etching the boron doped amorphous carbon comprising spacer from the substrate.
- 15 2. The method of claim 1 wherein the feature over which the masking material is formed comprises amorphous carbon which is not doped with boron.
3. The method of claim 2 wherein the masking material is formed on the
20 amorphous carbon which is not doped with boron.
4. The method of claim 1 wherein the masking material is formed over a pair of adjacent features, the substantially anisotropically etching being effective to form a pair of spaced, adjacent anisotropically etched sidewall spacers.
- 25 5. The method of claim 4 wherein,
the adjacent features are formed by photolithographic processing using a mask having a minimum opening dimension; said minimum opening dimension being the smallest opening dimension utilized in any and all photolithographic processing of the
30 semiconductor substrate before and after said masking method; and
the adjacent anisotropically etched sidewall spacers are separated by a shortest distance, the shortest distance being less than the smallest opening dimension.
6. The method of claim 1 wherein the masking material consists essentially
35 of boron doped amorphous carbon.

7. The method of claim 1 wherein the masking material consists of boron doped amorphous carbon.
8. The method of claim 1 wherein the forming comprises CVD.
9. The method of claim 8 wherein the CVD is plasma enhanced.
10. The method of claim 8 wherein the CVD is not plasma enhanced.
11. The method of claim 8 wherein boron doping occurs during the CVD.
12. The method of claim 8 wherein boron doping occurs after the CVD.
13. The method of claim 1 wherein the forming comprises CVD using at least one of C_2H_6 , C_2H_4 , C_2H_2 , C_3H_6 , and C_3H_8 ; and using at least one of B_2H_6 , B_4H_{10} and BH_3CO .
14. The method of claim 13 wherein the CVD is plasma enhanced.
15. The method of claim 13 wherein the CVD is not plasma enhanced.
16. The method of claim 1 wherein the feature sidewall is substantially perpendicular to the substrate.
17. The method of claim 1 wherein the masking material comprises from 1.0 atomic per cent to 5.0 atomic per cent boron.
18. The method of claim 1 wherein the masking material comprises from greater than 5.0 atomic per cent to 10.0 atomic per cent boron.
19. The method of claim 1 wherein the masking material comprises from greater than 10.0 atomic per cent to 15.0 atomic per cent boron.
20. The method of claim 1 wherein the masking material comprises from greater than 15.0 atomic per cent to 20.0 atomic per cent boron.

21. The method of claim 1 wherein the masking material comprises from greater than 20.0 atomic per cent to 75.0 atomic per cent boron.

22. The method of claim 1 wherein the processing of the substrate using the boron doped amorphous carbon comprising spacer as a mask comprises etching the substrate.

23. The method of claim 1 wherein the processing of the substrate using the boron doped amorphous carbon comprising spacer as a mask comprises ion implanting into the substrate.

24. The method of claim 1 wherein the processing of the substrate using the boron doped amorphous carbon comprising spacer as a mask comprises a deposition upon the substrate.

25. The method of claim 1 wherein the etching is with an O₂ comprising plasma.

26. The method of claim 1 further comprising after said processing of the substrate, etching the feature from the substrate.

27. The method of claim 26 wherein said feature is etched from the substrate after the boron doped amorphous carbon comprising spacer is etched from the substrate.

28. A masking method comprising:

chemical vapor depositing a masking material comprising boron doped amorphous carbon over a feature formed on a semiconductor substrate, the masking material comprising from about 1.0 atomic per cent to about 20 atomic per cent boron;

substantially anisotropically etching the masking material effective to form an anisotropically etched sidewall spacer comprising the boron doped amorphous carbon on a sidewall of the feature;

using the boron doped amorphous carbon comprising spacer as a mask while processing the substrate proximate the spacer; and

after said processing of the substrate, etching the boron doped amorphous carbon comprising spacer from the substrate using an O₂ comprising plasma

substantially selective to at least one of exposed silicon dioxide, silicon nitride and silicon.

29. The method of claim 28 wherein the feature over which the masking
5 material is formed comprises amorphous carbon which is not doped with boron.

30. The method of claim 29 wherein the masking material is formed on the amorphous carbon which is not doped with boron.

10 31. The method of claim 28 wherein the masking material is formed over a pair of adjacent features, the substantially anisotropically etching being effective to form a pair of spaced, adjacent anisotropically etched sidewall spacers.

32. The method of claim 31 wherein,
15 the adjacent features are formed by photolithographic processing using a mask having a minimum opening dimension; said minimum opening dimension being the smallest opening dimension utilized in any and all photolithographic processing of the semiconductor substrate before and after said masking method; and
the adjacent anisotropically etched sidewall spacers are separated by a shortest
20 distance, the shortest distance being less than the smallest opening dimension.

33. The method of claim 28 wherein the masking material consists essentially of boron doped amorphous carbon.

25 34. The method of claim 28 wherein the CVD is plasma enhanced.

35. The method of claim 28 wherein the CVD is not plasma enhanced.

36. The method of claim 28 wherein boron doping occurs during the CVD.
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37. The method of claim 28 wherein boron doping occurs after the CVD.

38. The method of claim 28 wherein the chemical vapor depositing uses at least one of C_2H_6 , C_2H_4 , C_2H_2 , C_3H_6 , and C_3H_8 ; and uses at least one of B_2H_6 , B_4H_{10} and BH_3CO .
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39. The method of claim 28 wherein the feature sidewall is substantially perpendicular to the substrate.

40. The method of claim 28 wherein the processing of the substrate using the boron doped amorphous carbon comprising spacer as a mask comprises etching the substrate.

41. The method of claim 28 wherein the processing of the substrate using the boron doped amorphous carbon comprising spacer as a mask comprises ion implanting into the substrate.

42. The method of claim 28 wherein the processing of the substrate using the boron doped amorphous carbon comprising spacer as a mask comprises a deposition upon the substrate.

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43. The method of claim 28 further comprising after said processing of the substrate, etching the feature from the substrate.

44. The method of claim 43 wherein said feature is etched from the substrate after the boron doped amorphous carbon comprising spacer is etched from the substrate.

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