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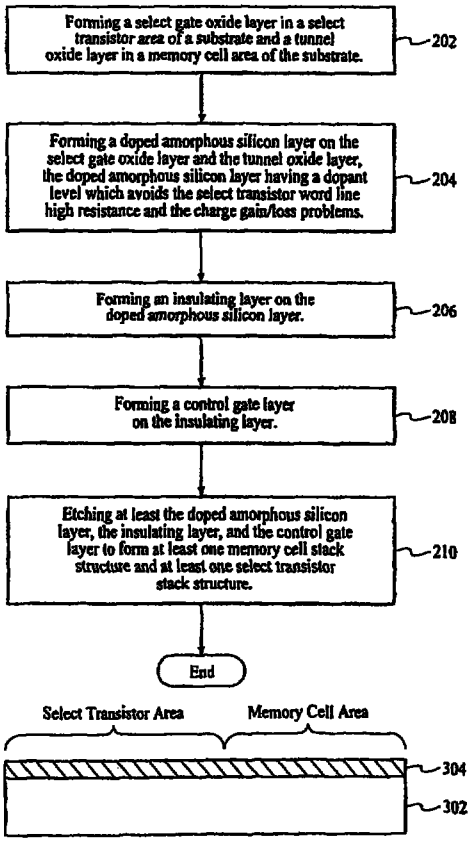
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(54) Title: METHOD FOR PROVIDING A DOPANT LEVEL FOR POLYSILICON FOR FLASH MEMORY DEVICES



(57) Abstract: The present invention provides a method and a NAND-type flash memory device. The method includes forming a select gate oxide layer in a select transistor area of a substrate and a tunnel oxide layer in a memory cell area of the substrate; forming a doped amorphous silicon layer on the select gate oxide layer and the tunnel oxide layer, the doped amorphous silicon layer having a dopant level which simultaneously avoids a select transistor word line high resistance problem and a charge gain/charge loss problem; forming an insulating layer on the doped amorphous silicon layer; forming a control gate layer on the insulating layer; and etching at least the doped amorphous silicon layer, the insulating layer, and the control gate layer to form at least one memory cell stack structure and at least one select transistor stack structure. In a preferred embodiment, the polysilicon layer which forms both the floating gate of the flash memory cell and the select gate of the select transistor of the device is doped with between approximately 5×10^{18} and 8×10^{19} ions/cm^3 of phosphorus. With this dopant level, the contact resistance of the select transistor's control gate is low, thus keeping the word line resistivity of the device low. Simultaneously, contamination of the tunnel oxide of the flash memory cell by the dopant is limited, allowing for the interface between the floating gate and the tunnel oxide to be smooth, which prevents charge gain/loss problems. Thus, the reliability of the device is increased.

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