

METHOD AND SYSTEM FOR MANAGING AN EXPRESS TRAVERSAL OF FLITS IN A NETWORK ON CHIP

Field of the Invention

This invention relates to a system and method for Network on a Chip (NoC). More particularly, this invention relates to a method and a system for managing an express traversal of flits in a network on chip.

Background

The number of processing elements in computer systems continues to increase at an exponential rate as the demand for faster and more powerful processing systems increases. As such, those skilled in the art have been focusing their efforts on coming up with communication solutions that may be scaled for large scale processing core counts while maintaining low communication latency between cores. Some solutions that have been proposed involve the use of interconnecting networks as a replacement for conventional methods such as shared buses and various communal wiring solutions. A solution that is commonly used in the art is a network-on-a-chip solution whereby multiple processing cores on a single chip are connected to one another using various two or three dimensional mesh topologies whereby point-to-point links connect a processing core with an adjacent core.

In a network-on-chip, data is often sent as packets whereby each packet typically comprises a head flit, body flits and a tail flit. As the names suggest, the head flit is the header of the data packet, the body flits make up the middle portions of the data packet while the tail flit indicates to a transmitting or receiving processing core that the entirety of

the data packet has been sent or received. Network-on-chips typically utilize shared links to transfer flits between its source and destination whereby each processing core would have its own router for routing flits between intermediate processing cores on the chip. These routers perform the multiplexing of flits on the links and when a conflict of flits occurs at a router, the router will cause flits to be buffered. In such a solution, each flit must typically traverse through multiple processing cores en-route to its final destination. This results in the accumulation of significant start-to-end latency issues that occur due to traversal overheads between processing cores.

A network on a chip solution that has been proposed by T.Krishna et al. in their paper titled "Breaking the On-Chip Latency Barrier Using SMART" published in the 2013 IEEE 19th International Symposium on High Performance Computer Architecture (HPCA2013) involves the embedding of asynchronous repeaters within each router's cross bar and sizing these repeaters up to drive signals up to multiple hops. It should be noted that a hop consists of a router-and-link traversal. In their work, each router in each processing core is configured to perform the followings actions: (1) Buffer Write Action– In this action, an incoming flit is buffered; (2) Route Compute Action – In this action, an incoming head flit chooses an output port to depart from; (3) Switch Allocation Local (SA-L) – In this action, buffered flits arbitrate among themselves for the crossbar switch and at the end of this action, there is only one winner flit for every input and output part of the crossbar; (4) Smart-hop Setup Request (SSR) and Switch Allocation Global (SA-G) – In this action, the winner flit at each output port will broadcast a SSR up to the required number of hops from that output port which the winning flit wishes to go to, and during SA-G, all intermediate routers arbitrate among the SSRs received to determine which flits are to be buffered (BWena set to high or low), which flits have access to the crossbar (BMsel set to either bypass or local) and which input and output ports of the crossbar are to be selected (XBsel); (5) Virtual Chanel (VC) Selection (VS)

Stage – In this action, head flits that win SA-L or SA-G reserve a VC of the next router from a pool of free VCs; and (6) Switch Traversal (ST) and Link Traversal (LT) Actions – In these actions, the winner flits from the SA-L and SA-G actions traverses the crossbars of each router to reach their destinations.

It should be noted that in the existing SMART network on a chip solution described above, a downstream router will issue a Virtual Channel (VC) credit to an adjacent upstream router when an entire VC is free or available. This VC credit is then sent to the adjacent upstream router via a credit wire connected between these two routers. As certain applications require larger data packets, the VC buffer size of each router has to be increased to accommodate the entirety of these larger data packets thereby rendering such routers impractical for network-on-chip solutions.

For the above reasons, those skilled in the art are constantly striving to come up with a system and method for improving the management of virtual credits in a NoC solution.

Summary of the Invention

The above and other problems are solved and an advance in the art is made by systems and methods provided by embodiments in accordance with the invention.

A first advantage of embodiments of systems and methods in accordance with the invention is that in this invention, routers in an EXTRA NoC communication solution are configured to track virtual channels at downstream routers with much finer granularity, i.e. at a flit level. In particular, an upstream router will be aware of the exact number of flits that may be received by a Virtual Channel (VC) in an adjacent downstream router. As such, the allocated VC at the downstream router need not be sized to receive the entirety of a packet

that is to be transmitted from an adjacent upstream router. This effectively reduces the buffer sizes of Virtual Channels in the routers of this proposed solution.

A second advantage of embodiments of systems and methods in accordance with the invention is that as two groups of wires are used to transfer the two types of VC credits to upstream routers, extra credit latency delays are decreased.

According to a first aspect of the invention, the method for managing an express traversal of flits in a network on chip comprises the steps of determining and allocating, during a first cycle, using a first router, a free virtual channel of a second router, and updating a VCMAP table of the first router with an identity of the allocated virtual channel of the second router, wherein the second router is downstream of the first router; determining and allocating, during a second cycle, using the second router, a free virtual channel of a third router, and updating a VCMAP table of the second router with an identity of the allocated virtual channel of the third router, wherein the third router is downstream of the second router; in response to allocating the free virtual channel of the second router, during a third cycle, delivering a first flit from the first router to the second router and informing the second router of the identity of the allocated virtual channel of the second router using a dedicated wire connecting the first and second routers, and in response to allocating the free virtual channel of the third router, during the third cycle, delivering the first flit from the second router to the third router and informing the third router of the identity of the allocated virtual channel of the third router using a dedicated wire connecting the second and third routers.

With reference to the first aspect, in a first possible implementation manner of the first aspect, wherein the determining and the allocating the free virtual channel of the second router comprises the steps of selecting, using the first router, a virtual channel of the second

router from a FreeVC table provided at the first router; determining if the selected virtual channel has credit; and in response to determining that the selected virtual channel has credit, allocating the selected virtual channel as the free virtual channel of the second router for receiving a flit from the first router.

With reference to the first aspect or the first possible implementation manner of the first aspect, in a second possible implementation manner of the first aspect, wherein the determining and the allocating the free virtual channel of the third router comprises the steps of selecting, using the second router, a virtual channel of the third router from a FreeVC table provided at the second router; determining if the selected virtual channel has credit; and in response to determining that the selected virtual channel has credit, allocating the selected virtual channel as the free virtual channel of the third router for receiving a flit from the second router.

With reference to the first aspect or the first or second possible implementation manners of the first aspect, in a third possible implementation manner of the first aspect wherein the updating of the VCMap table of the first router comprises the steps of adding the identity of the allocated virtual channel of the second router as an entry to the VCMap table; and associating the entry with an identity of the first router and an identity of a virtual network of the second router, wherein the allocated virtual channel is a part of the virtual network.

With reference to the first aspect or the first or second or third possible implementation manners of the first aspect, in a fourth possible implementation manner of the first aspect, wherein the updating of the VCMap table of the second router comprises the steps of adding the identity of the allocated virtual channel of the third router as an entry to the VCMap table; and associating the entry with an identity of the first router and an identity

of a virtual network of the third router, wherein the allocated virtual channel is a part of the virtual network.

With reference to the first aspect or the first or second or third or fourth possible implementation manners of the first aspect, in a fifth possible implementation manner of the first aspect, wherein the delivering the first flit from the first router to the second router comprises bypassing the allocated virtual channel of the second router.

With reference to the fifth possible implementation manner of the first aspect, in a sixth possible implementation manner of the first aspect, wherein the bypassing the allocated virtual channel of the second router further comprises generating a credit associated with the virtual channel of the second router; and providing the generated credit to the first router.

With reference to the sixth possible implementation manner of the first aspect, in a seventh possible implementation manner of the first aspect, wherein the generated credit is provided to the first router using a dedicated result wire provided between the first router and the second router.

With reference to the seventh possible implementation manner of the first aspect, in an eighth possible implementation manner of the first aspect, wherein the generated credit comprises a Switch Allocation Global (SA-G) action result.

With reference to the first aspect or any one of the first to sixth possible implementation manners of the first aspect, in a ninth possible implementation manner of the first aspect, wherein a dedicated result wire is provided between the first router and the second router, and between the second router and the third router.

According to a second aspect of the invention, a system for managing an express traversal of flits in a network on chip comprises a first router configured to, during a first cycle, determine and allocate a free virtual channel of a second router, and update a VCMaP table of the first router with an identity of the allocated virtual channel of the second router, wherein the second router is downstream of the first router; a second router configured to, during a second cycle, determine and allocate a free virtual channel of a third router, and update a VCMaP table of the second router with an identity of the allocated virtual channel of the third router, wherein the third router is downstream of the second router; in response to allocating the free virtual channel of the second router, the first router is configured to, during a third cycle, deliver a first flit from the first router to the second router and to inform the second router of the identity of the allocated virtual channel of the second router using a dedicated wire connecting the first and second routers, in response to allocating the free virtual channel of the third router, the second router is configured to, during the third cycle, deliver the first flit from the second router to the third router and to inform the third router of the identity of the allocated virtual channel of the third router using a dedicated wire connecting the second and third routers.

With reference to the second aspect, in a first possible implementation manner of the second aspect, wherein when determining and allocating the free virtual channel of the second router, the first router is further configured to select a virtual channel of the second router from a FreeVC table provided at the first router; determine if the selected virtual channel has credit; and in response to determining that the selected virtual channel has credit, to allocate the selected virtual channel as the free virtual channel of the second router for receiving a flit from the first router.

With reference to the second aspect or the first possible implementation manner of the second aspect, in a second possible implementation manner of the second aspect,

wherein when determining and allocating the free virtual channel of the third router, the second router is further configured to select a virtual channel of the third router from a FreeVC table provided at the second router; determine if the selected virtual channel has credit; and in response to determining that the selected virtual channel has credit, to allocate the selected virtual channel as the free virtual channel of the third router for receiving a flit from the second router.

With reference to the second aspect or the first or second possible implementation manners of the second aspect, in a third possible implementation manner of the second aspect, wherein when updating the VCMap table of the first router, the first router is further configured to add the identity of the allocated virtual channel of the second router as an entry to the VCMap table; and associate the entry with an identity of the first router and an identity of a virtual network of the second router, wherein the allocated virtual channel is a part of the virtual network.

With reference to the second aspect or the first or second or third possible implementation manners of the second aspect, in a fourth possible implementation manner of the second aspect, when updating the VCMap table of the second router, the second router is further configured to add the identity of the allocated virtual channel of the third router as an entry to the VCMap table; and associate the entry with an identity of the first router and an identity of a virtual network of the third router, wherein the allocated virtual channel is a part of the virtual network.

With reference to the second aspect or the first or second or third or fourth possible implementation manners of the second aspect, in a fifth possible implementation manner of the second aspect, wherein when delivering the first flit from the first router to the second

router, the second router is further configured to bypass the allocated virtual channel of the second router.

With reference to the fifth possible implementation manner of the second aspect, in a sixth possible implementation manner of the second aspect, wherein when the allocated virtual channel of the second router is bypassed, the second router is further configured to generate a credit associated with the virtual channel of the second router; and provide the generated credit to the first router.

With reference to the sixth possible implementation manner of the second aspect, in a seventh possible implementation manner of the second aspect, the generated credit is provided to the first router using a dedicated result wire provided between the first router and the second router.

With reference to the seventh possible implementation manner of the second aspect, in an eighth possible implementation manner of the second aspect, the generated credit comprises a Switch Allocation Global (SA-G) action result.

With reference to the second aspect or any one of the first to sixth possible implementation manners of the second aspect, in a ninth possible implementation manner of the first aspect, a dedicated result wire is provided between the first router and the second router, and between the second router and the third router.

Brief Description of the Drawings

The above advantages and features in accordance with this invention are described in the following detailed description and are shown in the following drawings:

Figure 1 illustrating a one-dimensional mesh topology for implementing a single-cycle multiple-hop asynchronous repeated traversal in a network-on-a-chip in accordance with embodiments of the invention;

Figure 2 illustrating a block diagram of modules contained within a router of a processing core, the modules being configured to implement the virtual channel allocation and virtual channel credit generation in accordance with embodiments of the invention;

Figure 3a illustrating a plurality of point-to-point interconnects between each processing core in a one-dimensional mesh topology for VC allocations, and VC credit generations and/or consumptions in accordance with embodiments of the invention;

Figure 3b illustrating a plurality of point-to-point interconnects between each processing core in a one-dimensional mesh topology for an optimized VC credit mechanism in accordance with embodiments of the invention;

Figure 4 illustrating processing cores configured to transfer a flit from an injector router to a destination router in accordance with embodiments of the invention;

Figure 5 illustrating a flow diagram of a process for the allocation of a virtual channel in a downstream router whereby the allocation takes place in an upstream router in accordance with embodiments of the invention;

Figure 6 illustrating a flow diagram of a process for transferring a flit from an injector router to a destination router by bypassing an intermediate router in accordance with embodiments of the invention; and

Figure 7 illustrating a flow diagram of a process for transferring a flit from an injector router to a destination router wherein the flit is buffered at an intermediate router before

reaching the destination router at a subsequent cycle in accordance with embodiments of the invention.

Detailed Description of the Embodiments

This invention relates to a system and method for managing and optimizing the generation and transfer of virtual channel credits in an Express Traversal (EXTRA) network on a chip (NoC). More particularly, this invention relates to a system and method whereby an upstream router manages the allocation of flit-slots within a virtual channel of a downstream router. A flit-slot comprises a storage slot or space within a virtual channel whereby each flit-slot is sized and configured to receive and store a flit of data. Each pre-allocated flit-slot within this pre-allocated virtual channel may subsequently be used to receive a flit of data from the upstream router. Prior to the transmission of the flits from the upstream router, the downstream router will be informed in advance about the allocation of its virtual channel and/or its flit-slots in the allocated virtual channel. Furthermore, each downstream processing core may be configured to bypass incoming flits as required thereby allowing flits to hop across multiple processing cores in a single cycle before the data is buffered.

Figure 1 illustrates processor 100 that employs a one-dimensional EXTRA NoC topology in accordance with embodiments of the invention. For brevity, in this description, features of this invention will only be described with reference to the implementation of the one-dimensional topology. One skilled in the art will recognize that the processing cores, e.g. processors 110-112 may also be arranged in a two-dimensional EXTRA NoC configuration (e.g. X columns with Y rows) without departing from this invention.

Processor 100 may comprise of a plurality of processing cores, i.e. processors 110-112, whereby each processing core may be connected to a neighbouring or adjacent

processing core via a plurality of links. One skilled in the art will recognize that the term processing core refers to any processing element within a chip such as an independent processor or a node of an on-chip network. Processes provided by instructions stored in a non-transitory computer-readable media may be executed by these processing cores. The instructions may be stored as firmware, hardware, or software. For the avoidance of doubt, non-transitory computer-readable media shall be taken to comprise all computer-readable media except for a transitory, propagating signal.

Each processing core is provided with a router, whereby each router performs a variety of routing functions or actions at various time-cycles to ensure that a packet gets delivered safely from an injector router to its destination router. Each router is also provided with input buffers 130 that may be used to store virtual networks or virtual channels. Each router in processor 100 may communicate with a neighbouring downstream router (belonging to a neighbouring downstream processor core) by transmitting data packet 106 to the neighbouring router via downstream link 102. Downstream link 102 is configured to transfer data or information in a downstream direction, i.e. from router 120 to 121 or router 121 to router 122. In embodiments of the invention, data packet 106 may be broken down into multiple flits. Contained within each of data packet 106 would be the payload data, i.e. the body flits, and the routing data, i.e. the head and tail flits. If data packet 106 were to be transmitted from router 120 to router 122, the data packet would have to traverse an intermediate processing core, i.e. router 121, before reaching its destination.

In embodiments of the invention, depending on the time-cycle or the action being carried out by the router, each router may perform the actions of: storing a received packet in its input buffer; allocating a virtual channel on a neighbouring downstream router for a received head-flit; allocating a flit-slot in the allocated virtual channel on the neighbouring downstream router for a received body-flit; bypassing a received flit by allocating a crossbar

switch of a router to the received flit and/or forwarding a buffered or received flit across a determined link. Figure 1 also illustrates upstream link 104. Upstream link 104 is configured to transfer data or information from a downstream router to an upstream router, e.g. from router 122 to router 121 or router 121 to router 120.

Figure 2 illustrates a block diagram showing modules that may be contained within router 200 whereby router 200 is an exemplary router of a processing core in accordance with embodiments of the invention. The modules illustrated in Figure 2 are configured to implement a virtual channel allocation and a virtual channel credit generation in accordance with embodiments of the invention. In Figure 2, router 200 is illustrated as having downstream links comprising data wire 202 and Virtual Channel (VC) identifier wire 204; and upstream links comprising credit wire 206 and SA-G result wire 208. SA-G result wire 208 may be included or may be omitted in accordance with embodiments of the invention. The detailed functions of these downstream and upstream links will be discussed in greater detail below with reference to Figure 3.

Input buffers 210 are provided within router 200 for storing data packets received via data wire 202. As illustrated in Figure 2, groups of virtual channels may be stored as Virtual Networks (VNETs) in each router. In particular, virtual network VNet 211 is illustrated as having a group of virtual channels 215a, 215b and 215c while virtual network VNet 21 is illustrated as having a group of virtual channels 216a, 216b and 216c. Each of these virtual channels may be utilized to store a plurality of flits. For example, virtual channel 215a is illustrated as having three flit-slots. As virtual channel 215a has three flit slots, this means that virtual channel 215a is able to store up to three flits. In embodiments of the invention, before an upstream router sends a head-flit to a downstream router, the upstream router has to ensure that a downstream router has an available virtual channel to receive or handle the data packet before the head-flit may be sent. In a similar context, before an upstream router

sends a body-flit to a downstream router, the upstream router has to ensure that a virtual channel allocated at a downstream router has sufficient available flit-slots to receive or handle the data before the body-flit may be sent.

As illustrated in Figure 2, router 200 is illustrated as having VC map module 220, free VC module 225, Credit Counter Module 226, VC selection module 250, buffer write module 255, switch allocation local (SA-L) module 265, switch allocation global (SA-G) module 270 and crossbar switch 275. These modules and components perform actions during various time cycles (simplified as “cycles”) to send a flit from a source router to a destination router. In accordance with embodiments of the invention, the following actions may be performed by the respective modules and components:

- 1) VC Map Module (220) – This module maintains a VCMap table that shows the association between the identity of an injector router, the virtual network associated with the flits of a particular packet and the selected virtual channel's identity.
- 2) Free VC Module (225) – This module maintains a table that sets out the number of free VCs in an adjacent router.
- 3) Credit Counter Module (226) – This module maintains a credit counter which tracks the credit count of each VC (i.e. the number of free flit-slots for each VC) at an adjacent downstream router.
- 4) VC Selection Module (250) – Head flits that win a local or global arbitration, i.e. a SA-L or a SA-G, cause VC selection module 250 to allocate or pre-allocate a Virtual Channel (VC) from a downstream router from the table contained in Free VC module 225. VC selection module 250 also updates the table maintained in VC map module 220 with the identity of the allocated virtual channel and the corresponding virtual network.

- 5) Buffer Write Module (255) – This module causes an incoming flit to be buffered.
- 6) Switch Allocation-Local Module (260) – This module causes buffered flits in router 200 to arbitrate among themselves for a winner flit whereby the winner flit is granted access to an input of crossbar switch 275.
- 7) Switch Allocation-Global Module (265) – This module causes winner flits at each output port of each router to broadcast a Smart-hop Setup Request (SSR) up to the require number of hops which the winning flit wishes to go to. This module then arbitrates the received SSR to determine which winner flits are to be buffered (BWena set to high or low), which flits have access to the respective crossbars (BMsel set to either bypass or local) and which input and output ports of the respective crossbars are to be selected (XBsel). The BWena, BMsel and XBsel logics utilized in this inventon are similar to that used in existing SMART NOC communication solutions as such; these operations of these logics will not be discussed in detail.

Figure 3a illustrates an implementation of a Port-to-Port VC credit management scheme that utilizes a one-dimensional mesh topology comprising routers 310, 311, and 312 for VC allocations, and VC credit generations and/or consumptions in accordance with an embodiment of the invention. As illustrated, router 310 has virtual channels 310a and 310b which each have three flit-slots respectively, e.g. VC ID 310a has flit-slots A1, A2 and A3 while VC ID 310b has flit-slots B1, B2 and B3, router 311 has virtual channels 311a and 310b while router 312 has virtual channels 312a and 312b with their respective flit-slots. Figure 3a also illustrates SSR pipelines 302, 303 which are used to broadcast the Smart-hop Setup Request (SSR) from the SA-G module contained within each router to downstream routers. As illustrated, SSR pipelines 302 connect router 310 to downstream routers 311 and 312 while SSR pipelines 303 connect router 311 to downstream router 312 and beyond.

Although Figure 3a only illustrates two sets of SSR pipelines being utilized, one skilled in the art will recognize that any number of sets of SSR pipelines may be included depending on the number-n of routers that are utilized in a processor.

Each of the routers 310, 311 and 312 are illustrated as having downstream links comprising data wire 202 and Virtual Channel (VC) identifier wire 204; and an upstream link comprising credit wire 206. Credit wire 206 is utilized to transfer a local VC credit or a global VC credit from a downstream router to an upstream router. It should be noted that in this Port-to-Port VC credit management scheme embodiment, all the virtual networks having the same port number will share the same group of credit wires. The generation and transfers of local and global VC credits are described in greater detail in the following sections.

Signal	VNet Identity	Virtual Channel Identity	Credit Type (optional)
Width(bits)	$\text{Log}_2(\#\text{VNet})$	$\text{Log}_2(\#\text{VC_Per_VNet})$	(1), (2) or (3)

Table 1

Table 1 above shows the format of a local or global VC credit whereby #VNet represents the number of virtual networks in a particular router and #VC_Per_VNet represents the number of virtual channels in the virtual network. The credit type of the VC credit may be selected from the following types: (1) FreeVCOnly type – which informs about availability of free VCs; (2) FreeVCAndCredit type – which represents a free VC action and credit and (3) FreeCreditOnly type – which represents a free credit action only. It should be noted that the Credit Type field is optional and may be included or excluded from the format of the local or global VC credit. The generation and consumption of the different types of credits will be described in detail below.

Figure 3a also illustrates timing diagram 350 which shows the various functions/actions that are carried out by the various modules of each router during each cycle in relation to flits 1, 2 and 3. For this timing diagram, the VC Selection (VS), Buffer Write (BW), Switch Allocation-Local (SA-L), SSR transmission (SSR), Switch Allocation-Global (SA-G), Switch Traversal (ST) and Link Traversal (LT) actions having the superscript “1” refers to actions/functions carried out in relation to a first (1st) flit, actions having the superscript “2” refers to actions/functions carried out in relation to a second (2nd) flit, and actions having the superscript “3” refers to actions/functions carried out in relation to a third (3rd) flit. One skilled in the art will recognize that although only three (3) flits are utilized in this timing diagram, the actual implementation of the invention may involve any number of flits as required. The respective actions then repeat continuously with cycle-1, cycle-2, cycle-3, cycle-1, etc. For completeness, it should be noted that the winner flits from the SA-L and SA-G actions traverse the crossbar switches of each router to reach their destinations during the ST and LT actions.

In embodiments of the invention, during the first cycle-1, the BW module in routers 310, 311 and 312 will carry out the BW action to buffer any incoming flits. Each of these routers will then perform SA-L to determine which buffered flit becomes a winner flit for each router.

For each router, before a buffered flit may become a winner flit, the affected router will check a table contained in its Free VC module to determine whether there are any free VCs in an adjacent downstream router (i.e. VC's with free input buffers). If it is determined that there are free VCs, the buffered flit is then allowed to become the winner flit. If the winner flit of a router is a head flit, the affected router will then allocate a free VC of a downstream router by tagging a VC ID of a free VC to the head flit. The identity of the allocated VC, e.g. the VC ID, will also be updated to a table maintained in the VC Map

module of the affected router. In addition to the above, the identity of the allocated VC will also be transmitted to the adjacent downstream router together with the winner flit to inform the adjacent downstream router of the allocation of its VC.

Similarly for each router, before a buffered body or tail flit may become a winner flit, the affected router will check its Credit Counter module to determine if a VC ID that had previously been allocated to a head flit associated with the body or tail flit has any free credits, i.e. whether the associated allocated VC of the downstream router has available flit-slots to receive the body or tail flit. If the router determines from its Credit Counter module that the allocated VC does have free credits, the buffered body or tail flit may then become a winner flit. If the winner flit of a router is a body or tail flit, the affected router will check a table maintained in the VC Map module to retrieve a VC ID that had previously been allocated to a head flit associated with the body or tail flit. The router will then allocate the retrieved VC ID to the body or tail flit. The identity of the allocated VC will then be transmitted to the adjacent downstream router together with the winner flit to inform the adjacent downstream router of the VC that is to be utilized.

For each router, a local VC credit will also be generated for the virtual channel (VC) of the winning flit during the SA-L action after the winning flit has been determined for a router. If the generated local VC credit utilizes the “credit type” field in its format and when the winning flit is a tail flit, a FreeVCandCredit type of local VC credit will be created and if the winning flit is a head or body flit, a FreeCreditOnly type of local VC credit will be created. Alternatively, the “credit type” field may be omitted from the format of the generated local VC credit. Regardless whether the credit type is utilized or not, the generated local VC credit is then transmitted to an adjacent upstream router via credit wire 206 during the next cycle, because a local VC credit and a global VC credit cannot be transferred at the same cycle.

This local VC credit will then be used to update a credit counter at the free VC module of the upstream router.

During cycle-2, the generated local VC credit is transmitted to an adjacent upstream router via credit wire 206. SSRs are also broadcasted using the SSR pipelines to each respective router. Each of these routers will then perform SA-G and arbitrate among the SSRs received to determine which routers are to perform the bypassing action (i.e. an input flit becomes the winning flit, whereby the input flit bypasses the router) and which routers are to perform the buffering function (i.e. a buffered flit becomes the winning flit, whereby the input flit is buffered by the router). The winner flit of a SA-G action at a router may either be a buffered flit at the router, or a flit at the input of the router.

For each router, before a head flit may become a winner flit during the SA-G action, an affected router will check a table contained in its Free VC module to determine whether there are any free VCs in an adjacent downstream router (i.e. VC's with free input buffers). If it is determined that there are free VCs, the buffered head flit is then allowed to become the winner flit. If the winner flit of a router during the SA-G action is a head flit, the affected router will then allocate a free VC ID of a downstream router from a table contained in the Free VC module of the affected router. The identity of the allocated VC will also be updated to a table maintained in the VC Map module of the affected router.

Similarly for each router, before a buffered body or tail flit may become a winner flit during the SA-G action, the affected router will check its Credit Counter module to determine if a VC ID that had previously been allocated to a head flit associated with the body or tail flit has any free credits, i.e. whether the associated allocated VC of the downstream router has available flit-slots to receive the body or tail flit. If the router determines from its Credit

Counter module that the allocated VC does have free credits, the buffered body or tail flit may then become a winner flit, else the router will be configured in stop mode.

Regardless whether the winner flit is a head, body or tail type of flit, the identity of the VC allocated to the winner flit of the SA-G action will then be transmitted to the adjacent downstream router together with the winner to inform the adjacent downstream router of the allocation of its VC. This transmission takes place via VC identifier wire 204.

If during the SA-G action it is determined that a router is to perform a bypassing action, a global VC credit will be generated by the affected router during the Switch Traversal (ST) and Link Traversal (LT) actions that take place during cycle-3. If the generated global VC credit utilizes the “credit type” field in its format and when the winning flit is a tail flit, a FreeVCandCredit type of global VC credit will be created and if the winning flit is a head or body flit, a FreeCreditOnly type of global VC credit will be created. Alternatively, the “credit type” field may be omitted from the format of the generated global VC credit.

During cycle-3, the local VC credit received at the upstream router is processed. If the credit type field is utilized for the received local VC credit, the upstream router will check this field to obtain the type of local VC credit received. If the local VC credit received is of the FreeVCandCredit type, the upstream router will obtain the VC ID from the local VC credit and increment a credit count associated with the VC in its Credit Counter module. The upstream router will also add the VC ID to a table maintained in its Free VC module. If the local credit received is of the type FreeCreditOnly, the upstream router will obtain the VC ID from the local VC credit and increment a credit count associated with the VC in its Credit Counter module only.

Alternatively, if the received local VC credit does not utilize the credit type field in its format, the upstream router will obtain the VC ID from the local VC credit and increment a credit count associated with the VC in its Credit Counter module. After the credit count has been incremented, if the total credit count is equal to the maximum number of credits associated with the VC, the upstream router will then release the VC by adding the VC ID to a table maintained in its Free VC module.

During cycle-3, the global VC credit will be generated as described above. It should be noted that the generated global VC credit is stored in the router that generated the global VC credit and is only transmitted to an adjacent upstream router via credit wire 206 during the next cycle-1. The winner flits from the SA-L and SA-G actions then traverse the crossbar switches of each of these routers.

During a subsequent cycle-1, the generated global VC credits will then be transmitted to the respective adjacent upstream routers. The received global VC credit will then be used to update a credit counter at the Credit Counter module of the relevant upstream router. If the credit type field is utilized for the received global VC credit, the upstream router will check this field to obtain the type of global VC credit received. If the global VC credit received is of the FreeVCandCredit type, the upstream router will obtain the VC ID from the global VC credit and increment a credit count associated with the VC in its Credit Counter module. The upstream router will also add the VC ID to a table maintained in its Free VC module. If the global VC credit received is of the type FreeCreditOnly, the upstream router will obtain the VC ID from the global VC credit and increment a credit count associated with the VC in its Credit Counter module only.

Alternatively, if the received global VC credit does not utilize the credit type field in its format, the upstream router will obtain the VC ID from the global VC credit and increment a

credit count associated with the VC in its Credit Counter module. After the credit count has been incremented, if the total credit count is equal to the maximum number of credits associated with the VC, the upstream router will then release the VC by adding the VC ID to a table maintained in its Free VC module.

Figure 3b illustrates another embodiment of the invention whereby the VC credit generation and consumption mechanism of the Port-to-Port VC credit management scheme as described above has been further optimized. In particular, Figure 3b illustrates a plurality of point-to-point interconnects and routers that are similar in configuration to those that have been previously described in relation to Figure 3a. The main difference between the schemes illustrated in Figures 3a and 3b is the addition of SA-G result wire 208 between each adjacent router whereby SA-G result wire 208 is utilized for the transfer of global VC credits from a router to an upstream router. By utilizing two groups of dedicated upstream wires, i.e. credit wire 206 and SA-G result wire 208, this means that the local VC credit and the global VC credit may both be transferred simultaneously during the same cycle without the need to delay the transmission of either VC credit. This additional SA-G result wire optimizes the operation of the previously described embodiment by decreasing the credit latency delays caused by the simultaneous transmission of two types of VC credits during a single cycle

In yet another embodiment of the invention, in order to reduce the total wire cost or the size of the wire required to transfer a global VC credit, the information contained within a global VC credit is reduced from a width size of $\lceil \log_2(\#VNet) + \log_2(\#VC_Per_VNet) + 2 \rceil$, i.e. 5 bits, to just 1 bit. The width size of the global VC credit has previously been described in Table 1. To do so, instead of transmitting a global VC credit that contains all the information set out in Table 1, the optimized global VC credit only transmits the result of the SA-G action. In particular, the optimized global VC credit comprises the following:

Global VC Credit Signal	SA-G Action Result (Bypass or Stop)
Width size (bit)	1

Table 2

The information contained within a global VC credit may be reduced as proposed above because an upstream router need only know whether an adjacent downstream router is bypassing an input flit (i.e. SA-G bypass result), buffering an input flit (i.e. SA-G stop result) or the flit cannot be bypassed because there are no available credits in an allocated VC in a further downstream router (i.e. SA-G stop result). The upstream router does not require information such as the VC ID, credit type or VNET ID because the upstream buffer has already stored in its VC Map module the flit type, the associated virtual network of an adjacent downstream router and the identity of the associated virtual channel of the adjacent downstream router. As such, the global credit transmitted by the downstream router need not repeat all the information already contained in the upstream router's VC Map module.

When an upstream router receives a SA-G "bypass" result, the upstream router will check a register that stores the SSR results to obtain the flit type, the associated VC ID and the associated virtual network identity. Using this information, the upstream router will then increment a credit count associated with the VC in its Credit Counter module accordingly. Conversely, when an upstream router receives a SA-G "stop" result, the upstream router will not increment any credit counts in its Credit Counter module.

In this embodiment of the invention, as a global VC credit only comprises the SA-G action's result, the global VC credit is generated after the SA-G action has taken place. The transmission of the global VC credit then can be subsequently transmitted in the subsequent cycle during the ST or LT action, which is one cycle faster than the previous embodiment of the invention. For completeness, it should be noted that in this embodiment of the invention,

the transmission of the local credit on credit wire 206 remains that same as that used in conventional SMART NOC communication solutions.

Figure 3c illustrates yet another embodiment of the invention whereby a VC-to-VC direct credit wire management scheme is proposed. The VC-to-VC direct credit wire management scheme utilizes a plurality of point-to-point interconnects and routers that are similar in configuration to those that have been previously described in relation to Figure 3a. As illustrated in Figure 3c, dedicated individual credit wires 370 comprise a plurality of individual credit wires that each connects a VC of downstream router 365 with a corresponding buffer in Free VC module 225 and Credit Counter module 226 of the upstream router. These dedicated credit wires 370 are utilized for the transfer of local and global VC credits from a router to an upstream router.

When a local or global VC credit is to be transmitted from the downstream router to the upstream router (i.e. from downstream router 365 to upstream router 360), the transmission of the relevant VC credit may be done using the individual credit wire associated with the VC in the downstream router. For example, as illustrated in Figure 3c, if VC-1 of downstream router 365 is to transmit a local or a global VC credit to upstream router 360, the generated VC credit will be transmitted using the individual credit wire connected to VC-1. Further, upstream router 360 does not require information such as the VC ID, credit type or VNET ID to be transmitted from downstream router 365 because each of credit wires 370 each link individual VCs from downstream router 365 to their associated buffers in Credit Counter module 226 and Free VC module 225. As such, in this example, upstream router 360 will know that the VC credit originated from VC-1.

When upstream router 360 receives a VC credit from downstream router 365, upstream router 360 will increment a credit count associated with the VC in Credit Counter

module 226. After the credit count has been incremented, if the total credit count is equal to the maximum number of credits associated with the VC, upstream router 360 will then release the VC by adding the VC ID to a table maintained in Free VC module 225.

An embodiment of the invention is described using an exemplary implementation as illustrated in Figure 4. In this exemplary implementation of the invention, router 420 is configured to transfer a buffered head flit A1 to router 422 by multiple hops, by bypassing router 421, within three (3) cycles. As the flit to be transferred originated from router 420, router 420 is known as the injector router for the purposes of this example. The timing diagram illustrated in this example only shows the actions that are carried out by the respective modules in relation to the transfer of flit A1 from router 420 to router 422.

During cycle-1, routers 420, 421 and 422 will carry out the BW action to buffer any incoming flits. As there are no incoming flits at this cycle, no BW action is taken. Each of these routers will then perform SA-L to determine which buffered flit becomes a winner flit for each router. We shall assume that VC IDs 420a, 421a and 422a all contain empty input buffers. When router 420 checks a table in Free VC module 410, router 420 will then determine that router 421 has free VC ID 421a. Similarly, when router 421 checks a table in Free VC module 411, router 421 will determine that router 422 has free VC ID 422a.

As router 420 has determined that VC ID 421a is free during the SA-L at router 420, flit A1 will then become the winning flit. As flit A1 is a head flit, router 420 will allocate VC ID 421a from Free VC module 410 for flit A1. A table in VC Map module 400 will also be updated with the allocated VC ID 421a. Simultaneously, VC ID 421a and information about flit A1 will also be transmitted to router 421 to inform router 421 about flit A1 and about the allocation of its VC. This transmission takes place when flit A1 is transmitted and is done via VC identifier wire 204.

At router 420, a local VC credit will also be generated for the VC of flit A1 during the SA-L action, i.e. a local credit for VC ID 420a. As flit A1 is a head flit, the local credit generated will be of the type FreeCreditOnly. However, as this router is the injector router, there is no upstream router for this credit to be transmitted to.

During cycle-2, SSRs are broadcasted from router 420 to routers 421 and 422 using SSR pipelines 302. Each of these routers will then perform SA-G and arbitrate among the SSRs received. Based on the SSRs, it is determined that at router 420, flit A1 will be the winning flit; at router 421, an input flit will be the winning flit; and at router 422, no further action will occur. In other words, router 421 will have a SA-G result of “bypass” while router 422 will have a SA-G result of “stop”.

As router 421 has determined that VC ID 422a has free credit, e.g. buffers C1-C3, during the SA-G at router 421, an input flit at router 421 may become the winning flit. As router 421 has previously been informed that flit A1 is a head flit, router 421 will allocate a free VC, i.e. VC ID 422a from free VC module 411, for the flit at its input, i.e. flit A1. A table in VC Map module 401 will then be updated with the allocated VC ID 422a. Simultaneously, VC ID 422a will also be transmitted to router 422 to inform router 422 about flit A1 and of the allocation of its VC. This transmission takes place when flit A1 is transmitted and is done via VC identifier wire 204.

At router 420, as the SA-G action has determined that buffered flit A1 will gain access to the crossbar switch of router 420, a Credit Counter module in router 420 will then be decreased accordingly to show that a buffer in allocated VC ID 421a will be occupied by flit A1 at the next cycle. Also, as a flit at the input of router 421 has gained access to the crossbar switch of the router, i.e. flit A1; a Credit Counter module in router 421 will then be

decreased accordingly to show that a buffer at the pre-allocated VC ID 422a will be occupied by flit A1 at the next cycle.

During cycle-3, as router 421 is carrying out the bypassing action, router 421 will generate a global VC credit. As flit A1 is a head flit, the global VC credit generated will be of the type FreeCreditOnly. It should be noted that this generated global credit remains with router 421, and the transmission of the global credit to router 420 only takes place in a subsequent cycle-1.

During cycle-3, flit A1 will traverse the crossbar switch of router 420, traverse through data wire 202 to the input of router 421, traverse the crossbar switch of router 421, traverse through data wire 202 to the input of router 422 and latching onto the input of router 422.

During a subsequent cycle-1, the global VC credit generated by router 421 will be transmitted to router 420 and is then used to update the Credit Counter module of router 420. As the global credit received by router 420 is of the type FreeCreditOnly, router 420 will only increment the credit count of corresponding VC ID 421a in its Credit Counter module. At this cycle, flit A1 will then be written into the input buffer of router 422 during the BW action at router 422.

In accordance with an embodiment of the invention, a method for managing the allocation of VCs in adjacent downstream routers and for generating local/global VC credits as required is provided, whereby the method comprises the following four steps:

Step 1, determining and allocating, during a first cycle, using a first router, a free virtual channel of a second router, and updating a VCMap table of the first router with an identity of the allocated virtual channel of the second router, wherein the second router is downstream of the first router;

Step 2, determining and allocating, during a second cycle, using the second router, a free virtual channel of a third router, and updating a VCMAP table of the second router with an identity of the allocated virtual channel of the third router, wherein the third router is downstream of the second router;

Step 3, in response to allocating the free virtual channel at the second router, during a third cycle, delivering a first flit from the first router to the second router and informing the second router of the identity of the allocated virtual channel at the second router using a dedicated wire connecting the first and second routers

Step 4, in response to allocating the free virtual channel at the third router, during the third cycle, delivering the first flit from the second router to the third router and informing the third router of the identity of the allocated virtual channel at the third router using a dedicated wire connecting the second and third routers.

In order to provide such a system or method, a process is needed for managing the allocation of VCs in adjacent downstream routers and for generating local/global VC credits as required. The following description and Figures 5-7 describe embodiments of processes in accordance with this invention.

Figure 5 illustrates process 500 that is performed by an injector router or upstream router of a processing core to arbitrate and allocate a VC in a downstream router in accordance with embodiments of this invention. Process 500 begins in step 505 by first selecting a head flit of a buffered packet that is to be transmitted from the injector router to a downstream router. This head flit would be stored in an input buffer in the injector router. At step 515, process 500 then determines whether a free VC is available for the associated virtual network. If process 500 determines that the selected virtual network does not have a free VC, process 500 proceeds to step 545 whereby process 500 determines whether Free

VC module contains another virtual network to be selected. If Free VC module does not contain a virtual network with a free VC, process 500 proceeds to step 550 whereby process 500 determines that the flit may not be transmitted. Process 500 then ends. Returning to step 545, if there exists another virtual network in the Free VC module, process 500 selects this other virtual network at step 540 and then proceeds back to the determination step at 515. Process 500 repeats steps 515-540 until a virtual network with a free VC is selected. Alternatively, if process 500 determines at step 515-545 that all virtual networks do not have free a VC, process 500 then ends.

If process 500 determines at step 515 that a selected virtual network has a free VC, process 500 then proceeds to step 520, to allocate the free virtual channel to the head flit that is to be transmitted to a router downstream. Process 500 then updates a table in its VC Map module to associate the selected virtual channel with the identity of the injector router so that subsequent body flits belonging to this packet may be transferred to the same virtual channel in the downstream router. At the next step, which is step 530, process 500 then informs the downstream router of the identity of its virtual channel which has been allocated to receive the head flit and subsequent flits belonging to the same packet. The head flit is also simultaneously transmitted at this step. Process 500 then ends.

Figure 6 illustrates process 600 that is performed to transfer a head flit from the first router to a third router by causing the flit to bypass the second router in accordance with embodiments of the invention. Process 600 begins at step 605 by first selecting a buffered head flit at the first router. Process 600 then performs the necessary checks as previously described in step 510-530 in process 500 to select a VC of the second router. In process 600, this takes place at step 610. It should be noted that step 605 and 610 of process 600 would take place during a cycle-1.

Process 600 then proceeds to set the second router to bypass mode at step 615 during the SA-G action. Process 600 then performs the necessary checks at the second router as previously described in step 510-530 in process 500 to select a VC of the third router. This step takes place during a cycle-2.

Process 600 then causes the head flit to be transferred from the first router to the second router at step 620 and since the router at the second router has been set to bypass mode, process 600 will cause the flit to bypass the second router at step 625. During the transmission of the head flit from the first router, the second router will be informed about its VC that had been allocated by the first router. Simultaneously, at step 640, process 600 will proceed to generate a global VC credit in the second router. The bypassed flit is then transferred to a third router by process 600 at step 630. During the transmission of the head flit from the second router, the third router will be informed about its VC that had been allocated by the second router. These steps all take place during cycle-3.

Process 600 then causes the flit received at the third router to be buffered at its pre-allocated virtual channel during a BW action at step 635. Simultaneously, process 600 will transfer the generated global VC credit from the second router to the first router at step 645. These steps all take place at a new cycle-1. Process 600 then ends.

Figure 7 illustrates process 700 that is performed by a first, a second and a third router to transfer a 1st flit from the first router to the second router, and a 2nd flit from the second router to the third router. The 1st flit buffered at the second Router is then transferred to a third Router at the subsequent cycles. Process 700 begins at step 705 by first selecting a buffered head flit at the first router. Process 700 then performs the necessary checks as previously described in step 510-530 in process 500 to select a VC of the second router. Simultaneously at step 704, process 700 selects a flit buffered at the second router and

performs the necessary checks as previously described in step 510-530 in process 500 to select a VC of the third router. After this is done, process 700 proceeds to generate a local VC credit at the second router at step 706. These steps all take place during cycle-1.

Process 700 then proceeds to set the SA-G of the second router to stop mode at step 708. The SA-G of the third router is also set to stop mode at step 710 by process 700. Simultaneously, process 700 causes the earlier generated local VC credit to be transmitted from the second router to the first router at step 712. These steps all take place during cycle-2.

Process 700 then proceeds to transfer the head flit from the first router to the second router and the flit buffered at the second router to the third router. This takes place at steps 714 and 716 respectively. These steps all take place during cycle-3.

Process 700 then causes the head flit to be buffered into the allocated virtual channel at the second router at step 718. The flit received by the third router is buffered into the allocated virtual channel at the third router at step 720. Process 700 then proceeds to select the buffered head flit in the second router at step 722. The necessary checks as previously described in step 510-530 in process 500 to select a free VC of the third router are also carried out at step 722. Simultaneously, a local VC credit will be generated at the second router by process 700 at step 724. These steps all take place at a subsequent cycle-1.

Process 700 then proceeds to set the SA-G of the second router to stop mode at step 726. Simultaneously, process 700 causes the earlier generated local VC credit to be transmitted from the second router to the first router at step 730. These steps all take place during a subsequent cycle-2.

Process 700 then proceeds to transfer the buffered head flit from the second router to the third router at step 728. This step takes place during a subsequent cycle-3.

Subsequently during yet another new cycle-1, process 700 will cause the head flit to be buffered at the allocated virtual channel at the third router at step 732. Process 700 then ends.

The processes mentioned above may be provided as instructions stored in a non-transitory computer-readable media and may be executed by a processing unit in a computer system. For the avoidance of doubt, non-transitory computer-readable media shall be taken to comprise all computer-readable media except for a transitory, propagating signal. A processing unit may be provided in one or more computer systems to provide this invention. The instructions may be stored as firmware, hardware, or software.

The above is a description of embodiments of a system and process in accordance with the present invention as set forth in the following claims. It is envisioned that others may and will design alternatives that fall within the scope of the following claims.

CLAIMS:

1. A method for managing an express traversal of flits in a network on chip, the method comprising:

determining and allocating, during a first cycle, using a first router, a free virtual channel of a second router, and updating a VCMMap table of the first router with an identity of the allocated virtual channel of the second router, wherein the second router is downstream of the first router;

determining and allocating, during a second cycle, using the second router, a free virtual channel of a third router, and updating a VCMMap table of the second router with an identity of the allocated virtual channel of the third router, wherein the third router is downstream of the second router;

in response to allocating the free virtual channel of the second router, during a third cycle, delivering a first flit from the first router to the second router and informing the second router of the identity of the allocated virtual channel of the second router using a dedicated wire connecting the first and second routers, and

in response to allocating the free virtual channel of the third router, during the third cycle, delivering the first flit from the second router to the third router by bypassing the allocated virtual channel of the second router, and informing the third router of the identity of the allocated virtual channel of the third router using a dedicated wire connecting the second and third routers.

2. The method according to claim 1 wherein the determining and the allocating the free virtual channel of the second router comprises:

selecting, using the first router, a virtual channel of the second router from a FreeVC table provided at the first router;

determining if the selected virtual channel has credit; and

in response to determining that the selected virtual channel has credit, allocating the selected virtual channel as the free virtual channel of the second router for receiving a flit from the first router.

3. The method according to any one of claims 1 or 2 wherein the determining and the allocating the free virtual channel of the third router comprises:

selecting, using the second router, a virtual channel of the third router from a FreeVC table provided at the second router;

determining if the selected virtual channel has credit; and

in response to determining that the selected virtual channel has credit, allocating the selected virtual channel as the free virtual channel of the third router for receiving a flit from the second router.

4. The method according to any one of claims 1 to 3 wherein the updating of the VCMap table of the first router comprises:

adding the identity of the allocated virtual channel of the second router as an entry to the VCMap table; and

associating the entry with an identity of the first router and an identity of a virtual network of the second router, wherein the allocated virtual channel is a part of the virtual network.

5. The method according to any one of claims 1 to 4 wherein the updating of the VCMap table of the second router comprises:

adding the identity of the allocated virtual channel of the third router as an entry to the VCMap table; and

associating the entry with an identity of the first router and an identity of a virtual network of the third router, wherein the allocated virtual channel is a part of the virtual network.

6. The method according to claim 1 wherein the bypassing the allocated virtual channel of the second router further comprises:
 - generating a credit associated with the virtual channel of the second router;
 - and
 - providing the generated credit to the first router.
7. The method according to claim 6 wherein the generated credit is provided to the first router using a dedicated result wire provided between the first router and the second router.
8. The method according to claim 7 wherein the generated credit comprises a Switch Allocation Global (SA-G) action result.
9. The method according to any one of claims 1 to 6 wherein a dedicated result wire is provided between the first router and the second router, and between the second router and the third router.
10. A system for managing an express traversal of flits in a network on chip, the system comprising:
 - a first router configured to, during a first cycle, determine and allocate a free virtual channel of a second router, and update a VCMaP table of the first router with an identity of the allocated virtual channel of the second router, wherein the second router is downstream of the first router;
 - a second router configured to, during a second cycle, determine and allocate a free virtual channel of a third router, and update a VCMaP table of the second

router with an identity of the allocated virtual channel of the third router, wherein the third router is downstream of the second router;

in response to allocating the free virtual channel of the second router, the first router is configured to, during a third cycle, deliver a first flit from the first router to the second router and to inform the second router of the identity of the allocated virtual channel of the second router using a dedicated wire connecting the first and second routers, and

in response to allocating the free virtual channel of the third router, the second router is configured to, during the third cycle, deliver the first flit from the second router to the third router by bypassing the allocated virtual channel of the second router and to inform the third router of the identity of the allocated virtual channel of the third router using a dedicated wire connecting the second and third routers.

11. The system according to claim 10 wherein when determining and allocating the free virtual channel of the second router, the first router is further configured to:

select a virtual channel of the second router from a FreeVC table provided at the first router;

determine if the selected virtual channel has credit; and

in response to determining that the selected virtual channel has credit, to allocate the selected virtual channel as the free virtual channel of the second router for receiving a flit from the first router.

12. The system according to any one of claims 10 or 11 wherein when determining and allocating the free virtual channel of the third router, the second router is further configured to:

select a virtual channel of the third router from a FreeVC table provided at the second router;

determine if the selected virtual channel has credit; and

in response to determining that the selected virtual channel has credit, to allocate the selected virtual channel as the free virtual channel of the third router for receiving a flit from the second router.

13. The system according to any one of claims 10 to 12 wherein when updating the VCMMap table of the first router, the first router is further configured to:

add the identity of the allocated virtual channel of the second router as an entry to the VCMMap table; and

associate the entry with an identity of the first router and an identity of a virtual network of the second router, wherein the allocated virtual channel is a part of the virtual network.

14. The system according to any one of claims 10 to 13 wherein when updating the VCMMap table of the second router, the second router is further configured to:

add the identity of the allocated virtual channel of the third router as an entry to the VCMMap table; and

associate the entry with an identity of the first router and an identity of a virtual network of the third router, wherein the allocated virtual channel is a part of the virtual network.

15. The system according to claim 10 wherein when the allocated virtual channel of the second router is bypassed, the second router is further configured to:

generate a credit associated with the virtual channel of the second router; and
provide the generated credit to the first router.

16. The system according to claim 15 wherein the generated credit is provided to the first router using a dedicated result wire provided between the first router and the second router.
17. The system according to claim 16 wherein the generated credit comprises a Switch Allocation Global (SA-G) action result.
18. The system according to any one of claims 10 to 15 wherein a dedicated result wire is provided between the first router and the second router, and between the second router and the third router.