

ABSTRACT

A vertical memory device includes a channel extending in a vertical direction on a substrate, a charge storage structure on an outer sidewall of the channel and including a tunnel insulation pattern, a charge trapping pattern, and a first blocking pattern sequentially stacked in a horizontal direction, and gate electrodes spaced apart from each other in the vertical direction, each of which surrounds the charge storage structure. The charge storage structure includes charge trapping patterns, each of which faces one of the gate electrodes in the horizontal direction. A length in the vertical direction of an inner sidewall of each of the charge trapping patterns facing the tunnel insulation pattern is less than a length in the vertical direction of an outer sidewall thereof facing the first blocking pattern.

FIG. 2