## Claims

1. A method, comprising:

providing a monocrystalline silicon wafer having a principal surface which supports a masking layer having windows which expose corresponding regions of the silicon wafer;

forming silicon carbide seed regions on the exposed regions of the wafer; and

growing monocrystalline silicon carbide on the silicon carbide seed regions.

2. A method according to claim 1, wherein providing the silicon wafer having a principal surface which supports a masking layer comprises:

providing an monocrystalline silicon wafer;

forming a masking layer on the silicon wafer, the masking layer directly overlying the principal layer;

providing an etch mask having windows on the masking layer; and

etching the masking layer through the windows in the etch mask to reach the principal surface of the wafer.

3. A method according to claim 1 or 2, wherein the masking layer is a layer of dielectric material.

4. A method according to claim 3, wherein the masking layer is a silicon dioxide layer.

5. A method according to claim 4, wherein forming the silicon dioxide layer is a thermal oxide layer.

6. A method according to claim 1 or 2, wherein the masking layer is a layer of semiconductor or conductive material.

7. A method according to claim 1 or 2, wherein the masking layer is a layer of polycrystalline silicon.

8. A method according to any preceding claim, wherein the masking layer comprises a bilayer comprising first and second bilayer layers.

9. A layer according to any preceding claim, wherein the masking layer has a thickness in a range between 2,000 and 10,000 Å.

10. A layer according to any preceding claim, wherein the masking layer has a thickness in a range between 4,000 and 6,000 Å.

11. A method according to any preceding claim, wherein the principal surface is a first principle surface and the masking layer is a first masking layer and the silicon wafer has a second, opposite principal surface which supports a second masking layer.

12. A method according to claim 11, wherein the first masking layer and the second masking layer comprise the same material.

13. A method according to any preceding claim, wherein forming the silicon carbide seed regions comprises:

depositing carbon on the exposed regions of the wafer; and

converting the carbon into silicon carbide.

14. A method according to any preceding claim, wherein growing the silicon carbide comprises growing silicon carbide having a thickness of at least 0.5 μm, optionally at least 1 μm, optionally at least 2 μm and/or optionally at least 5 μm.

15. A method according to any preceding claim, wherein growing the silicon carbide layers comprises growing silicon carbide having a thickness of no more than 5 μm or no more than 10 μm.

16. A method according to any preceding claim, wherein growing the silicon carbide layers comprises growing 3-step cubic silicon carbide.

17. A method according any preceding claim, wherein the wafer has a diameter of at least 4 inches (101.6 mm) or 100 mm.

18. A method according to any preceding claim, wherein the wafer has a thickness of at least 500 μm.

19. A method according to any preceding claim, further comprising:
processing the silicon carbide to form semiconductor devices.

20. A method according to any preceding claim, further comprising:
cutting the masking layer and the silicon wafer between the windows to form dies.

21. A method according to any preceding claim, wherein the windows have a first width which is substantially larger than a second width between the windows.

22. A method according to any preceding claim, wherein the windows have a width and/or length in a range between 5 mm and 20 mm.

23. A method according to any preceding claim, wherein the windows are separated by a width of less than 1 mm, less than 500 μm or less than 200 μm.

24. A method according to any preceding claim, wherein the windows are separated by a width of about 100 μm.

25. A method of forming a semiconductor die including a method according to any preceding claim.

26. A method comprising:
forming a semiconductor die according to claim 25; and
packaging the semiconductor die.

27. A silicon semiconductor structure comprising:

a monocrystalline silicon wafer having a principal surface; and

spaced apart monocrystalline silicon carbide layers disposed directly on the principal surface of the wafer.

28. A semiconductor structure according to claim 27, wherein each silicon carbide layer comprises:

a silicon carbide seed region formed directly on the principal surface of the silicon wafer; and

a monocrystalline silicon carbide layer disposed directly on the silicon carbide seed region.

29. A semiconductor structure according to claim 27 or 28, wherein the silicon carbide layers comprise 3-step cubic silicon carbide.

30. A semiconductor structure according to any one of claims 27 to 29, further comprising:

a masking layer supported on the principal surface of the silicon wafer having windows which cause the monocrystalline silicon carbide layers to be spaced apart.

31. A semiconductor structure according to any one of claims 27 to 30, further comprising:

polycrystalline silicon carbide layer(s) disposed between the silicon carbide layers.

32. A semiconductor structure according to claim 31, wherein polycrystalline and monocrystalline silicon carbide layers are formed in different regions of a single silicon carbide layer.

33. A semiconductor device comprising:

a monocrystalline silicon substrate having a principal surface and a perimeter, the silicon substrate comprising an outer, annular region running

adjacent to the perimeter of the substrate and an inner region disposed inside the outer region; and

a monocrystalline silicon carbide layer disposed directly on the principal surface of the substrate on the inner region but not on or over the outer region of the substrate.

34. A semiconductor device according to claim 33, wherein the silicon carbide layer comprises:

a monocrystalline silicon carbide seed region formed directly on the principal surface of the silicon substrate; and

a monocrystalline silicon carbide layer disposed directly on the silicon carbide seed region.

35. A semiconductor device according to claim 33 or 34, wherein the silicon carbide layer comprises 3-step cubic silicon carbide.

36. A semiconductor device according to any one of claims 33 to 35, further comprising:

a masking layer supported on the principal surface of the silicon substrate on the outer region but not on the inner region .

37. A semiconductor device according to any one of claims 33 to 36, further comprising:

polycrystalline silicon carbide layer disposed on the outer region but not on the inner region.

38. A semiconductor device according to claim 37, wherein polycrystalline monocrystalline silicon carbide layers are formed in different regions of a single silicon carbide layer.

39. A semiconductor device according to any one of claims 33 to 38, wherein the inner region has a width and/or length in a range between 5 mm and 20 mm.

Claims

1. A method, comprising:

providing a monocrystalline silicon wafer having a principal surface which supports a masking layer having windows which expose corresponding regions of the silicon wafer;

forming silicon carbide seed regions on the exposed regions of the wafer;

growing monocrystalline silicon carbide layers on the silicon carbide seed regions; and

forming regions of polycrystalline and/or amorphous silicon carbide between the monocrystalline silicon carbide layers.

2. A method according to claim 1, wherein providing the silicon wafer having a principal surface which supports a masking layer comprises:

providing an monocrystalline silicon wafer;

forming a masking layer on the silicon wafer, the masking layer directly overlying the principal layer;

providing an etch mask having windows on the masking layer; and

etching the masking layer through the windows in the etch mask to reach the principal surface of the wafer.

3. A method according to claim 1 or 2, wherein the masking layer is a layer of dielectric material.

4. A method according to claim 3, wherein the masking layer is a silicon dioxide layer.

5. A method according to claim 4, wherein forming the silicon dioxide layer is a thermal oxide layer.

6. A method according to claim 1 or 2, wherein the masking layer is a layer of semiconductor or conductive material.

7. A method according to claim 1 or 2, wherein the masking layer is a layer of polycrystalline silicon.

8. A method according to any preceding claim, wherein the masking layer comprises a bilayer comprising first and second bilayer layers.

9. A layer according to any preceding claim, wherein the masking layer has a thickness in a range between 2,000 and 10,000 Å.

10. A layer according to any preceding claim, wherein the masking layer has a thickness in a range between 4,000 and 6,000 Å.

11. A method according to any preceding claim, wherein the principal surface is a first principle surface and the masking layer is a first masking layer and the silicon wafer has a second, opposite principal surface which supports a second masking layer.

12. A method according to claim 11, wherein the first masking layer and the second masking layer comprise the same material.

13. A method according to any preceding claim, wherein forming the silicon carbide seed regions comprises:

depositing carbon on the exposed regions of the wafer; and

converting the carbon into silicon carbide.

14. A method according to any preceding claim, wherein growing the silicon carbide layers comprises growing silicon carbide having a thickness of at least 0.5 μm, optionally at least 1 μm, optionally at least 2 μm and/or optionally at least 5 μm.

15. A method according to any preceding claim, wherein growing the silicon carbide layers comprises growing silicon carbide having a thickness of no more than 5 μm or no more than 10 μm.

16. A method according to any preceding claim, wherein growing the silicon carbide layers comprises growing 3-step cubic silicon carbide.

17. A method according any preceding claim, wherein the wafer has a diameter of at least 4 inches (101.6 mm) or 100 mm.

18. A method according to any preceding claim, wherein the wafer has a thickness of at least 500 μm.

19. A method according to any preceding claim, further comprising:

processing the silicon carbide to form semiconductor devices.

20. A silicon semiconductor structure comprising:

a monocrystalline silicon wafer having a principal surface;

monocrystalline silicon carbide layers disposed directly on the principal surface of the wafer, wherein each monocrystalline silicon carbide layer is spaced apart from one another on the principal surface of the wafer; and

polycrystalline and/or amorphous silicon carbide layer(s) disposed between the silicon carbide layers.

21. A semiconductor structure according to claim 20, wherein each silicon carbide layer comprises:

a silicon carbide seed region formed directly on the principal surface of the silicon wafer; and

a monocrystalline silicon carbide layer disposed directly on the silicon carbide seed region.

22. A semiconductor structure according to claim 20 or 21, wherein the silicon carbide layers comprises 3-step cubic silicon carbide.

23. A semiconductor structure according to any one of claims 20 to 22, further comprising:

a masking layer supported on the principal surface of the silicon wafer having windows which cause the monocrystalline silicon carbide layers to be spaced apart.

24. A semiconductor structure according to any one of claims 20 to 23, wherein polycrystalline and monocrystalline silicon carbide layers are formed in different regions of a single silicon carbide layer.