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METHOD OF FABRICATION A POLYSILICON CAPACITOR UTILIZING FET AND BIPOLAR BASE POLYSILICON LAYERS

Abstract

A method of forming a poly-poly capacitor, a MOS transistor, and a bipolar transistor simultaneously on a substrate (10) comprising the steps of depositing and patterning a first layer of polysilicon on the substrate (10) to form a first plate electrode (26) of said capacitor and on a electrode of the MOS transistor, and depositing and patterning a second layer of polysilicon on the substrate (10) to form a second plate electrode (42) of said capacitor and an electrode of the bipolar transistor.

Fig 1D

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