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COPPER INTERCONNECT WITH TOP BARRIER LAYER

BACKGROUND OF THE INVENTION

(1) FIELD OF THE INVENTION

The invention relates to the general field of integrated circuits, more particularly to the design and use of copper interconnections therein.

(2) DESCRIPTION OF THE PRIOR ART

As wire widths in integrated circuits continue to shrink, the electrical conductivity of the wiring material itself becomes increasingly more important. Thus, in this regard, aluminum, which has been the material of choice since the integrated circuit art began, is becoming less attractive than other better conductors such as copper, gold, and silver. These materials, in addition to their superior electrical conductivity, are also more resistant than aluminum to electromigration, a quality that grows in importance as wire widths decrease.

The metals in question have not been widely used for wiring as yet because they also suffer from a number of disadvantages, including formation of undesirable intermetallic alloys and/or recombination centers in other parts of the integrated circuit and they often have high diffusion rates. Copper has the additional disadvantage of being readily oxidized at relatively low temperatures. Nevertheless, copper is seen as an attractive replacement for aluminum because of its low cost and ease of processing so that the prior and current art has tended to concentrate on finding ways to overcome these limitations.

A particular problem related to copper's high susceptibility to oxidation is that conventional photoresist processing cannot be used when the copper is to be patterned into various wire shapes because the photoresist needs to be removed at the end of the process by heating it in a highly oxidizing environment, such as an oxygen plasma, thereby converting it to an easily removed ash.

Several solutions to the above problems associated with copper processing have been proposed in the prior art. Hoshino (U.S.P. 4,910,169 Mar 1990) teaches the use of low temperature deposition techniques, such as RF sputtering, for coating copper layers with materials such as silicon oxide, silicon nitride, and phosphosilicate glass. It should be noted that the materials

mentioned were for the purpose of forming inter-metal dielectric layers rather than for use as barrier layers, implying that they were relatively thick.

Li et al. (U.S.P. 5,447,599 Sep 1995) use TiN(O) as a barrier layer material for copper. The copper is initially coated with a layer of titanium and a copper-titanium alloy is formed by heating at 3-400 °C. Unreacted titanium is then removed and the alloy is transformed to TiN(O) by means of a rapid thermal anneal in ammonia and oxygen.

Nakasaki (U.S.P. 5,084,412 Jan 1992) underlays the copper layer with a metallic nitride and then heats the combination in nitrogen to bring about grain boundary diffusion of the nitrogen into the copper. This results in a material having relatively low electrical resistivity together with good resistance to electromigration.

Tokunaga et al. (U.S.P. 4,931,410 Jun 1990) use photoresist for shaping their copper but first protect it with an anti-oxidizing layer. Etching is then performed in two steps ---- first the anti-oxidizing layer is etched in conventional fashion, including photoresist removal, following which said anti-oxidizing layer is used as the mask for the etching of the copper.

Filipiak et al. (U.S.P. 5,447,887 Sep 1995) use an intermediate layer of copper silicide to improve the adhesion between a copper layer and a silicon nitride layer.

It should be noted that none of the above-cited examples of the prior art is based on a damascene process nor do they incorporate more than a single barrier layer in their structures or processes. The term 'damascene' is derived from a form of inlaid metal jewelery first seen in the city of Damascus. In the context of integrated circuits it implies a patterned layer imbedded on and in another layer such that the top surfaces of the two layers are coplanar.

SUMMARY OF THE INVENTION

It has been an object of the present invention to provide a copper connector in an integrated circuit.

A further object of the present invention has been to provide means for preventing the outdiffusion of copper from said connector into adjoining layers.

Yet another object of the present invention has been to

provide a method for manufacturing said copper connector that does not expose the copper to the possibility of being oxidized during processing.

A still further object of the present invention has been to provide a method for manufacturing said copper connector without having a layer of photoresist in contact with the copper at any time.

These objects have been achieved by providing a damascene copper connector whose upper surface is coplanar with the upper surface of the insulating layer in which it is embedded. Out-diffusion of copper from the connector is prevented by two barrier layers. One is located at the interface between the connector and the insulating layer while the second barrier is an insulating layer which covers the upper surface of the connector. The damascene process involves filling a trench in the surface of the insulator with copper and then removing the excess by chem.-mech. polishing. Since photoresist is never in direct contact with the copper the problem of copper oxidation during resist ashing has been effectively eliminated.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows the starting point of a process for the manufacture of the present invention.

FIG. 2 shows an intermediate step in said manufacturing process.

FIG. 3 shows a preferred embodiment of the present invention obtained at the completion of said manufacturing process.

FIG. 4 shows additional details related to the application of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A more detailed description of the structure that comprises the present invention will be given below. First, however, it is important to describe the basic nature of said structure as well as the motives behind its development. As already noted, copper is easily oxidized at relatively low temperatures and copper is known to diffuse rapidly through certain dielectric materials, such as silicon oxide, that are widely used in the integrated

circuit art. Also as noted, said oxidation problem of copper makes it impossible to use conventional ashing techniques for the removal of used photoresist in the presence of copper.

To overcome the photoresist removal problem, the present invention uses a damascene technique for forming the copper interconnection pattern, thereby eliminating the need for ashing photoresist in the presence of copper. To overcome said diffusion problem, the present invention provides for a second barrier layer in addition to the barrier layer already known to the prior art. Because the damascene process was used to shape the copper, said second barrier layer lies on a planar surface, making it more effective (for a given thickness) than is the case in a conventional structure of the prior art.

Referring now to FIG. 1, the process for manufacturing the present invention begins with the provision of silicon substrate 20. It is assumed that substrate 20 has already been subjected to a variety of processes associated with the formation of integrated circuits but this is not shown in the figure. Insulating layer 21, consisting of silicon oxide, polyimide, or any similar low dielectric constant material, is then deposited to a thickness between about 0.5 and 2 microns onto substrate 20 by chemical vapor deposition (CVD), physical vapor deposition (PVD) or spin coating. Layer 21 is then patterned and etched to

form trench 22 in its upper surface. Our preferred method for forming the trench has been dry plasma etching but any similar method, such as wet etching, may be used. Typically, the depth of the trench has been between about 4,000 and 12,000 Angstroms, leaving a separation distance between the bottom of the trench and the bottom surface of layer 21 of between about 4,000 and 8,000 Angstroms.

Referring now to FIG. 2, barrier layer 31, comprising titanium nitride, tungsten nitride, titanium tungstide, or tantalum nitride, is now deposited over layer 21, including all walls of trench 22, to a thickness between about 200 and 2,000 Angstroms. This is followed by the deposition of copper layer 30 to a depth sufficient to ensure that all parts of trench 22 are filled with copper as well as those parts of barrier layer 31 that lie outside trench 22. Our preferred method for depositing copper has been CVD, but any similar method such as PVD or electroplating could have been used. An optional copper reflow step may be added following copper deposition.

Referring now to FIG. 3, excess copper, above the level of the top of the trench, is now removed together with those parts of barrier layer 31 that lie outside the trench. This results in the formation of damascene connector 51, as shown. Our preferred method for removing the copper has been chemical-mechanical

polishing but any equivalent method such as blanket etch-back in a chlorine plasma at high temperature could have been used. Second barrier layer 60, comprising an insulating material such as aluminum oxide, tantalum oxide, or silicon nitride is now deposited over layer 21, as well as the exposed surface of demascene connector 51, to a thickness between about 200 and 2,000 Angstroms by CVD or PVD. This is followed by the deposition of insulating layer 41, comprising silicon oxide, polyimide, or similar low dielectric constant material to a thickness between about 0.5 and 2 microns.

FIG. 3 illustrates a preferred embodiment of the structural aspects of the present invention. As can be seen, it comprises damascene copper connector 51 that serves as a wiring connector, being located at the interface betweeen two insulating layers 21 and 41. Outdiffusion of copper from connector 51 into either of layers 21 or 41 is prevented by the presence of the two barrier layers 31 and 60. The former is conventional and well known whereas the latter is believed to be novel.

In practice, connector 51 will need to be accessed through via holes passing through layers 41 and 60. This is illustrated in FIG. 4 where via 23 is seen to have been etched through layers 41 and 60 down to the top surface of copper damascene connector 51. Our preferred method for etching such via holes has been

plasma dry etching but any similar method such as wet chemical etching may be used. An adjoining damascene connector 61 is shown in FIG. 4 to illustrate that second barrier layer 60 serves to protect both it and connector 51. This also means that layer 60 must comprise an insulating material to avoid the formation of short circuits between the different connectors that it protects.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. An electrical connector in an integrated circuit comprising:

a silicon substrate;

a first insulating layer, having upper and lower surfaces, on said substrate;

a copper connector, having upper and lower surfaces, in said first insulating layer such that the upper surface of said copper connector is at the level of the upper surface of said first insulating layer and the lower surface of said copper connector is a distance above the lower surface of said first insulating layer;

an interface between said copper connector and said first insulating layer;

a first barrier layer at said interface;

a second, insulating, barrier layer on the upper surface of said copper connector and the upper surface of said first insulating layer; and

a second insulating layer on said second barrier layer.

2. The connector described in claim 1 wherein said second barrier layer comprises material taken from the group consisting of aluminum oxide, tantalum oxide, and silicon nitride.

3. The connector described in claim 1 wherein the thickness of said second barrier layer is between about 200 and 2,000 Angstroms.

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4. The connector described in claim 1 further comprising a via hole through said second insulating layer and said second barrier layer down to the level of said upper surface of said connector.

5. The connector described in claim 1 wherein the distance between the lower surfaces of said copper connector and said first insulating layer is between about 4,000 and 8,000 Angstroms.

6. A method for manufacturing a copper connector in an integrated circuit comprising:

(a) providing a silicon substrate;

(b) depositing a first insulating layer on said silicon substrate;

(c) patterning and then etching said first insulating layer to form a trench therein;

(d) depositing a first barrier layer on said first insulating layer and on all walls of said trench;

(e) depositing a copper layer on said first barrier layer so as to more than fill said trench;

(f) removing said copper layer and said first barrier layer down to the level of said first insulating layer, thereby forming a damascene connector having an upper surface;

(g) depositing a second barrier layer on said first insulating layer and said upper surface of said damascene

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connector;

(h) depositing a second insulating layer on said second barrier layer; and

(i) patterning and then etching said second insulating layer to form a via passing through said second insulating layer and said second barrier layer to said upper surface of the damascene connector.

7. The method of claim 6 wherein said first insulating layer comprises silicon oxide or polyimide.

8. The method of claim 6 wherein said first insulating layer is deposited to a thickness between about 0.5 and 2 microns.

9. The method of claim 6 wherein the depth of said trench is between about 4,000 and 12,000 Angstroms.

10. The method of claim 6 wherein said first barrier layer comprises material taken from the group consisting of titanium nitride, tungsten nitride, titanium tungstide, and tantalum nitride.

11. The method of claim 6 wherein said first barrier layer is deposited to a thickness between about 200 and 2,000 Angstroms.

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12. The method of claim 6 wherein said copper layer is deposited by chemical vapor deposition or physical vapor deposition or electroplating.

13. The method of claim 6 wherein said copper layer is removed by chemical-mechanical polishing or blanket etch-back.

14. The method of claim 6 wherein said trench is etched by plasma dry etching .

15. The method of claim 6 wherein said via is etched by plasma dry etching.

16. The method of claim 6 wherein said second insulating layer comprises silicon oxide or polyimide.

17. The method of claim 6 wherein said second insulating layer is deposited to a thickness between about 0.5 and 2 microns.

18. The method of claim 6 wherein step (g) further comprises depositing the second barrier layer by chemical vapor deposition or physical vapor deposition.

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