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(54) METHOD AND CIRCUIT FOR DRIVING AN ELECTROCHROMIC DISPLAY CELL

(71) We, TIMEX CORPORATION, a Corporation organized under the Laws of the State of Delaware, United States of America, of Waterbury, Connecticut 06720, United States of America, do hereby declare the invention, for which we pray that a Patent may be granted to us, and the method by which it is to be performed, to be more particularly described in and by the following statement:—

The invention relates to a circuit for driving an electrochromic display cell, and to a method of updating the information displayed by such a cell. Such electrochromic display cells can be utilized to display figures, letters, symbols and the like in timepieces, calculators, meters or the like.

In recent years a great deal of interest has been shown in the provision of electrochromic displays having, for example, a digital or analog readout such as in copending commonly assigned U.S. Patent No. 3,908,355 issued 30th September 1975 in the name of Leo Wiesner. Such cells generally comprise a plurality of segments making up indicating indicia, such as alpha-numeric characters.

Typically, the driving circuit for or method of changing the information being displayed consisted of the two visually distinct operations of consecutively and separately writing and erasing selected segments to effect the change, such as in U.S. Patent No.'s 3,807,832 and 3,839,857.

Thus from the prior art, it is known to separately write selected segments by applying a voltage V_1 of one polarity (usually negative) with respect to a counter electrode for a period to completely write the selected segments and then, consecutively, to erase a segment by separately applying a voltage V_2 of opposite polarity with respect to the same counter electrode for a period to completely erase the selected segments. It is also known to write and erase only those segments requiring change, when changing or updating the character to be displayed, and to utilize the inherent memory of the display by not switching those segments required to remain in their respective "on" or "off" states.

The consecutive operation of updating the prior art displays by completing first the writing process, then the erasing process, or vice versa, results in ambiguities during the transition.

Simultaneous writing and erasing of the respective segments to be written and erased required two voltages V_1 and V_2, of opposite polarity, which are not available from the single energy cell usually provided in a wristwatch. Furthermore, simultaneous writing and erasing results in a voltage $V_3=|V_1|+|V_2|$ existing between a segment to be written and a segment to be erased. This voltage V_3 being sufficiently high to cause undesirable electrochemical reactions leading to degradation of the display.

In accordance with one aspect of the invention there is provided a driver circuit for an electrochromic display cell having at least one segment electrode and a counter electrode, said driver circuit comprising circuit means for providing a command write signal and a command erase signal; alternating signal means for applying to said counter electrode an alternating signal having a write signal level and an erase signal level; switch means coupled to said circuit means and to said alternating signal means and controlled by said command write signal and said write signal level to provide a voltage to said segment electrode in time coincidence with said write signal level being applied to said counter electrode for providing a write potential between said counter electrode and said segment electrode, said switch means also being controlled by said command erase signal and said erase signal level to provide a voltage to said segment electrode in time coincidence with said erase signal level being applied to said counter electrode for providing an erase potential between said

counter electrode and said segment electrode.

The term "segment" as used throughout the specification and claims refers to a portion of a digit or a digit or hands of an analog display or entire digits or other indicating indicia which can be caused to fade-in and fade-out substantially simultaneously.

The circuit of the invention thus enables fade-in and fade-out of selected segments of a segmented alpha-numerical display to be effected when changing the character to be displayed.

The writing and erasing voltages are applied alternately in rapid succession during time intervals which are short compared to those required for complete writing or erasing. In each of these several successive intervals, only partial writing or erasing is achieved. In this manner, the illusion of simultaneous writing and erasing is created, and the appearance of ambiguities or meaningless displays is minimized or entirely avoided. Furthermore, only a single voltage source is required which is alternately switched in rapid succession between the write condition in which the counter electrode is positive and the segment electrodes to be written are negative, and the erase condition in which the counter electrode is negative and the segment electrodes to be erased are positive.

In accordance with a further aspect of the invention, there is provided a method of updating the information being displayed by an electrochromic display cell having a plurality of segment electrodes grouped to form indicia and a counter electrode, said method comprising applying to said counter electrode an alternating signal that alternates between a write signal level and an erase signal level; applying for a duration to effect partial erasing of a selected first segment electrode a voltage in time coincidence with said erase signal level being applied to said counter electrode to effect by the coincidence an erase potential between the selected first segment electrode and the counter electrode; applying for a duration to effect partial writing of a selected second segment electrode a voltage in time coincidence with said write signal level being applied to said counter electrode to effect by the coincidence a write potential between the selected second segment electrode and the counter electrode; applying the write and erase potentials across the selected segment electrodes and the counter electrode during alternate levels of each cycle of said alternating signal for several cycles of the alternating signal to fade-in and fade-out the selected segment electrodes.

In order that the invention may be better understood an embodiment thereof will now be described by way of example only and with reference to the accompanying drawings in which:—

Figure 1 is a plan view of a known seven segment electrochromic display indicating the manner in which displayed alpha-numeric information is updated;

Figure 2 is a logic circuit diagram of a driver circuit employed in an embodiment of the present invention;

Figure 3 is a pulse train diagram showing the coincidence activation period of the pulses applied to the display;

Figure 4 is a general block diagram of the logic circuitry employed in the embodiment of Figure 2 to provide selective alpha-numeric display information in a timepiece; and

Figure 5 is a logic circuit diagram of the decoder used to provide the write/erase command to the driver circuit shown in Figures 2 and 3.

In order to give better understanding of the present invention, a brief description will first be made with reference to Figure 1, of the manner of changing the information being displayed by the known electrochromic display devices.

In updating digital electrochromic displays, it is preferable to write or erase only those segment electrodes of the seven segment array which require change. The segment electrodes which are common to both the old and the new alpha-numeric character are not switched, and remain in their previous state because of the memory of the display. This is shown in Figure 1. The advantage gained, thereby, is a saving in current consumption.

The display is preferably an electrochromic device using a well-known phenomenon such as is described in U.S. Patent Nos. 3,704,057, 3,708,220 and 3,807,832.

Briefly stated, these electro-optical devices exhibit the phenomenon whereby the light transmitting ability of the display cell is varied by the application of an electric field across the electrochromic material to turn it darker, for example decreasing its light transmitting ability over the area of the activated segment electrode. The activated segment electrode retains, in a memory-like manner, this varied light transmitting characteristic till the application of a bleaching electric field.

In prior art, writing and erasing of electrode-segments was effected in a visually distinctive way. For example, either the segments to be erased were first completely bleached and then the segments to be written were coloured, or vice versa. Because of the relatively slow response of

the electrochromic display and to provide complete colouring and bleaching, the appearance of the alpha-numeric character(s) during transition of the displayed information was, prior to the present invention, confusing or misleading.

This undesirable characteristic of the prior art electrochromic display devices will be better understood by reference to Figures 1A and 1B in which is shown the transition or update of the digital number 6 to 7. The first method, shown in Figure 1A, is to erase the segments D, E, F and G which are not common to both digits. This produces the confusing ERASE display between START of update, i.e. the digit to be changed, and the WRITE display in which the selected segment(s) B has been coloured to form the updated digit.

If, on the other hand and with reference to Figure 1B, the updating sequence is reversed, i.e. first write and then erase, then segment B is coloured which results in the misleading WRITE display which illustrates the numeric digit eight.

Reference will now be made to Figures 2 and 3 which together show how the segments to be written and erased, i.e. update of the display, are caused to fade-in and fade-out in accordance with the present invention. The electrochromic display cell 8 comprises an electrochromic material 9 disposed between a plurality of segment electrodes X, Y and counter electrode 10. Typically, electrochromic displays comprise a plurality of alpha-numeric characters formed by seven segment arrays such as is shown in U.S. Patent No. 3,839,857. For simplicity and clarity the following explanation of the invention will be directed to the simultaneous fade-in and fade-out of two segment electrodes X, Y, it being understood that the number of segment electrodes, i.e. number and type of display characters, which can be faded-in and faded-out is substantially unlimited.

The counter electrode 10 is connected to receive a pulse signal ϕ from, for example, a chopping frequency generator 11 or an output of a stage of a frequency divider such as is found in electronic watches. The pulse signal ϕ is, for example, a unipolarity alternating voltage which varies in value between zero, e.g., a logic "0", and some positive level, e.g., a logic "1", at a predetermined frequency. Each segment electrode X, Y is connected through first switch means comprising switches 12, 12' such as transmission gates, to a write voltage 13, 13' and through second switch means comprising switches 14, 14' to an erase voltage 15, 15'. The write voltage 13, 13' is, for example, at battery negative or logic "0" level and the erase voltage 15, 15' is, for example, at battery positive or logic "1" potential.

Write and erase switch control devices 16, 16' and 17, 17' such as two input logic "AND" gates are connected to each of the switches 12, 12', 14, 14' respectively to selectively enable the switches in conjunction with the signal ϕ being applied to the counter electrode 10, to cause a write or erase potential to be established across the electrochromic material in the area of the selected (activated) segment electrode. Switch control devices 16, 16' each have one of their inputs 18, 18' coupled to the signal ϕ and their other input 19, 19' coupled to command write signal means, for example, a decoder. Switch control devices 17, 17' each have one of their inputs 20, 20' coupled to a signal $\bar{\phi}$ which is inverted with respect to the ϕ signal, and their other input 21, 21' coupled to command erase signal means. The write and erase two input AND gate switch control devices 16, 16', 17, 17' are enabled only when there is coincidence of a high or logic 1 on both of their respective two inputs.

In operation, if segment electrodes X and Y are to be written and erased, respectively, an enable write (seg.) X and erase (seg.) Y signal command is applied to the respective switch control devices 16 and 17'. The logic "AND" gate switch control devices 16, 17' and then alternately enabled by the signals ϕ and $\bar{\phi}$ to, thereby, activate or close switches 12 and 14' during a respective write and erase half-cycle or portion of the signal ϕ being applied to the counter electrode 10. A segment electrode X write potential is provided by coincidence of a write signal ϕ such as a positive or logic "1" on the counter electrode 10 and a write voltage 13 such as a negative or logic "0" on segment electrode X. Since switch control device 16 and switch 12 are, also, enabled when the signal ϕ is at the write (logic "1") voltage, coincidence occurs during the write portion or phase of the signal ϕ. Then the signal ϕ alternates to its erase (logic "0") voltage, the signal $\bar{\phi}$ is at a logic "1" voltage due to the action of inverter 22, which causes switch control device 17' and, therefore, switch 14' to be enabled. With switch control 14' enabled, the erase (positive) voltage 15' is applied to segment electrode Y, and, coincidentally, the erase (negative or logic "0") voltage or level of the signal ϕ is applied to the counter electrode 10 to, thereby, provide or establish an erase (polarity) potential difference between segment electrode Y and the counter electrode.

The frequency of the signal ϕ and, therefore, the signal $\bar{\phi}$ is predetermined

such that during a cycle thereof the write and erase potentials provided have a duration or duty-cycle such that only partial or incomplete writing and erasing of the selected segments is effected. Therefore, the segments to be written and erased are caused to partially fade-in and fade-out, respectively, during each cycle of the signals ϕ and $\bar{\phi}$, and to completely fade-in and fade-out after several cycles so as to give the appearance of simultaneous transition or update of the display characters. In this embodiment, a frequency range of, for example, 2 HZ to several KHZ may be successfully used.

The duty cycle or period during which the erase and write potentials are applied may be varied, i.e. they can be applied for different times or numbers of cycles of oscillation of the alternating signal, to further improve the appearance of the display during updating.

Referring now to Figure 4, a block diagram of the electronic circuitry for a timepiece embodying this invention is shown. The display is actuated by electronic circuitry which generally consists of a frequency standard 23, frequency dividing unit 24, a minutes counter 25, an hours counter 26, a decoder 27 and the driver circuit 28. Since circuitry for performing these functions is well known to those skilled in the art such as is described in U.S. Patent No. 3,754,392 exhaustive details thereof are omitted.

Referring now to Figure 5, a more detailed logic circuit of a decoder for providing the write and erase commands to the driver circuit shown in Figures 2 and 4 will now be described. The operation may best be understood by first considering the decoder logic circuit 29 for one segment electrode, it being understood that each segment electrode of each seven segment display digit has a similar decoder circuit arrangement.

In an electronic watch, for example, the seven segment decoder 30 is connected through a display select circuit 31 to an hours and minutes counter and month and date counter 32, 33. Each output of the seven segment decoder 30 is connected to a segment decoder 29, 29', etc. On start up, the Q output of the D type flip-flop 34 latches in a low level and, therefore, input 35 of "Exclusive-OR" gate 36 is low. The other input 37 of "Exclusive-OR" gate 36 is connected to a respective output of the seven segment decoder 30. The segment electrode(s) to be turned on, is enabled by a high or logic "1" on the respective output 38 of the seven segment decoder 30 which is compared with the Q output of flip-flop 34 and causes a high or logic "1" at the output of "Exclusive-OR" gate 36. This high is on the output of "Exclusive-OR" gate 36 is coupled to the input of the succeeding "OR" gate 39 which causes its output to go high. The W (write) and E (erase) "AND" gates are therefore provided with a high input. The other input 40 of the W gate being coupled to the respective decoder 38 is high for the segment electrode(s) that is to be turned on, resulting in a command write signal to the driver.

As soon as the display update of the segment electrode(s) is completed, a pulse is applied to the clock input of flip-flop 34. The Q output then indicates the state of the segment electrode, as the information on the D input, which corresponds to the seven segment decoder output, is clocked in.

With a change in the state of the output from the seven segment decoder, i.e. from a write to erase enable, input 41 of the E gate goes high and input 40 of the W gate goes low. Since the output of "OR" gate 39 is high, the E gate is enabled to provide a command erase signal to the decoder. In other words, if the output of the seven segment decoder goes high, the W gate gets two high inputs and the driver as shown in Figure 2 gets an erase command.

As before, when the display change or update is complete, a clock pulse transfers this new information to the Q output of the flip-flop 34.

During a slewing operation, e.g. when the watch wearer changes the time being displayed, this procedure of transferring the information through the flip-flop latches is avoided by tying the "refresh" input of the "OR" gate, of the digit being slewed, high. Then the write and erase commands are supplied by the segment outputs, as they are connected to the W and E gate inputs.

The "refresh" can also be used periodically to maintain an even display contrast by refreshing the display memory.

The above described circuitry thus enables an electrochromic display means to be provided which causes substantially simultaneous fade-in of one or more segments to be written and fade-out of one or more segments to be erased. Furthermore means are provided for updating an electrochromic display which minimizes or eliminates ambiguities or meaningless characters during the updating transition. In addition, means are provided for rapidly alternating write and erase operations using only a single voltage source.

The above described apparatus thus provides the illusion of simultaneous writing and erasing.

WHAT WE CLAIM IS:—

1. A driver circuit for an electrochromic

such that during a cycle thereof the write and erase potentials provided have a duration or duty-cycle such that only partial or incomplete writing and erasing of the selected segments is effected. Therefore, the segments to be written and erased are caused to partially fade-in and fade-out, respectively, during each cycle of the signals ϕ and $\bar{\phi}$, and to completely fade-in and fade-out after several cycles so as to give the appearance of simultaneous transition or update of the display characters. In this embodiment, a frequency range of, for example, 2 HZ to several KHZ may be successfully used.

The duty cycle or period during which the erase and write potentials are applied may be varied, i.e. they can be applied for different times or numbers of cycles of oscillation of the alternating signal, to further improve the appearance of the display during updating..

Referring now to Figure 4, a block diagram of the electronic circuitry for a timepiece embodying this invention is shown. The display is actuated by electronic circuitry which generally consists of a frequency standard 23, frequency dividing unit 24, a minutes counter 25, an hours counter 26, a decoder 27 and the driver circuit 28. Since circuitry for performing these functions is well known to those skilled in the art such as is described in U.S. Patent No. 3,754,392 exhaustive details thereof are omitted.

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The "refresh" can also be used periodically to maintain an even display contrast by refreshing the display memory.

The above described circuitry thus enables an electrochromic display means to be provided which causes substantially simultaneous fade-in of one or more segments to be written and fade-out of one or more segments to be erased. Furthermore means are provided for updating an electrochromic display which minimizes or eliminates ambiguities or meaningless characters during the updating transition. In addition, means are provided for rapidly alternating write and erase operations using only a single voltage source.

The above described apparatus thus provides the illusion of simultaneous writing and erasing.

WHAT WE CLAIM IS:—

1. A driver circuit for an electrochromic

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display cell having at least one segment electrode and a counter electrode, said driver circuit comprising circuit means for providing a command write signal and a command erase signal; alternating signal means for applying to said counter electrode an alternating signal having a write signal level and an erase signal level; switch means coupled to said circuit means and to said alternating signal means and controlled by said command write signal and said write signal level to provide a voltage to said element electrode in time coincidence with said write signal level potential between said counter electrode and said segment electrode, said switch means also being controlled by said command erase signal and said erase signal level to provide a voltage to said segment electrode in time coincidence with said erase signal level being applied to said counter electrode for providing an erase potential between said counter electrode and said segment electrode.

2. A drive circuit as claimed in claim 1, wherein the switch means comprises a first switch connected between a first voltage source and said segment electrode, a first AND circuit having an output coupled to said first switch and a first input coupled to said circuit means providing a command write signal and a second input coupled to said alternating signal means, a second switch connected between a second voltage source and said segment electrode, a second AND circuit having an output coupled to said second switch and a first input coupled to said circuit means providing a command erase signal and at a second input coupled through a signal inverter means to said alternating signal means.

3 A driver circuit as claimed in claim 1 or 2, wherein the electrochromic display cell exhibits colouration and bleaching by control of the polarity of an applied electric field for a substantially predetermined duration, and wherein the alternating signal varies between said write signal level and said erase signal level and having a period such that each write signal level has a duration such that said write potential is applied for a duration which is less than the predetermined duration required to effect a complete colouration and each erase signal level has a duration such that said erase potential is applied for a duration which is less than the predetermined duration required to effect complete bleaching, the circuit means selectively providing a command write signal and a command erase signal having a duration such as to enable said switch means over a several cycle duration of the alternating signal to selectively effect a complete colouration or a complete bleaching of the segment electrode.

4. A driver circuit as claimed in claim 1, 2 or 3 wherein the switch means is connected to a voltage source to selectively couple said voltage source between said segment electrode and said counter electrode for providing thereby said write potential having a first plurality, said switch means being operable to reverse the coupling of said voltage source across said segment and said counter electrode for providing said erase potential having a second polarity.

5. A driver circuit as claimed in any one of the preceding claims wherein the alternating signal is a square wave alternating between a first state corresponding to said write signal level and a second state corresponding to said erase signal level.

6. A driver circuit as claimed in any one of the preceding claims wherein each segment electrode is part of an alpha-numeric character.

7. A driver circuit as claimed in any one of claims 1 to 5, wherein each segment electrode is an alpha-numeric character.

8. An electronic timepiece comprising a driver circuit as claimed in any one of the preceding claims, said electrochromic display cell having a plurality of said segment electrodes grouped to form at least one digit, means for providing electrical signals representing time information, and display control means including said switch means, said display control means being responsive (a) to said signals representing time information to display an indication of the correct time at least to one digit, (b) to said alternating signal and said command write signal to provide a write voltage to a first segment electrode in coincidence with said write signal level being applied to said counter electrode whereby a write potential is provided between said counter electrode and said first segment electrode, and (c) to said alternating signal and said command erase signal to provide an erase voltage to a second segment electrode in coincidence with said erase signal level being applied to said counter electrode whereby an erase potential is provided between said counter electrode and said second segment electrode.

9. An electronic timepiece as claimed in claim 8, wherein the display control means alternates the potential-polarity across the electrochromic display cell for providing the write potential-polarity and the sense potential-polarity alternately.

10. A method of updating the information being displayed by an electrochromic display cell having a plurality of segment electrodes grouped to form indicia and a counter electrode, said

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method comprising applying to said counter electrode an alternating signal that alternates between a write signal level and an erase signal level; applying for a duration to effect partial erasing of a selected first segment electrode a voltage in time coincidence with said erase signal level being applied to said counter electrode to effect by the coincidence an erase potential between the selected first segment electrode and the counter electrode; applying for a duration to effect partial writing of a selected second segment electrode a voltage in time coincidence with said write signal level being applied to said counter electrode to effect by the coincidence a write potential between the selected second segment electrode and the counter electrode; applying the write and erase potentials across the selected segment electrodes and the counter electrode during alternate levels of each cycle of said alternating signal for several cycles of the alternating signal to fade-in and fade-out the selected segment electrodes.

11. A driver circuit for an electrochromic display cell, substantially as hereinbefore described with reference to Figure 2 to 5 of the accompanying drawings.

12. A method of updating information being displayed by an electrochromic display cell, as claimed in claim 10, substantially as hereinbefore described.

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