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(54) Title: PAGE MODE ERASE IN A FLASH MEMORY ARRAY

(57) Abstract

In a sector in a flash memory array PAGE ERASE and MULTIPLE PAGE ERASE modes of operation are provided. In the PAGE ERASE and MULTIPLE PAGE ERASE modes of operation, a preferred tunneling potential of approximately -10 Volts is applied to the gates of the flash memory cells on the row or rows being selected for erasure, and the bitlines connected to the drains of the flash memory cells are driven to a preferred voltage of approximately 6.5 Volts. To reduce the unintended erasure of memory cells in rows other than the selected row or rows a preferred bias voltage of approximately 1 to 2 Volts is applied to the gates of all the flash memory cells in the rows other than the selected row or rows.

