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(54) TIME DIVISION MULTIPLEX TRANSMISSION SYSTEM /

(71) We, TERASAKI DENKI SANGYO KABUSHIKI KAISHA, a Japanese corporation, of 3-3, Showa-cho 5-chome, Abeno-ku, Osaka-shi, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

10 The present invention relates to a time division multiplex transmission system.

A time division multiplex transmission system for data communication among transmitters and receivers in a synchronized manner has been proposed and put into practical use. The data to be communicated may comprise a plurality of contact signals obtainable from limit switches, relay contacts, push button switches and the like or a plurality of output signals obtainable from a semiconductor circuits such as a transistor circuit and the like. Such signals are often referred to as a digital signal or a binary signal.

For the purpose of synchronization in the system, a train of clock pulses is utilized and the data is communicated in synchronism with the clock pulses. More specifically, a typical time division multiplex transmission system comprises a plurality of transmitters and a plurality of receivers which are adapted to be operable in synchronism with the clock pulses and a transmission path for interconnection thereof. While the clock pulses are transmitted on the transmission path, transmitters and receivers are selected in order and data is transmitted and received between the selected transmitter and receiver.

Fig. 1A shows wave forms of a train of clock pulses and a train of data signals on an enlarged time scale, while Fig. 1B shows wave forms of the same clock pulses and data signals on a reduced time scale. It is pointed out that the Fig. 1A graph is aimed to show in detail the data to be transmitted only from a few transmitters, whereas the Fig. 1B graph is aimed to show the data to be transmitted by all the transmitters in the system. With particular reference to Fig. 1A, it will be appreciated that

the system has been structured such that a plurality of transmitters are sequentially selected each for a predetermined time period while each transmitter is adapted to transmit eight different digital signals. More specifically, when the first transmitter is selected, a parallel input signal of eight bit positions is connected into a series signal of eight bit positions as a function of the clock pulses and is transmitted on the data signal transmission line. After transmission of the data signal for the first transmitter, the second transmitter is selected and a further data signal of eight bit positions is transmitted similarly. The data signal transmitted by the first transmitter is received by the corresponding first receiver controlled to be mated therewith. Thereafter, the second receiver is controlled to be mated with the second transmitter to receive the second data signal. Thus, data communication, i.e. transmission and reception of the data signals, is carried out in sequence between the transmitters and receivers. After transmission and reception of the data signals by all the transmitters and receivers in the system is over, the clock pulses are discontinued for a given time period, such that a train of clock pulses is followed by a predetermined intermission period. After the lapse of that time period, the clock pulses are again transmitted, whereby transmission and reception of the data signals is carried out again in turn starting from the first transmitter and receiver.

The data signal transmission described in the foregoing starting from the first selected transmitter and receiver and ending at the finally selected transmitter and receiver is referred to as one data signal transmission cycle. With particular reference to Fig. 1B, it will be appreciated that such a data signal transmission cycle is carried out repeatedly, with intermission of data communication for a given time period therebetween. More specifically, continual connection is not made between each input terminal of the transmitter and the corresponding output terminal of the receiver, but rather intermittent connection of each input and output out of a plurality of inputs

and outputs takes place, in turn, for a given time period. In other words, time is divided so as to be assigned to each input and output, so that the same transmission line is shared to perform the transmission and reception of the data signal between each input and output out of a plurality of inputs and outputs.

The system thus described for communicating a plurality of data signals by the use of a common transmission line using time division is referred to as a time division multiplex transmission system.

In a typical conventional time division multiplex transmission system, a clock pulse generator for generating clock pulses for control of time division is provided in each of the transmitters and receivers. Alternatively, a system is structured such that the clock pulses are generated in each of the transmitters and receivers by the use of a carrier wave of the data signal. However, since the conventional system has no independent clock pulse transmission line, it suffers from various shortcomings.

Firstly, since each of the transmitters and receivers in a conventional system comprises a respective inherent oscillator used as a clock pulse generator, lack of stability of the characteristics of the respective oscillators with respect to the ambient conditions, such as temperature, humidity, and the like causes problems, if the phase of the clock pulses is shifted because of variation of the respective oscillation frequency, synchronization of the operation of the system cannot be maintained and the system becomes inoperative. On the other hand, with the system utilizing the carrier wave of the data signal for the purpose of synchronization, it is necessary to employ operations such as modulation and demodulation, which complicates the structure of the system. Furthermore, the conventional system is vulnerable to failure of synchronization because of disturbance such as noise and the like.

Another problem is that since the switching speed of channels for multiplex transmission cannot be changed as desired with a conventional system, the switching speed is fixed and cannot be adjusted.

A further problem encountered with a conventional system is that since the number of clock pulses in each train of clock pulses cannot be adjusted, the number of digital signals being communicated for each transmitter-receiver pair is half way fixed and cannot be increased or decreased. Thus, with a conventional system, expandibility of the number of digital signals being processed for each data signal cannot be expected.

With a conventional system, the data signal transmission and the reset signal transmission are achieved by the same transmission line. Therefore, it is necessary that the system is structured so as to discriminate such signals,

which complicates the circuit configuration of the system but nevertheless leaves it subject to disturbance.

It is thus desirable to avoid these problems by separately transmitting clock pulses to the transmitters and receivers, and it is also desirable to provide a way in which disturbance of or interference with the clock pulses can be avoided or reduced.

In accordance with the invention there is provided a time division multiplex transmission system comprising:

data signal transmission path means;
clock pulse transmission path means;
means for separately and concurrently transmitting along said clock pulse transmission path means first and second trains of clock pulses, the pulses of said first and second trains having opposite phases; and

at least one transmitter and at least one receiver between which data can be communicated along said data signal transmission path means, the or each transmitter and receiver being connected to said clock pulse transmission path means and being arranged to be synchronized in their operation by synchronizing pulses derived from the difference between the values of said first and second trains of clock pulses.

In the preferred embodiment described below, single phase synchronizing clock pulses are generated locally in the respective transmitter or receiver in response to the first and second trains of clock pulses transmitted through a clock pulse transmission line which is separate from a data signal transmission line, and any disturbances such as noise occurring in the clock pulse transmission line can be eliminated in the local generation of the single phase clock pulses in the respective transmitter or receiver. Since the generated single phase synchronizing clock pulses are immune to external disturbance occurring in the clock pulse transmission line, improved synchronization can be achieved in the transmission system.

Preferably, the duration of each of said first and second trains of clock pulses covers a plurality of station selection time periods, such that in each period there is provided a plurality of clock pulses required for communication of said data signal of said plurality of bits. A plurality of transmitters is provided, each transmitter further comprising means responsive to said single phase clock pulses for providing an enabling signal for identifying a predetermined one of said station selection time periods to be uniquely allotted to the transmitter, said delivering means being arranged to be enabled in response to said enabling signal. Also, a plurality of receivers is provided, each receiver further comprising means responsive to said single phase clock pulses for providing an enabling signal for identifying a predetermined one of said station selection time periods to be uniquely allotted to the receiver,

said receiving means being arranged to be enabled in response to said enabling signal. At least one pair comprising a preselected one of said plurality of transmitters and a preselected one of said plurality of receivers is arranged so that said preselected transmitter and said preselected receiver are preset to identify the same station selection time period, whereby said preselected transmitter and said preselected receiver establish a mating relation during the said same station selection time period for communication of the data signal therebetween.

Preferably, the transmission of said first and second trains of clock pulses is interrupted for a predetermined intermission time period after each data signal transmission cycle, and each of said transmitters and receivers further comprises means responsive to the occurrence of a predetermined intermission time period for returning to an initial condition said enabling signal providing means. As a result, complete synchronism of all the transmitters and receivers in the whole system can be achieved with ease.

In a preferred embodiment the number of clock pulses in one data signal transmission cycle can be varied with ease, whereby the number of transmitter-receiver pairs to be mated with each other in said transmission cycle can be varied with ease.

Also in the preferred embodiment, station selection in the transmitters and receivers can be achieved using similar circuit configurations, with the result that the circuit configuration of the whole system can be made simple.

An advantage of the preferred embodiment of the present invention is that since the first and second trains of clock pulses are provided by a generator which is common to the whole system and the single phase clock pulses are generated, in response to these trains of clock pulses, locally in each of the transmitters and receivers, which single phase clock pulses are utilized for synchronized multiplex operation in the respective transmitters and receivers, stability of the frequencies of the clock pulses does not cause problems with the synchronization of the system.

An arrangement embodying the invention will now be described by way of example with reference to the accompanying drawings, in which:

Fig. 1A shows the wave forms of a train of clock pulses and a train of data signals on an enlarged time scale;

Fig. 1B shows the wave forms of the same clock pulses and data signals on a reduced time scale;

Fig. 1 is a block diagram of one embodiment of a time division multiplex transmission system in accordance with the present invention;

Fig. 2A is a block diagram of the clock pulse generator 1;

Fig. 2B shows the wave forms of signals at various points in the Fig. 2A diagram;

Fig. 3 shows in more detail the structure of the wave form shaper 5 in the Fig. 1 embodiment;

Fig. 4 shows the wave forms of the incoming in-phase and opposite phase clock pulses to be received by the wave form shaper 5 and the output clock pulses from the amplifier 5a;

Fig. 5A is a detailed block diagram of the selection circuit 6 in the transmitters and receivers;

Fig. 5B is a schematic diagram of one embodiment of the parallel/serial converter 9;

Fig. 5C shows the wave forms of the station selection signal c2 and the data signal c3 with respect to the clock pulse c1;

Fig. 5D is a schematic diagram of one embodiment of the serial/parallel converter 10;

Fig. 6A is a detailed block diagram of one embodiment of the rectangular wave generator 1a;

Fig. 6B shows the wave forms of signals at various points in the Fig. 6A embodiment;

Fig. 7A is a block diagram of one embodiment of the reset signal detector 14;

Fig. 7B shows the wave forms of signals at various points in the Fig. 7A embodiment;

Fig. 8A is a block diagram of bidirectional multiplex transmission system in accordance with the present invention; and

Fig. 8B shows the wave forms of signals at various points in the Fig. 8A diagram.

Fig. 1 is a block diagram of one embodiment of a time division multiplex transmission system in accordance with the present invention. Referring to Fig. 1, the embodiment shown comprises a plurality of transmitters 3a, 3b, and a plurality of receivers 4a, 4b,, each being structured for communication of a data signal of a plurality of bits and coupled to a data signal transmission line 12 and a clock pulse transmission line 2 connected to receive clock pulses from a common clock pulse generator 1. It is pointed out that the transmitter 3a and the receiver 4a have been illustrated in some detail while the remaining transmitters and receivers have been illustrated in a simplified manner for facility of illustration. Only a single common clock pulse generator is provided in the whole system, for maintaining synchronization among the transmitters and receivers. The clock pulse generator 1 is structured to generate a succession of clock pulse trains, each train including a plurality of station selection time periods, each period comprising the same predetermined number of clock pulses as the said plurality of bits. Preferably, the clock pulse generator 1 is structured such that the number of clock pulses in each clock pulse train is variable and a predetermined intermission time period is provided between consecutive pulse trains. The clock pulse generator 1 is structured to generate multiphase clock pulses or two-phase pulses. The clock pulse generator 1 may com-

prise any type of oscillator, such as a crystal oscillator, an RC oscillator, an astable multivibrator, or the like, wherein the generated wave form is converted to a rectangular wave form.

Fig. 2A is a block diagram of the clock pulse generator 1 and Fig. 2B shows the wave forms of the signals at various points in the Fig. 2A diagram. Referring to Fig. 2A, the clock pulse generator 1 is arranged to provide two-phase clock pulses, i.e. clock pulses of in-phase and opposite-phase. To that end, the generator 1 shown comprises a rectangular wave generator 1a, a buffer amplifier 1c directly coupled to the output of the rectangular wave generator 1a, and another buffer amplifier 1d coupled through an inverter 1b to the output of the rectangular wave generator 1a. The rectangular wave form output obtainable from the rectangular wave generator 1a is directly applied to the buffer amplifier 1c, and, through the inverter 1b applied to the buffer amplifiers 1d. With simultaneous reference to Fig. 2B, the rectangular wave generator serves to generate a rectangular wave form p. The in-phase clock pulse q1 is obtained by amplifying the said rectangular wave form with the buffer amplifier 1c, while the opposite-phase clock pulse q2 is obtained by inverting the polarity of the said rectangular wave form through the inverter 1b and by amplifying the output from the inverter 1b with the buffer amplifier 1d.

The two-phase clock pulses thus generated by the generator 1 are transmitted through the clock pulse transmission line 2 provided as a special purpose line. The clock pulse transmission line 2 of the embodiment shown comprises two lines for transmission of the in-phase clock q1 and the opposite-phase clock q2. The two-phase clock pulses thus transmitted are received by the transmitters 3a, 3b, and receivers 4a, 4b, Now returning to Fig. 1, the transmitter 3a is shown comprising a wave form shaper 5 for processing the said two-phase clock pulses for the purpose of demodulating the original trains of clock pulses, a counter 7 for counting the number of clock pulses in each clock pulse train, a reset signal detector 14 responsive to the succession of clock pulse trains to detect the intermission time period between consecutive clock pulse trains to provide a reset signal to the counter 7, a decoder 8 coupled to the counter 7 for decoding the count output of the counter 7 for generating an enabling signal identifying a predetermined station selection time period uniquely allotted to its own transmitter 3a, and a parallel/serial converter 9 responsive to the enabling signal by way of the decoded output from the decoder 8 to be enabled to convert an input of a plurality of parallel bits 11a, 11b, 11c, 11n into a series bit signal as a function of the demodulated clock pulses. The receiver 4a is of substantially the same structure as that of the transmitter 3a, except that

the parallel/serial converter 9 has been replaced by a serial/parallel converter 10. The serial/parallel converter 10 is responsive to the enabling signal by way of the decoded output of the decoder 8 to be enabled to convert the series bit signal transmitted through the data signal transmission line 12 into an output of a plurality of parallel bits 13a, 13b, 13c, 13n as a function of the demodulated clock pulses obtainable from the wave form shaper 5. It is pointed out that the counter 7 and the decoder 8 constitutes a station selection circuit 6.

Fig. 3 shows in more detail the structure of the wave form shaper 5. Referring to Fig. 3, the wave form shaper 5 typically comprises a differential amplifier 5a, wherein the differential voltage between the said in-phase clock pulses q1 and the opposite-phase clock pulses q2 is amplified to provide a single phase demodulated synchronizing clock pulse q3. According to the embodiment shown, any noise coming into the clock pulse transmission line 2 appears with the same polarity in both the in-phase clock pulse transmission line and the opposite-phase clock pulse transmission line, so that the noise components on both transmission lines offset each other, with the result that the noise has no influence on the output wave form from the wave form shaper 5.

More specifically, Fig. 4 shows the wave forms of the incoming in-phase and opposite-phase clock pulses to be received by the differential amplifier 5a and the output clock pulses from the amplifier 5a. Referring to Fig. 4, the wave forms are shown comprising a noise component occurring with the same polarity in both the in-phase and opposite-phase clock pulses (a) and (b), respectively. However, a well-shaped single phase demodulated synchronizing clock pulse (c) is obtained by means of the wave form shaper 5 with the noise component removed.

Fig. 5A shows a detailed block diagram of the station selection circuit 6 in the transmitters and receivers. As described previously, the station selection circuit comprises the counter 7 and the decoder 8 as major elements. Referring to Fig. 5A, the counter 7 is shown as comprising a seven-digit binary counter by way of an example, the three least significant bit positions forming a first counter means for counting clock pulses, and the four more significant bit positions forming a second counter means for counting station selection time periods. The decoder 8 is shown as comprising a binary-decimal converter for converting the four-bit binary number in the second counter means formed by the four more significant bit positions in the counter 7 into decimal numbers 0 through 15 of individual parallel bit outputs. Referring to Fig. 5A, the block 9 (10) is shown to indicate either the parallel/serial converter 9 of a transmitter or the serial/parallel converter 10 of a receiver,

as the case may be. More specifically, the outputs from the bit positions 3 through 6, i.e. the fourth through seventh bit positions, of the counter 7 are connected, in parallel fashion, to the decoder 8, such that the contents in the bit positions 3 through 6 of the counter 7 may be converted into a decimal number to be represented as the corresponding one of the individual decimal number outputs from the decoder 8.

It will be appreciated that the contents in the bit positions 3 through 6, i.e. the fourth through seventh bit positions, of the counter 7 change each time eight single phase clock pulses q3 are received by the counter 7. In the case where the contents in the bit positions 3 through 6 of the counter, are all logic zero, the output from the decimal number 0 of the decoder 8 becomes logic one, while the remaining decimal number outputs of the decoder 8 are all logic zero. In the case where the bit position 3 of the counter 7 becomes logic one while the bit positions 4 through 6 of the counter 7 become logic zero, the outputs from the decimal number 1 of the decoder 8 becomes logic one while the remaining decimal number outputs of the decoder 8 are all logic zero. Similarly, in the case where the bit position 4 of the counter 7 becomes logic one while the bit positions 3, 5 and 6 become logic zero, the output from the decimal number 2 of the decoder 8 becomes logic one while the remaining decimal number outputs of the decoder 8 are all logic zero. In other words, regarding the contents in the bit positions 3 through 6 of the counter 7 as a four-bit binary number, the said binary number is converted into a decimal number by way of the corresponding one of a plurality of individual bit parallel decimal number outputs 0 through 15, whereby only one of the decimal number outputs of the decoder 8 corresponding to the converted decimal value becomes logic one, while the remaining decimal number outputs of the decoder 8 all become logic zero. A predetermined one of these bit parallel decimal number outputs of the decoder 8 is in advance uniquely selected or allotted to each of the transmitters and receivers, so that the said preselected decimal number output is applied to the converter 9 or 10 as an enabling signal thereof. In the embodiment shown in Fig. 5A, the output of the decimal number 2 of the decoder 8 has been preselected. Therefore, the decimal number output 2 of the decoder 8 becomes logic one in the case where the bit position 4, i.e. the fifth bit position, of the counter 7 becomes logic one while the bit positions 3, 5 and 6 become logic zero, whereby the parallel/serial converter 9 or the serial/parallel converter 10 receives such an enabling output from the decimal number output 2 of the decoder 8 as a station selection signal. As described previously, the contents in the bit positions 3 through 6 of the counter 7 change

each time eight single phase clock pulses are received thereby. Accordingly, the station selection signal is kept supplied to the converter 9 or 10 for a station selection time period during which eight clock pulses are received by the counter 7. In other words, each time eight clock pulses are transmitted, the transmitters and receivers are selected in turn. The order of selection of the stations is determined by which decimal number output of the decoder 8 is selectively connected to the parallel/serial converter 9 or the serial/parallel converter 10.

Fig. 5B is a schematic diagram of one embodiment of the parallel/serial converter 9. The converter 9 shown comprises an AND gate 9a connected to receive the single phase clock pulses and the station selection signal to provide a train of clock pulses if and when the station selection signal is received, a switch 9b having a plurality of stationary contacts 90, 91, 92, 97 connected to a plurality of bit parallel inputs 11a, 11b, 11c, 11h, respectively, and a movable contact switchable in turn to the respective stationary contacts as a function of the incoming clock pulses, and an AND gate 9c connected to receive the output from the movable contact of the switch 9b and the station selection signal so as to deliver the output to the data signal transmission line 12 from the movable contact of the switch 9b if and when the station selection signal is received.

In operation, when a station selection signal is obtained from the station selection circuit 6 implemented by the decoder 8 and the counter 7, the AND gate 9a is enabled, whereby the switch 9b becomes operative in synchronism with the clock pulses, so that the switch 9b is turned sequentially to the stationary contacts 90 through 97, thereby to withdraw the input signals received by the input terminals 11a through 11h, respectively. Since the AND gate 9c has also been enabled, the input signals 11a through 11h are sequentially transmitted over the data signal transmission line 12 as the switch 9b is turned to the respective stationary contacts 90 through 97, respectively. If and when eight clock pulses have been received, the station selection signal is no longer obtained from the corresponding decimal number output of the decoder 8, which means that the station in question is not selected. Instead, another station is selected in the same manner.

Fig. 5C shows the wave forms of the station selection signal c2 and the data signal c3 with respect to the clock pulses c1.

In the foregoing, a case was described where a plurality of bit parallel digital signals 11a through 11h are applied to the parallel/serial converter 9 in the selected transmitter 3 and converted into a series signal as a function of the clock pulses, whereupon the series signal is outputted over the data signal transmission line 12. On the other hand the serial/parallel converter 10 of the receiver 4 has bit parallel

outputs 13a through 13h, so that the series signal transmitted over the data signal transmission line 12 can be converted into a bit parallel signal in the selected receiver 4 as a function of the clock pulses.

Fig. 5D is a schematic diagram of one embodiment of the serial/parallel converter 10. The serial/parallel converter 10 is of a circuit configuration adapted to operate contrary to the parallel/serial converter 9. To that end, the converter 10 shown comprises an AND gate 10a connected to receive the data signal transmitted over the data signal transmission line 12 and the station selection signal to provide the data signal if and when the station selection signal is received, and AND gate 10c connected to receive the station selection signal and the clock pulses to provide the clock pulse output if and when the station selection signal is received, and a switch 10b having a plurality of stationary contacts 100 through 107 connected through memory devices to a plurality of bit parallel outputs 13a through 13h, respectively, and a movable contact switchable in turn to the respective stationary contacts 100 through 107 as a function of the clock pulses obtainable from the AND gate 10c, thereby to convert the incoming series signal obtainable from the AND gate 10a into an output of the plurality of bits 13a through 13h.

In operation, when a station selection signal is obtained, the AND gate 10a is enabled and the series signal on the data signal transmission line 12 is allowed to pass through the AND gate 10a to reach the switch 10b. At the same time, the AND gate 10c is enabled, so that the switch 10b becomes operative in synchronism with the clock pulses obtainable from the AND gate 10c. As a result, the switch 10b is turned sequentially to the stationary contacts 100 through 107, storing the data signals transmitted as a function of the clock pulses in the memory devices for keeping the data until the next time the station selection signal is activated. Thereafter the bit parallel output signals 13a through 13h, respectively, are withdrawn.

Assuming that the transmitter 3a and the receiver 4a have been simultaneously selected as a function of the station selection signal, when the switch 9b of the parallel/serial converter 9 in the transmitter 3a is in the position of the stationary contact 90, the switch 10b of the serial/parallel converter 10 of the receiver 4a is in the position of the stationary contact 100, so that the input signal 11a at the stationary contact 90 of the transmitter 3a is transmitted to the output terminal 100 of the receiver 4a as the output signal 13a. Thus, the bit parallel input signals entering from the input terminals 90 through 97 of a given station selected as a function of the station selection signal are transmitted to the output terminals 100 through 107, respectively, of a receiver to be selected simultaneously as a function of the

station selection signal, whereby this transmitter and this receiver establish a mating relation for data communication for a time period of a single train of eight clock pulses. After these eight clock pulses are received, the station selection signal ceases in the above described transmitter and receiver between which a mating relation was established. As a result, the above described mating relation ends. Instead, another transmitter-receiver pair establishes a new mating relation for data communication as a result of the station selection signals generated therein. Thus, the mating pair of transmitter and receiver is changed in turn each time a train of eight clock pulses is terminated.

For the purpose of synchronization of the transmitters and receivers in the whole system, each clock pulse train is followed by an intermission time period of a given duration. More specifically, a train of clock pulses is discontinued for a given time period upon detection of the termination of a data signal transmission cycle by means of a counter in the rectangular wave generator 1a. Briefly described, when a train of clock pulses is discontinued for the said given time period of the intermission, the counters 7 in the transmitters and receivers in the whole system are simultaneously reset in response to discontinuance of the clock pulses. Thereafter, the succeeding clock pulse train is generated and transmitted, so that the counters 7 in the respective transmitters and receivers start to count the clock pulses simultaneously starting from the reset state of the counter. As a result, complete synchronization of the transmitters and receivers in the whole system can be maintained.

Fig. 6A is a detailed block diagram of one embodiment of the rectangular wave generator 1a for generating the above described succession of clock pulse trains including an intermission time period between consecutive trains. Fig. 6B shows the wave forms of the signals at various points in the Fig. 6A embodiment. The rectangular wave generator 1a shown in Fig. 6A comprises a rectangular wave oscillator 15a which generates pulses of the wave form (a) as a clock pulse. This clock pulse (a) is applied to a counter 15d where the number of the pulses is counted. The contents in the counter 15d are applied to a decoder 15e in a bit parallel fashion, so that the count value in the counter 15d is decoded into a plurality of individual decimal number outputs. The output of the decimal number 0 of the decoder 15e is connected through an inverter 15b to one input of an AND gate 15c. The output from the rectangular wave oscillator 15a is connected to another input of the AND gate 15c. The output from the AND gate 15c is withdrawn as an output of the rectangular wave generator 1a. A selectable output of the decoder 15e, associated with the decimal number i, is connected to a monostable multi-

vibrator 15f and the output from the monostable multivibrator 15f is applied to the counter 15d as a reset signal thereof.

In operation, unless the count value in the counter 15d is zero, the output of the decimal number zero of the decoder 15e is logic zero and the inverted signal at the point e inverted by the inverter 15b is logic one. Therefore, the AND gate 15c is enabled, so that the output pulses from the rectangular wave oscillator 15a are transmitted through the AND gate 15c to the output terminal p. If and when the count value of the counter 15d becomes value i indicating the termination of a train of clock pulses necessary for one data signal transmission cycle, the output of the decimal number i of the decoder 15e becomes logic one, thereby to trigger the monostable multivibrator 15f. As a result, the monostable multivibrator 15f is triggered and an output of logic one is obtained from the monostable multivibrator 15f for a predetermined time period. The counter 15d is responsive to the output from the monostable multivibrator 15f to be kept reset for the said predetermined time period. Therefore, the output of the decimal number zero of the decoder 15e becomes logic one and the output from the inverter 15b becomes logic zero. Accordingly, the AND gate 15c is disabled, so that the output of the AND gate 15c becomes logic zero, with the result that the clock pulse train is discontinued. After the lapse of the said predetermined time period, the output of the monostable multivibrator 15f returns to logic zero, so that the counter 15d is no longer supplied with the reset signal. The counter 15d starts to count pulses again from the rising edge of the following pulse and, when the count value in the counter 15d rises above zero, the AND gate 15c is again enabled, whereby the clock pulses are again transmitted through the AND gate 15c, with the result that the wave form at the point f is obtained with an intermission period commensurate with the said predetermined time period interposed between the preceding clock pulse train for one data signal transmission cycle and the succeeding clock pulse train for one data signal transmission cycle.

Now returning to Fig. 1, it is recalled that if and when the clock pulse trains are discontinued for a predetermined time period as described above the reset signal detectors 14 of the transmitters 3a, 3b, and the receivers 4a, 4b, become operative, so that the counters 7 of the respective transmitters 3a, 3b, and the receivers 4a, 4b, are reset. In the following, description will be made of a scheme for resetting the counters 7 in response to the discontinuance for the said predetermined time period of the clock pulse trains.

Fig. 7A is a block diagram of one embodiment of the reset signal detector 14 and Fig. 7B shows the wave forms of the signals at

various points in the Fig. 7A embodiment. Referring to Fig. 7A, the reset signal detector 14 comprises a series connection of a diode D1, a resistor R1, and an inverter 14a, with the junction between the resistor R1 and the inverter 14a grounded through a parallel connection of a capacitor C1 and a resistor R2. In operation, when successive clock pulses are received by the wave shaper 5, the diode D1 becomes conductive each time the clock pulse becomes logic one and the capacitor C1 is charged through the resistor R1, whereby a charged voltage across the capacitor C1 increases. When the clock pulse becomes logic zero, the diode D1 becomes non-conductive, so that the capacitor C1 is not charged and in fact the capacitor C1 discharges through the resistor R2, so that the charged voltage decreases. However, since the discharging resistor R2 has been selected to be sufficiently larger than the charging resistor R1, and the time constant R_2C_1 has been selected to be large as compared with the period of the clock pulses, the charged voltage decreases very slowly. When a logic one clock pulse is next received, the diode D1 becomes conductive to charge the capacitor C1. Accordingly, the input voltage of the inverter 14a is always higher than the threshold level of the inverter 14a, so that the output from the inverter 14a is always logic zero. The output from the inverter 14a is applied to the reset terminal of the counter 7, so that the counter is reset when the output from the inverter 14a is logic one. Therefore, while the clock pulses are successively transmitted, the output from the inverter 14a is logic zero, so that the clock pulses are counted by the counter 7. When the clock pulses are discontinued for a predetermined time period as shown in Fig. 7B, the capacitor C1 is discharged through the resistor R2 and the charged voltage decreases gradually. When the charged voltage of the capacitor C1 becomes lower than the threshold level E of the inverter 14a, the output from the inverter 14a shifts from logic zero to logic one. As a result, the counter 7 is reset and remains reset for the said predetermined time period. When the clock pulses are received again, the diode D1 becomes conductive, so that the capacitor C1 is again charged through the resistor R1. Since the time constant R_1C_1 has been selected to be much smaller, the capacitor C1 is abruptly charged and the output from the inverter 14a becomes logic zero again, and the counter 7 is no longer supplied with the reset signal. Thus, the counter 7 starts again to count the clock pulses. As described above, the counter 7 of the respective transmitters and receivers is reset in response to the intermission of the clock pulses for a predetermined time period and the counting operation by the counter 7 is regained simultaneously in all the transmitters and receivers starting from the reset state of the counter 7, with the result that

complete synchronism of all the transmitters and receivers in the whole system can be maintained.

One aspect of the present embodiment is that bidirectional multiplex transmission can be achieved with ease on the same transmission line. Some description will be made of the said facilitated bidirectional multiplex transmission on the same transmission line. As described previously, station selection in the respective transmitters and receivers is determined in accordance with the connection of the output of the decoder 8 to the converter 9 or 10. The selected transmitter has an operative parallel/serial converter 9, whereby a parallel input signal is converted into a series signal and the series signal is transmitted on the data signal transmission line 12. On the other hand, the selected receiver has an operative serial/parallel converter 10, whereby the series signal on the data signal transmission line 12 is converted into a parallel signal. The arrangement of these transmitters and receivers may be provided in any places where a multiplex transmission line comprising a data signal transmission line 12 and a clock pulse transmission line 2 is available.

Fig. 8A is a block diagram of bidirectional multiplex transmission system in accordance with the present invention and Fig. 8B shows the wave forms of the signals at various points in the Fig. 8A diagram. Referring to Fig. 8A, a transmitter/receiver casing in the place A comprises a transmitter 3a and a receiver 4a. On the other hand, a transmitter/receiver casing in the place B comprises a transmitter 3b and a receiver 4b. If and when the transmitter 3a is selected, simultaneously the receiver 4b is selected. If and when the transmitter 3b is selected, simultaneously the receiver 4a is selected. Accordingly, a first set of data transmitted from the transmitter 3a is received by the receiver 4b. On the other hand, a second set of data transmitted from the transmitter 3b is received by the receiver 4a. The same transmission line 12 is utilized between the transmitter/receiver casing in the place A and the transmitter/receiver casing in the place B for transmission and reception of the data signals. Referring to Fig. 8B, the outputs b2 and b3 from the first and second transmitters 3a and 3b, respectively, are shown with respect to the clock pulses b1, wherein bidirectional signal transmission has been performed. By determining station selection in the respective transmitters and receivers and the place to be installed of the transmitters and receivers, the direction of the transmission can be selected as desired, so that bidirectional multiplex transmission can be achieved with ease on the same transmission line.

Although the present invention has been described and illustrated in detail, it is to be clearly understood that the same is by way of illustration and example only and is not to be

taken by way of limitation, the scope of the present invention being limited only by the terms of the appended claims.

WHAT WE CLAIM IS:—

1. A time division multiplex transmission system comprising:

data signal transmission path means;

clock pulse transmission path means;

means for separately and concurrently transmitting along said clock pulse transmission path means first and second trains of clock pulses, the pulses of said first and second trains having opposite phases; and

at least one transmitter and at least one receiver between which data can be communicated along said data signal transmission path means, the or each transmitter and receiver being connected to said clock pulse transmission path means and being arranged to be synchronized in their operation by synchronizing pulses derived from the difference between the values of said first and second trains of clock pulses.

2. A time division multiplex transmission system in accordance with claim 1, including means for generating said first and second trains of clock pulses, said generating means comprising:

means for generating said first train of clock pulses, and

means coupled to said first train generating means for inverting the clock pulses of said first train for providing said second train of clock pulses.

3. A time division multiplex transmission system in accordance with claim 1 or 2, wherein said transmitter and said receiver each has differential amplifier means responsive to said first train of clock pulses and said second train of clock pulses for evaluating the difference between the values of said first and second trains of clock pulses thereby to provide said synchronizing pulses.

4. A time division multiplex transmission system in accordance with any preceding claim, arranged to transmit a series data signal having a plurality of series bits, wherein said transmitter includes

means for receiving a parallel data signal having a plurality of parallel bits, and

means responsive to said synchronizing pulses for converting said parallel data signal into said serial data signal.

5. A time division multiplex transmission system in accordance with any preceding claim, arranged to transmit a series data signal having a plurality of series bits, wherein said receiver includes

means responsive to said synchronizing pulses for converting said transmitted serial data signal into a parallel data signal having a plurality of parallel bits, and

means for holding said parallel data signal.

6. A time division multiplex transmission



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complete synchronism of all the transmitters and receivers in the whole system can be maintained.

One aspect of the present embodiment is that bidirectional multiplex transmission can be achieved with ease on the same transmission line. Some description will be made of the said facilitated bidirectional multiplex transmission on the same transmission line. As described previously, station selection in the respective transmitters and receivers is determined in accordance with the connection of the output of the decoder 8 to the converter 9 or 10. The selected transmitter has an operative parallel/serial converter 9, whereby a parallel input signal is converted into a series signal and the series signal is transmitted on the data signal transmission line 12. On the other hand, the selected receiver has an operative serial/parallel converter 10, whereby the series signal on the data signal transmission line 12 is converted into a parallel signal. The arrangement of these transmitters and receivers may be provided in any places where a multiplex transmission line comprising a data signal transmission line 12 and a clock pulse transmission line 2 is available.

Fig. 8A is a block diagram of bidirectional multiplex transmission system in accordance with the present invention and Fig. 8B shows the wave forms of the signals at various points in the Fig. 8A diagram. Referring to Fig. 8A, a transmitter/receiver casing in the place A comprises a transmitter 3a and a receiver 4a. On the other hand, a transmitter/receiver casing in the place B comprises a transmitter 3b and a receiver 4b. If and when the transmitter 3a is selected, simultaneously the receiver 4b is selected. If and when the transmitter 3b is selected, simultaneously the receiver 4a is selected. Accordingly, a first set of data transmitted from the transmitter 3a is received by the receiver 4b. On the other hand, a second set of data transmitted from the transmitter 3b is received by the receiver 4a. The same transmission line 12 is utilized between the transmitter/receiver casing in the place A and the transmitter/receiver casing in the place B for transmission and reception of the data signals. Referring to Fig. 8B, the outputs b2 and b3 from the first and second transmitters 3a and 3b, respectively, are shown with respect to the clock pulses b1, wherein bidirectional signal transmission has been performed. By determining station selection in the respective transmitters and receivers and the place to be installed of the transmitters and receivers, the direction of the transmission can be selected as desired, so that bidirectional multiplex transmission can be achieved with ease on the same transmission line.

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taken by way of limitation, the scope of the present invention being limited only by the terms of the appended claims.

WHAT WE CLAIM IS:—

1. A time division multiplex transmission system comprising:

data signal transmission path means;

clock pulse transmission path means;

means for separately and concurrently transmitting along said clock pulse transmission path means first and second trains of clock pulses, the pulses of said first and second trains having opposite phases; and

at least one transmitter and at least one receiver between which data can be communicated along said data signal transmission path means, the or each transmitter and receiver being connected to said clock pulse transmission path means and being arranged to be synchronized in their operation by synchronizing pulses derived from the difference between the values of said first and second trains of clock pulses.

2. A time division multiplex transmission system in accordance with claim 1, including means for generating said first and second trains of clock pulses, said generating means comprising:

means for generating said first train of clock pulses, and

means coupled to said first train generating means for inverting the clock pulses of said first train for providing said second train of clock pulses.

3. A time division multiplex transmission system in accordance with claim 1 or 2, wherein said transmitter and said receiver each has differential amplifier means responsive to said first train of clock pulses and said second train of clock pulses for evaluating the difference between the values of said first and second trains of clock pulses thereby to provide said synchronizing pulses.

4. A time division multiplex transmission system in accordance with any preceding claim, arranged to transmit a series data signal having a plurality of series bits, wherein said transmitter includes

means for receiving a parallel data signal having a plurality of parallel bits, and

means responsive to said synchronizing pulses for converting said parallel data signal into said serial data signal.

5. A time division multiplex transmission system in accordance with any preceding claim, arranged to transmit a series data signal having a plurality of series bits, wherein said receiver includes

means responsive to said synchronizing pulses for converting said transmitted serial data signal into a parallel data signal having a plurality of parallel bits, and

means for holding said parallel data signal.

6. A time division multiplex transmission

system in accordance with any preceding claim, wherein the duration of each of said first and second trains of clock pulses covers a plurality of station selection timing periods, in each of which periods is provided a plurality of clock pulses for communication of a data signal of a plurality of bits, and wherein

- 5 a plurality of said transmitters is provided, each said transmitter having means responsive to said synchronizing pulses for providing an enabling signal for identifying a predetermined one of said station selection time periods allotted to its own transmitter, each said transmitter being arranged to deliver said data signal to said data signal transmission path means in response to said enabling signal, and
- 10 a plurality of said receivers is provided, each said receiver having means responsive to said synchronizing pulses for providing an enabling signal for identifying a predetermined one of said station selection time periods allotted to its own receiver, each said receiver being arranged to receive said data signal in response to said enabling signal,
- 15 at least a predetermined one of said transmitters and a predetermined one of said receivers having the same station selection time period, whereby said predetermined transmitter and said predetermined receiver establish a mating relation during said same station selection time period for communication of the data signal therebetween.

- 20 7. A time division multiplex transmission system in accordance with claim 6, wherein each said enabling signal providing means comprises

means for counting the number of said station selection time periods, and

- 25 means responsive to the count reached by said counting means for identifying the predetermined station selection time period and providing said enabling signal in response to said identification.

- 30 8. A time division multiplex transmission system in accordance with claim 7, wherein said means for counting the number of station selection time periods comprises

first counter means for counting clock pulses and producing an output when the count reached equals the number of clock pulses in each said station selection time period, and

second counter means for counting the number of outputs from said first counter means.

- 35 9. A time division multiplex transmission system in accordance with any one of claims 6 to 8, including

means for defining the number of clock pulses in said first and second trains, and

means coupled to said clock pulse number defining means for selectively adjusting the defined number of clock pulses.

- 60 10. A time division multiplex transmission system in accordance with claim 9, wherein said clock pulse number defining means comprises

counter means for counting clock pulses,

means coupled to said counter means for detecting a predetermined count value reached by said counter means,

means responsive to the detection of said predetermined count value for resetting said counter means, and

means responsive to the reset state of said counter means for disabling the generation of said clock pulses.

- 65 11. A time division multiplex transmission system in accordance with any one of claims 6 to 10, arranged such that the generation of said clock pulses is terminated for a predetermined intermission time period at the end of each of said first and second trains of clock pulses.

- 70 12. A time division multiplex transmission system in accordance with claim 11, wherein each of said transmitters and receivers further comprises means responsive to the occurrence of said predetermined intermission time period for returning to an initial condition said enabling signal providing means.

- 75 13. A time division multiplex transmission system in accordance with claim 12 when appendant to claim 7, or any claim dependent thereon, wherein said returning means comprises means responsive to the occurrence of said predetermined intermission time period for resetting said means for counting the number of said station selection time periods.

- 80 14. A time division multiplex transmission system substantially as hereinbefore described with reference to Figures 1, 2A and B, 3, 4, 5A and 5C, optionally including Figures 5B and D, Figures 6A and B, Figures 7A and B and/or Figures 8A and B of the accompanying drawings.

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