

CLAIMS:

1. A method of facilitating exception handling, the method comprising steps of:
determining, by a processor, that an instruction executing within a computing environment has caused an exception, the instruction to operate on a vector register comprising a plurality of elements;
obtaining, based on the exception, a vector exception code, the vector exception code including a position within the vector register of an element of the plurality of elements of the vector register that caused the exception; and
outputting the vector exception code, including the position within the vector register of the element that caused the exception, in order to perform one or more actions based on the vector exception code.
2. The method of claim 1, wherein the position comprises an index within the vector register corresponding to the element that caused the exception.
3. The method of claim 1, wherein the position comprises a lowest indexed element in the vector register which caused the exception.
4. The method of claim 1, wherein the obtaining is based on the exception causing an interrupt.
5. The method of claim 1, wherein the vector exception code comprises a first portion to specify the position, and a second portion to specify a vector interrupt code.
6. The method of claim 5, wherein the position comprises a lowest indexed element in the vector register which caused the exception.
7. The method of claim 5, wherein the vector interrupt code comprises a value to indicate one of an invalid operation, division by zero, an overflow, an underflow or an inexact result.
8. The method of claim 1, wherein the method further comprises determining which one or more elements of the vector register caused the exception, and obtaining, based on the determining which one or more elements caused the exception, the position to be included in the vector exception code.

9. The method of claim 8, wherein the obtaining the position comprises determining the lowest indexed element of the one or more elements that caused the exception and using an index of the lowest indexed element as the position.
10. The method of claim 1, wherein the method further comprises placing the vector exception code in a data exception code field of a floating point control register.
11. The method of claim 1, wherein a size of the element is specified in a field of the instruction.
12. A system comprising means adapted for carrying out all the steps of the method according to any one of claims 1 to 11.
13. A computer program comprising instructions for carrying out all the steps of the method according to any one of claims 1 to 11, when said computer program is executed on a computer system.
14. A computer program product comprising a non-transitory computer readable storage medium readable by a processing circuit and storing instructions for execution by the processing circuit for execution by the processing circuit for performing the method according to any one of claims 1 to 11.