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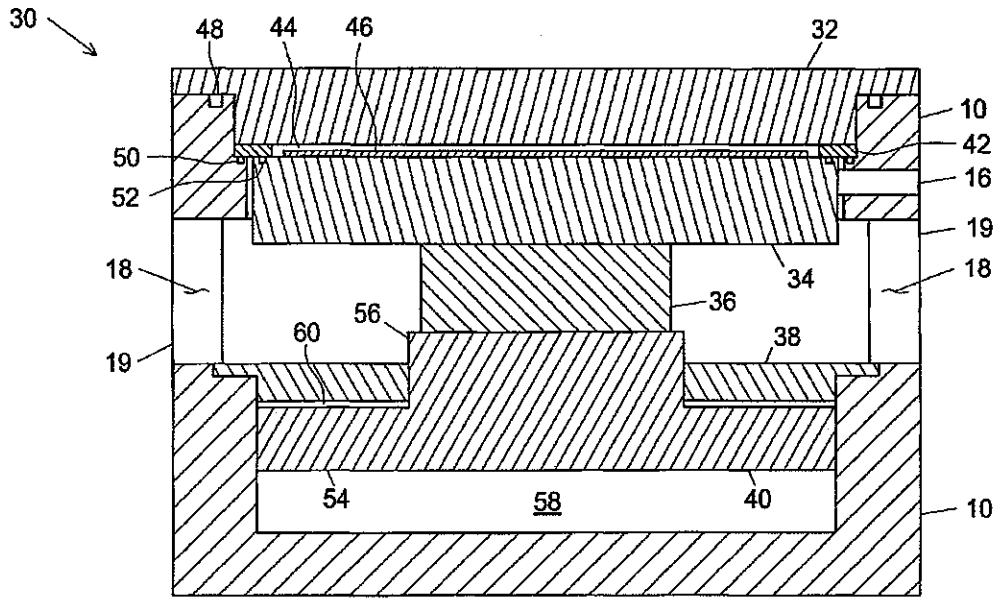
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(54) Title: HIGH PRESSURE PROCESSING CHAMBER FOR SEMICONDUCTOR SUBSTRATE



(57) Abstract: A high pressure chamber comprises a chamber housing, a platen, and a mechanical drive mechanism. The chamber housing comprises a first sealing surface. The platen comprises a region for holding the semiconductor substrate and a second sealing surface. The mechanical drive mechanism couples the platen to the chamber housing. In operation, the mechanical drive mechanism separates the platen from the chamber housing for loading of the semiconductor substrate. In further operation, the mechanical drive mechanism causes the second sealing surface of the platen and the first sealing surface of the chamber housing to form a high pressure processing chamber around the semiconductor substrate.

WO 02/09147 A2

HIGH PRESSURE PROCESSING CHAMBER FOR SEMICONDUCTOR SUBSTRATE

FIELD OF THE INVENTION

This invention relates to the field of high pressure processing. More particularly, this invention relates to the field of high pressure processing of a semiconductor substrate.

BACKGROUND OF THE INVENTION

Processing of semiconductor substrates presents unique problems not associated with processing of other workpieces. Typically, the semiconductor processing begins with a silicon wafer. The semiconductor processing starts with doping of the silicon wafer to generate transistor semiconductors. Next, the semiconductor processing continues with deposition of metal and dielectric layers interspersed with etching of lines and vias to produce transistor contacts and interconnect structures. Ultimately in the semiconductor processing, the transistor semiconductors, the transistor contacts, and the interconnects form integrated circuits.

A critical processing requirement for the processing of the semiconductor substrate is cleanliness. Much of semiconductor processing takes place in vacuum, which is an inherently clean environment. Other semiconductor processing takes place in a wet process at atmospheric pressure, which because of a rinsing nature of the wet process is an inherently clean process. For example, removal of photoresist and photoresist residue subsequent to etching of the lines and the vias uses plasma ashing, a vacuum process, followed by stripping in a stripper bath, a wet process.

Other critical processing requirements for the processing of the semiconductor substrates include throughput and reliability. Production processing of the semiconductor substrates takes place in a semiconductor fabrication facility. The semiconductor fabrication facility requires a large capital outlay for processing equipment, for the facility itself, and for a staff to run it. In order to recoup these expenses and generate a sufficient income from the facility, the processing equipment requires a throughput of a sufficient number of the wafers in a period of time. The processing equipment must also promote a reliable process in order to ensure continued revenue from the facility.

Until recently, the plasma ashing and the stripper bath was found sufficient for the removal of the photoresist and the photoresist residue in the semiconductor processing. However, recent advancements for the integrated circuits include etch feature critical dimensions below dimensions with sufficient structure to withstand the stripper bath and low

dielectric constant materials which cannot withstand an oxygen environment of the plasma ashing.

Recently, interest has developed in replacing the plasma ashing and the stripper bath for the removal of the photoresist and the photoresist residue with a supercritical process. However, high pressure processing chambers of existing supercritical processing systems are not appropriate to meet the unique needs of the semiconductor processing requirements.

What is needed is a high pressure processing chamber for semiconductor processing which meets cleanliness requirements of the semiconductor processing.

What is needed is a high pressure processing chamber for semiconductor processing which meets throughput requirements of the semiconductor processing.

What is needed is a high pressure processing chamber for semiconductor processing which meets reliability requirements of the semiconductor processing.

SUMMARY OF THE INVENTION

According to one aspect of the present invention, there is provided a high pressure chamber for processing of a semiconductor substrate comprises a chamber housing comprises a first sealing surface; a spacer contains a plurality of injection nozzles, the spacer seals to the first sealing surface; a platen comprises a region for holding the semiconductor substrate and a second sealing surface; and a single mechanical drive mechanism has a single pressure source, the single mechanical drive mechanism couples the platen to the chamber housing such that in operation the single mechanical drive mechanism separates the second sealing surface from the spacer for loading of the semiconductor substrate and further such that in operation the single mechanical drive mechanism causes the second sealing surface of the platen to seal to the spacer, such that the spacer, the first sealing surface, and the second sealing surface form and maintain a wafer cavity contains the region for holding the semiconductor substrate during high pressure processing.

According to another aspect of the present invention, there is provided a high pressure chamber for processing a semiconductor substrate comprises: a chamber housing comprises a first sealing surface; a spacer contains a plurality of injection nozzles, the spacer configured to seal to the first sealing surface; a platen comprises a second sealing surface and a region for holding the semiconductor substrate; a single mechanical drive mechanism has a single pressure source, the single mechanical drive mechanism couples the platen to the chamber housing such that in operation the single mechanical drive mechanism separates the second sealing surface from the spacer for loading the semiconductor substrate and further such that in operation the said single mechanical drive mechanism causes the second sealing surface of the platen to seal to the spacer, such that the spacer, the first sealing surface, and the second

sealing surface form a wafer cavity containing the region for holding the semiconductor substrate; and a mechanical clamp coupled to the chamber housing and the platen such that in operation the mechanical clamp maintains the wafer cavity during high pressure processing.

According to yet another aspect of the present invention, there is provided a high pressure chamber for processing of a semiconductor substrate comprises: chamber housing; platen comprises a region for holding the semiconductor substrate; a single mechanical drive mechanism has a single pressure source for forming and maintaining a wafer cavity contains the region for holding the semiconductor substrate during high pressure processing, the single mechanical drive mechanism couples the platen to the chamber housing such that in operation the single mechanical drive mechanism separates the platen form the chamber housing for loading of the semiconductor substrate; and means for sealing coupled to the chamber housing such that in operation the single pressure source causes the means for sealing, the platen, and the chamber housing to form the wafer cavity and maintain the wafer cavity during high pressure processing, wherein the means for sealing contains a plurality of injection nozzles configured to couple the wafer cavity to a supply source.

According to yet another aspect of the present invention, there is provided an apparatus for high pressure processing of a semiconductor substrate comprises: a pressure chamber frame; a single piston coupled to the pressure chamber frame and comprises a piston body and a piston neck, the pressure chamber frame and the piston body forms a first fluid cavity; a sealing plate coupled to the pressure chamber frame, the sealing plate in conjunction with the pressure chamber frame, the piston body, and the piston neck forms a second fluid cavity; a platen coupled to the piston neck, the platen comprises a region for holding the semiconductor substrate and a first sealing surface; a spacer has a plurality of injection nozzles configured to couple to a supply source; and a top lid coupled to the pressure chamber frame and comprises a second sealing surface, the second sealing surface seals to the spacer, the first sealing surface of the platen and the spacer configured such that in operation the piston body can be moved using a single pressure within the first fluid cavity so that the first sealing surface seals to the spacer to form a wafer cavity and to maintain the wafer cavity during high pressure processing, and in further operation the piston body can be moved so that the first sealing surface is separated from the spacer, thereby allows the semiconductor substrate to be loaded into and unloaded from the pressure chamber frame.

According to yet another aspect of the present invention, there is provided a high pressure chamber for processing a semiconductor substrate comprises: a chamber housing having a first sealing surface; a spacer contains a plurality of injection nozzles; a platen comprises a second sealing surface and a region for holding the semiconductor substrate; and a single mechanical drive mechanism couples to the platen and has a single pressure source, the single pressure source configured to move the platen to a first position and a second position such that in the first position the spacer seals to the first sealing surface and the second sealing surface thereby forms and maintains a wafer cavity contains the region

for holding the semiconductor substrate during high pressure processing and in the second position the spacer is separated from the second sealing surface.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a pressure chamber frame of the present invention.

FIG. 2 illustrates a first alternative pressure chamber of the present invention.

FIG. 3 illustrates a cross-section of the first alternative pressure chamber of the present invention.

FIGS. 4A and 4B illustrate a spacer/injection ring of the present invention.

FIG. 5 illustrates a wafer cavity and a two port outlet of the present invention.

FIG. 6 illustrates the preferred pressure chamber of the present invention.

FIGS. 7A through 7C illustrate an upper platen of the present invention.

FIGS. 8A through 8F illustrate the pressure chamber frame, the spacer/injection ring, and a wafer platen assembly of the present invention.

FIG. 9 illustrates a supercritical processing module and a second alternative pressure chamber of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The preferred pressure chamber of the present invention is preferably used for supercritical processing of a semiconductor wafer. Preferably, the preferred pressure chamber forms part of a supercritical processing module. Preferably, the supercritical processing module is used to remove photoresist from the semiconductor wafer. Alternatively, the supercritical processing module is used for other supercritical processing of the semiconductor wafer, such as photoresist development.

A pressure chamber frame of the present invention is illustrated in FIG. 1. The pressure chamber frame 10 includes a pressure chamber housing portion 12, an opening/closing housing portion 14, a wafer slit 16, windows 18, posts 19, a top opening 20, and top bolt holes 22. The wafer slit 16 is preferably sized for a 300 mm wafer. Alternatively, the wafer slit 16 is sized for a larger or a smaller wafer. Further alternatively, the wafer slit 16 is sized for a semiconductor substrate other than a wafer, such as a puck.

The opening/closing housing portion 14 of the pressure chamber frame 10 includes the windows 18, which provide access for assembly and disassembly of the preferred pressure chamber. Preferably, there are four of the windows 18, which are located on sides of the pressure chamber frame 10. Preferably, each of the windows 18 are framed on their sides by two of the posts 19, on their top by the pressure chamber housing portion 12, and on their bottom by a base 23. The bolt holes 22 of the pressure chamber housing portion 12 are for bolting a top lid to the pressure chamber frame 10.

Prior to describing the preferred pressure chamber of the present invention, a first alternative pressure chambers is described in order to more simply introduce aspects of the present invention.

The first alternative pressure chamber of the present invention is illustrated in FIG. 2. The first alternative pressure chamber 30 includes the pressure chamber frame 10, the top lid 32, a wafer platen 34, a cylinder 36, and a sealing plate 38. The top lid 32 is coupled to the pressure chamber frame 10, preferably by bolts (not shown). The wafer platen 34 is coupled to the cylinder 36. The cylinder 36 is coupled to a piston (not shown). The sealing plate 38 seals the piston from atmosphere.

It will be readily apparent to one skilled in the art that fasteners couple the wafer platen 34 to the cylinder 36, couple the cylinder 36 to the piston, and couple the sealing plate 38 to the pressure chamber frame 10. Further, it will be readily apparent to one skilled in the art that the bolts which preferably couple the top lid 32 to the pressure chamber frame 10 can be replaced by an other fastener, such as by screws or by threading the pressure chamber frame 10 and the top lid 32.

A cross-sectional view of the first alternative pressure chamber 30 in a closed configuration is illustrated in FIG. 3. The first alternative pressure chamber 30 includes the pressure chamber frame 10, the top lid 32, the wafer platen 34, the cylinder 36, the sealing plate 38, the piston 40, and a spacer/injection ring 42. Preferably, the pressure chamber frame 10, the top lid 32, the wafer platen 34, the cylinder 36, the sealing plate 38, the piston 40, and the spacer/injection ring 42 comprise stainless steel. The spacer/injection ring 42, the

top lid 32, and the wafer platen 34 form a wafer cavity 44. The wafer cavity 44 is preferably sealed with first, second, and third o-rings (not shown) located in first, second, and third o-ring grooves, 48, 50, and 52. The pressure chamber frame 10 and the sealing plate 38 enclose a piston body 54 leaving a piston neck 56 extending through the sealing plate 38. The piston neck 56 couples to the cylinder 36, which in turn couples to the wafer platen 34.

The pressure chamber frame 10 and the piston body 56 form a hydraulic cavity 58 below the piston body 56. The pressure chamber frame 10, the sealing plate 38, the piston body 54, and the piston neck 56 just above the piston body 54 form a pneumatic cavity 60 between the piston body 54 and the sealing plate 38.

It will be readily apparent to one skilled in the art that a piston seal between the piston body 54 and the pressure chamber frame 10 isolates the hydraulic cavity 58 from the pneumatic cavity 60. Further, it will be readily apparent to one skilled in the art that a neck seal, between the piston neck 56 and the sealing plate 38, and a plate seal, between the sealing plate 38 and the pressure chamber frame 10, isolate the pneumatic cavity 60 from atmosphere. Moreover, it will be readily apparent to one skilled in the art that in operation hydraulic and pneumatic fluid systems, both of which are well known in the art, are coupled to the hydraulic cavity 58 and the pneumatic cavity 60, respectively.

In the supercritical processing, the semiconductor wafer 46 occupies the wafer cavity 44 where a supercritical fluid is preferably used in conjunction with a solvent to remove the photoresist from the semiconductor wafer 46. After the supercritical processing and venting of the wafer cavity 44 to atmospheric pressure, hydraulic fluid within the hydraulic cavity 58 is depressurized while the pneumatic cavity 60 is slightly pressurized with a gas, which moves the piston 40 down. This lowers the wafer platen 34 so that the semiconductor wafer 46 is adjacent to the slit 16. The wafer 46 is then removed through the slit 16. Preferably, the semiconductor wafer is removed by a robot (not shown). Alternatively, the semiconductor wafer 46 is removed by a technician.

A second semiconductor wafer is then loaded through the slit 16 and onto the wafer platen 34. Next, the pneumatic cavity 60 is vented to atmospheric pressure while the hydraulic cavity 58 is pressurized with the hydraulic fluid, which drives the wafer platen 34 into the spacer/injection ring 42, which reforms the wafer cavity 44. The wafer cavity 44 is then pressurized, and the supercritical fluid and the solvent remove the photoresist from the second wafer.

It will be readily apparent to one skilled in the art that during the supercritical processing the hydraulic fluid within the hydraulic cavity 58 must be maintained at an hydraulic pressure which causes an upward force that is greater than a downward force on the wafer platen 34 caused by the supercritical fluid.

The spacer/injection ring 42 of the present invention is further illustrated FIG. 4A. The spacer/injection ring comprises a ring body 62 having an annulus 64 and injection nozzles 66. Preferably, the spacer/injection ring 42 has an inside diameter of slightly greater than 12 inches, which is sized for the 300 mm wafer. Alternatively, the spacer/injection ring

42 has a larger or smaller inside diameter. Preferably, the spacer/injection ring has forty-five of the injection nozzles 66. Alternatively, the spacer/injection ring has more or less of the injection nozzles 66. Preferably, each of the injection nozzles 66 is oriented at 45° to a radius of the inside diameter of the spacer/injection ring 42. Alternatively, the injection nozzles are at a larger or smaller angle. Preferably, the spacer/injection ring 42 has a thickness of .200 inches. Alternatively, the spacer/injection ring 42 has a larger or smaller thickness.

A cross-section of the spacer/injection ring 42 is illustrated in FIG. 4B, showing the ring body 62, the annulus 64, and one of the injection nozzles 66. Preferably, the annulus 64 has a rectangular cross-section having a width of .160 inches and a height of .110 inches. Preferably, each of the injection nozzles 66 a diameter of .028 inches. The annulus 64 and the injection nozzles 66 of the spacer/injection ring 42 form a passage for the supercritical fluid entering the wafer cavity 44 (FIG. 3). In the supercritical processing, the supercritical fluid first enters the annulus 64, which acts as a reservoir for the supercritical fluid. The supercritical fluid is then injected into the wafer cavity 44 by the injection nozzles 66, which creates a vortex within the wafer cavity 44 (FIG. 3).

The wafer cavity 44 and a two port outlet of the present invention are illustrated in FIG. 5. The wafer cavity 44 formed by an alternative top lid 32A, the wafer platen 34, and the spacer/injection ring 42 is preferably exhausted through the two port outlet 70. The two port outlet 70 includes a shuttle piece 72, which is alternated between a first position 74 and a second position 76. By alternating the shuttle piece 72 between the first and second positions, a center of the vortex formed by the spacer/injection ring 42 will alternate between a first exhaust port 78 and a second exhaust port 80. Preferably, the first and second exhaust ports, 78 and 80, have a diameter of .50 inch and have centers separated by a distance of 1.55 inches. Alternatively, the diameter and the distance are larger or smaller depending upon the specific implementation of the present invention.

In operation, incoming supercritical fluid 82 enters the annulus 64 of the spacer/injection ring 42, creates the vortex within the wafer cavity 44, and alternately creates first and second vortex centers proximate to the first and second exhaust ports, 78 and 80, as the shuttle piece moves from the first position 74 to the second position 76. Outgoing supercritical fluid 84 then exits the two port outlet 70. In this way, the supercritical processing of an entire surface of the semiconductor wafer 46 is assured.

It will be readily apparent to one skilled in the art that the injection nozzles 66 of the spacer/injection ring 42 and the two port outlet 70 can be incorporated into a general pressure chamber having ingress and egress for a semiconductor substrate through a gate valve. Further, it will be readily apparent to one skilled in the art that depending upon a particular supercritical process for the semiconductor substrate, the spacer/injection ring 42 could be unneeded since the particular supercritical process does not require the vortex for adequate processing. Moreover, it will be readily apparent to one skilled in the art that the shuttle piece 72 of the two port outlet 70 can be replaced by a more general valve arrangement.

The preferred pressure chamber of the present invention is illustrated in FIG. 6. The preferred pressure chamber 30A includes the pressure chamber frame 10, the alternative top lid 32A, a wafer platen assembly 34A, the sealing plate 38, an alternative piston 40A, and a pneumatic cylinder 86. The wafer platen assembly 34A includes a lower platen 88, an upper platen 90, and a pedestal 92. The alternative piston 40A includes an alternative piston body 54A and an alternative piston neck 56A.

The alternative piston neck 56A includes a hollow center portion where the pneumatic cylinder 86 couples to the alternative piston 40A. The piston neck 56A couples to the lower platen 88 at a top of the piston neck 56A. The lower platen 88 couples to the upper platen 90 at an upper surface of the lower platen 88. The lower platen 88 and the upper platen 90 couple to the pedestal 92 at centers of the lower and upper platens, 88 and 90. The pedestal 92 couples to the pneumatic cylinder 86 at a lower end of the pedestal 92. The pedestal 92 includes a vacuum port 94, which provides vacuum for a pedestal vacuum chuck 96.

It will be readily apparent to one skilled in the art that the preferred pressure chamber 30A includes a vacuum line to the vacuum port 94 and a pneumatic line to the pneumatic cylinder 86.

A top view of the upper platen 90 is illustrated in FIG. 7A. The upper platen 90 includes fourth and fifth o-ring grooves, 100 and 102, and first and second vacuum grooves, 104 and 106. In operation, fourth and fifth o-rings occupy the fourth and fifth o-ring grooves, 104 and 106.

A cross-section of a portion of the upper platen 90 is illustrated in FIG. 7B. The cross section includes the fourth and fifth o-ring grooves, 100 and 102, the first and second vacuum grooves, 104 and 106, and a second vacuum port 108. In operation, the second vacuum port 108 is coupled to a vacuum pump so that vacuum is applied to the first and second vacuum grooves, 104 and 106. Thus, the fourth o-ring groove 100 and the first vacuum groove 104 form a vacuum chuck in conjunction with the lower platen 88 and the pedestal 92 (FIG. 6). The fifth o-ring groove 102 and the second vacuum groove add a redundancy to the vacuum chuck so that a leak that passes the fourth o-ring groove 100 does not prevent the vacuum chuck from functioning. The redundancy also provides backside protection for the semiconductor wafer 46 (FIG. 6).

A bottom surface of the upper platen 90 is further illustrated in FIG. 7C. Preferably, the bottom surface 90 includes a resistive heating element groove 110. Preferably in operation, a resistive heating element occupies the resistive heating element groove 110 to assist in heating the wafer cavity 44 and the semiconductor wafer 46 (FIG. 6).

The upper platen 90 is preferably sized to accommodate a 300 mm wafer. An alternative upper platen can be used in lieu of the upper platen 90, where the alternative upper platen has the fourth and fifth o-ring grooves, 100 and 102, and the first and second vacuum grooves sized to accommodate a different size wafer than the 300 mm wafer, for example a 200 mm wafer. Thus, rather than replacing the wafer platen assembly 34A in the

preferred pressure chamber 30A (FIG. 6), only the upper platen 90 needs to be replaced to accommodate the different size wafer.

The pressure chamber frame 10, the alternative top lid 32A, the spacer/injection ring 42, and the wafer platen assembly 34A of the preferred pressure chamber 30A are further illustrated in FIGS. 8A-8F. The wafer platen assembly 34A includes the lower platen 88, the upper platen 90, and the pedestal 92. The lower platen includes sixth and seventh o-ring grooves, 112 and 114, for sixth and seventh o-rings (not shown), which seal the lower platen 88 to the upper platen 90 and the pedestal 92, respectively. The lower platen 88 also includes a third vacuum port (not shown) which couples the vacuum pump to the second vacuum port 108 (FIG. 7B).

In FIG. 8A, the wafer platen assembly 34A is in a closed position and the wafer cavity 44 is empty. In FIG. 8B, the alternative piston 40A (FIG. 6) has lowered the wafer platen assembly 34A to a load position. In FIG. 8C, a robot end effector 116 has moved the semiconductor wafer 46 into the preferred pressure chamber 30A. In FIG. 8D, the pedestal 92 was driven by the air cylinder 86 (FIG. 6) to raise the semiconductor wafer 46 off the robot end effector 116 and the robot end effector 116 has retracted from the preferred pressure chamber 30A. As the pedestal 92 raised the semiconductor wafer 46 off the robot end effector a vacuum applied through the first vacuum port 94 secured the semiconductor wafer 46 to the pedestal vacuum chuck 96.

In FIG. 8E, the pedestal 92 was lowered by the air cylinder 86 so that a lower surface of the pedestal 92 seals to the lower platen 88 at the seventh o-ring groove 114. As the pedestal 92 reached the lower platen 88, the vacuum applied to the first and second vacuum grooves, 104 and 106, secured the semiconductor wafer 46 to the upper platen 90. In FIG. 8F, the alternative piston 40A has raised the wafer platen assembly 34A so that the wafer cavity 44 is sealed between the upper platen 90 and the spacer/injection ring 42.

The supercritical processing module of the present invention, incorporating a second alternative pressure chamber of the present invention, is illustrated in FIG. 9. The supercritical processing module 200 includes the second alternative pressure chamber 30B, a pressure chamber heater 204, a carbon dioxide supply arrangement 206, a circulation loop 208, a circulation pump 210, a chemical agent and rinse agent supply arrangement 212, a separating vessel 214, a liquid/solid waste collection vessel 217, and a liquefying/purifying arrangement 219.

The second alternative pressure chamber 30B includes an alternative pressure chamber housing 12A and an alternative wafer platen 34B. The alternative pressure chamber housing 12A and the alternative wafer platen 34B form an alternative wafer cavity 44A for the semiconductor substrate 46. The alternative pressure chamber housing 12A includes alternative injection nozzles 66A. Preferably, the alternative wafer platen 34A is held against the alternative pressure chamber housing 12A using a hydraulic force. Alternatively, the alternative wafer platen 34B is held against the alternative pressure chamber housing 12A using a mechanical clamping force. Preferably, the alternative wafer platen 34B moves to a

load/unload position 215 by releasing the hydraulic force. Alternatively, the alternative wafer platen 34B moves to the load/unload position 215 upon release of the mechanical clamping force. Further alternatively, the alternative wafer platen 34B moves to the load/unload position 215 by actuating a drive screw coupled to the alternative wafer platen 34B or by using a pneumatic force.

The carbon dioxide supply arrangement 206 includes a carbon dioxide supply vessel 216, a carbon dioxide pump 218, and a carbon dioxide heater 220. The chemical agent and rinse agent supply arrangement 212 includes a chemical supply vessel 222, a rinse agent supply vessel 224, and first and second high pressure injection pumps, 226 and 228.

The carbon dioxide supply vessel 216 is coupled to the second alternative pressure chamber 30B via the carbon dioxide pump 218 and carbon dioxide piping 230. The carbon dioxide piping 230 includes the carbon dioxide heater 220 located between the carbon dioxide pump 218 and the second alternative pressure chamber 30B. The pressure chamber heater 204 is coupled to the second alternative pressure chamber 30B. The circulation pump 210 is located on the circulation loop 208. The circulation loop 208 couples to the second alternative pressure chamber 30B at a circulation inlet 232 and at a circulation outlet 234. The chemical supply vessel 222 is coupled to the circulation loop 208 via a chemical supply line 236. The rinse agent supply vessel 224 is coupled to the circulation loop 208 via a rinse agent supply line 238. The separating vessel 214 is coupled to the second alternative pressure chamber 30B via exhaust gas piping 240. The liquid/solid waste collection vessel 217 is coupled to the separating vessel 214.

The separating vessel 214 is preferably coupled to the liquefying/purifying arrangement 219 via return gas piping 241. The liquefying/purifying arrangement 219 is preferably coupled to the carbon dioxide supply vessel 216 via liquid carbon dioxide piping 243. Alternatively, an off-site location houses the liquefying/purifying arrangement 219, which receives exhaust gas in gas collection vessels and returns liquid carbon dioxide in liquid carbon dioxide vessels.

The pressure chamber heater 204 heats the second alternative pressure chamber 30B. Preferably, the pressure chamber heater 204 is a heating blanket. Alternatively, the pressure chamber heater is some other type of heater.

Preferably, first and second filters, 221 and 223, are coupled to the circulation loop 208. Preferably, the first filter 221 comprises a fine filter. More preferably, the first filter 221 comprises the fine filter configured to filter 0.05 μm and larger particles. Preferably, the second filter 223 comprises a coarse filter. More preferably, the second filter 223 comprises the coarse filter configured to filter 2-3 μm and larger particles. Preferably, a third filter 225 couples the carbon dioxide supply vessel 216 to the carbon dioxide pump 218. Preferably, the third filter 225 comprises the fine filter. More preferably, the third filter 225 comprises the fine filter configured to filter the 0.05 μm and larger particles.

It will be readily apparent to one skilled in the art that the supercritical processing module 200 includes valving, control electronics, and utility hookups which are typical of

supercritical fluid processing systems. Further, it will be readily apparent to one skilled in the art that the alternative injection nozzles 66A could be configured as part of the alternative wafer platen 34B rather than as part of the alternative chamber housing 12A.

In operation, the supercritical processing module is preferably used for removing the photoresist and photoresist residue from the semiconductor wafer 46. A photoresist removal process employing the supercritical processing module 200 comprises a loading step, a cleaning procedure, a rinsing procedure, and an unloading step.

In the loading step, the semiconductor wafer 46 is placed on the alternative wafer platen 34B and then the alternative wafer platen 34B is moved against the alternative chamber housing 12A sealing the alternative wafer platen 34B to the alternative chamber housing 12A and, thus, forming the alternative wafer cavity 44A.

The cleaning procedure comprises first through fourth process steps. In the first process step, the alternative wafer cavity 44A is pressurized by the carbon dioxide pump 218 to desired supercritical conditions. In the second process step, the first injection pump 226 pumps solvent form the chemical supply vessel 222 into the alternative wafer cavity 44A via the chemical supply line and the circulation loop 208. Upon reaching desired supercritical conditions, the carbon dioxide pump stops pressurizing the alternative wafer cavity 44A. Upon reaching a desired concentration of the solvent, the first injection pump 226 stops injecting the solvent. In the third process step, the circulation pump 210 circulates supercritical carbon dioxide and the solvent through the alternative wafer cavity 44A and the circulation loop 208 until the photoresist and the photoresist residue is removed from the semiconductor wafer. In the fourth process step, the wafer cavity 44A is partially exhausted while maintaining pressure above a critical pressure, then the alternative wafer cavity 44A is re-pressurized by the carbon dioxide pump 218 and partially exhausted again while maintaining the pressure above the critical pressure.

The rinsing procedure comprises fourth through seventh process steps. In the fourth process step, the alternative wafer cavity is pressurized by the carbon dioxide pump 218. In the fifth process step, the second injection pump 228 pumps a rinse agent form the rinse agent supply vessel 224 into the alternative wafer cavity 44A via the rinse agent supply line 238 and the circulation loop 208. Upon reaching a desired concentration of the rinse agent, the second injection pump 228 stops injecting the rinse agent. In the sixth process step, the circulation pump 210 circulates the supercritical carbon dioxide and the rinse agent through the alternative wafer cavity 44A and the circulation loop 208 for a pre-determined time. In the seventh process step, the alternative wafer cavity 44A is de-pressurized. Alternatively, it may be found that the fifth and sixth process steps are not needed.

In the unloading step, the alternative wafer platen 34B is moved to the load/unload position 215 where the semiconductor is removed from the alternative wafer platen 34B.

Preferably, at least two of the supercritical processing modules of the present invention form part of a multiple workpiece processing system, which provides simultaneous processing capability for at least two of the semiconductor wafers. The multiple workpiece

processing system is taught in U.S. Patent Application No. 09/704,642, filed on Nov. 1, 2000, which is incorporated in its entirety by reference. Alternatively, the supercritical processing module of the present invention along with a non-supercritical processing module forms part of a multiple process semiconductor processing system. The multiple process semiconductor processing system is taught in U.S. Patent Application No. 09/704,641, filed Nov. 1, 2000, which is incorporated in its entirety by reference. Further alternatively, the supercritical processing module of the present invention forms part of a stand-alone supercritical processing system employing a single supercritical processing module of the present invention.

A third alternative pressure chamber of the present invention comprises the second alternative pressure chamber 34B plus a surface enhancement feature of the alternative chamber housing 12A above the semiconductor substrate 46. The surface enhancement feature comprises a height variation from an outer diameter of the alternative wafer cavity 44A to a center of the alternative wafer cavity 44A in order to provide more uniform molecular speeds above the semiconductor substrate 46. Preferably, the height variation comprises a high point at the outer diameter of the alternative wafer cavity 34B to a low point at the center of the alternative wafer cavity 34B providing a more constricted space at the center of the wafer cavity 34B. Alternatively, the height variation comprises the high point at the outer diameter of the alternative wafer cavity 34B, the low point between the outer diameter and the center of the alternative wafer cavity 34B, and an intermediate point at the center of the alternative wafer cavity 34B.

It will be readily apparent to one skilled in the art that the preferred pressure chamber 30A and the first through third alternative pressure chambers of the present invention are appropriate for high pressure processing that is below supercritical conditions.

It will be readily apparent to one skilled in the art that other various modifications may be made to the preferred embodiment without departing from the spirit and scope of the invention as defined by the appended claims.

CLAIMS

1. A high pressure chamber for processing of a semiconductor substrate comprising:

   a. a chamber housing comprising a first sealing surface;

   b. a spacer containing a plurality of injection nozzles, the spacer sealing to the first sealing surface;

   c. a platen comprising a region for holding the semiconductor substrate and a second sealing surface; and

   d. a single mechanical drive mechanism having a single pressure source, the single mechanical drive mechanism coupling the platen to the chamber housing such that in operation the single mechanical drive mechanism separates the second sealing surface from the spacer for loading of the semiconductor substrate and further such that in operation the said single mechanical drive mechanism causes the second sealing surface of the platen to seal to the spacer, such that the spacer, the first sealing surface, and the second sealing surface form and maintain a wafer cavity containing the region for holding the semiconductor substrate during high pressure processing.

2. The high pressure chamber of claim 1 wherein the first sealing surface of the chamber housing comprises an o-ring groove.

3. The high pressure chamber of claim 2 further comprising an o-ring within the o-ring groove.

4. The high pressure chamber of claim 1 wherein the second sealing surface of the platen comprises an o-ring groove.

5. The high pressure chamber of claim 4 further comprising an o-ring within the o-ring groove.

6. The high pressure chamber of claim 1 wherein the single mechanical drive mechanism comprises a piston driven by a fluid.

7. The high pressure chamber of claim 6 wherein the fluid comprises an incompressible fluid.

8. The high pressure chamber of claim 6 wherein the fluid comprises a compressible fluid.

9. The high pressure chamber of claim 1 wherein the single mechanical drive mechanism comprises an electro-mechanical drive mechanism.

10. The high pressure chamber of claim 9 wherein the electro-mechanical drive mechanism comprises a linear actuator.

11. The high pressure chamber of claim 10 wherein the linear actuator comprises a drive screw.

12. A high pressure chamber for processing a semiconductor substrate comprising

a. a chamber housing comprising a first sealing surface;

b. a spacer containing a plurality of injection nozzles, the spacer configured to seal to the first sealing surface;

c. a platen comprising a second sealing surface and a region for holding the semiconductor substrate;

d. a single mechanical drive mechanism having a single pressure source, the single mechanical drive mechanism coupling the platen to the chamber housing such that in operation the single mechanical drive mechanism separates the second sealing surface from the spacer for loading the semiconductor substrate and further such that in operation the said single mechanical drive mechanism causes the second sealing surface of the platen to seal to the spacer, such that the spacer, the first sealing surface, and the second sealing surface form a wafer cavity containing the region for holding the semiconductor substrate; and

e. a mechanical clamp coupled to the chamber housing and the platen such that in operation the mechanical clamp maintains the wafer cavity during high pressure processing.

13. A high pressure chamber for processing of a semiconductor substrate comprising:

a. chamber housing;

b. platen comprising a region for holding the semiconductor substrate;

c. a single mechanical drive mechanism having a single pressure source for forming and maintaining a wafer cavity containing the region for holding the semiconductor substrate during high pressure processing, the single mechanical drive mechanism coupling the platen to the chamber housing such

that in operation the single mechanical drive mechanism separates the platen from the chamber housing for loading of the semiconductor substrate; and

d. means for sealing coupled to the chamber housing such that in operation the said single pressure source causes the means for sealing, the platen, and the chamber housing to form the wafer cavity and maintain the wafer cavity during high pressure processing,
wherein the means for sealing contains a plurality of injection nozzles configured to couple the wafer cavity to a supply source.

14. An apparatus for high pressure processing of a semiconductor substrate comprising:

a. a pressure chamber frame;

b. a single piston coupled to the pressure chamber frame and comprising a piston body and a piston neck, the pressure chamber frame and the piston body forming a first fluid cavity;

c. a sealing plate coupled to the pressure chamber frame, the sealing plate in conjunction with the pressure chamber frame, the piston body, and the piston neck forming a second fluid cavity;

d. a platen coupled to the piston neck, the platen comprising a region for holding the semiconductor substrate and a first sealing surface; e. a spacer having a plurality of injection nozzles configured to couple to a supply source; and

f. a top lid coupled to the pressure chamber frame and comprising a second sealing surface, the second sealing surface sealing to the spacer, the first sealing surface of the platen and the spacer configured such that in operation the said piston body can be moved using a single pressure within the first fluid cavity so that the first sealing surface seals to the spacer to form a wafer cavity and to maintain the wafer cavity during high pressure processing, and in further operation the piston body can be moved so that the first sealing surface is separated from the spacer, thereby allowing the semiconductor substrate to be loaded into and unloaded from the pressure chamber frame.

15. The apparatus of claim 14 wherein the first sealing surface and the second sealing surface are configured to form the wafer cavity and to maintain the wafer cavity with a supercritical environment therein.

16. The apparatus of claim 14 wherein the first sealing surface and the second sealing surface are configured to form the wafer cavity and to maintain the wafer cavity with a non-supercritical environment therein.

17. The high pressure chamber of claim 1, wherein the spacer further contains a plenum coupled to the plurality of injection nozzles, the plenum having a width larger than a width of the plurality of injection nozzles.

18. The high pressure chamber of claim 17, wherein a ratio of the width of the plenum to the width of the plurality of injection nozzles is at least 3:1.

19. The high pressure chamber of claim 17, further comprising a supercritical condition generator coupled to the plenum, the supercritical condition generator comprising a heater coupled to a supply source, the supply source comprising a supply vessel.

20. The high pressure chamber of claim 1, further comprising a circulation loop coupled to the wafer cavity and configured to maintain a supercritical fluid in a supercritical state and to circulate the supercritical fluid through the wafer cavity.

21. The high pressure processing chamber of claim 20, further comprising a pump and a filter coupled to the circulation loop.

22. A high pressure chamber for processing a semiconductor substrate comprising:

a. a chamber housing having a first sealing surface;

b. a spacer containing a plurality of injection nozzles;

c. a platen comprising a second sealing surface and a region for holding the semiconductor substrate; and

d. a single mechanical drive mechanism coupled to the platen and having a single pressure source, the single pressure source configured to move the platen to a first position and a second position such that in the first position the spacer seals to the first sealing surface and the second sealing surface thereby forming and maintaining a wafer cavity containing the region for holding the semiconductor substrate during high pressure processing and in the second position the spacer is separated from the second sealing surface.

23. The high pressure chamber of claim 22, further comprising a supply source coupled to the plurality of injection nozzles, the plurality of injection nozzles configured to introduce a material contained in the supply source into the wafer cavity.

24. The high pressure chamber of claim 23, further comprising one or more heaters coupled to the wafer cavity, the one or more heaters configured to generate and maintain supercritical conditions within the wafer cavity.