Claims

What is claimed is:

1. A semiconductor device for a RF-front end module, the semiconductor device comprising:

a first wafer comprising a deep trench capacitor;

a second wafer bonded to the first wafer, wherein the second wafer comprises:

a first active device on a first silicon-on-insulator (SOI) substrate; and

a first metal interconnection connected to the first active device and the deep trench capacitor,

a dielectric layer formed on the first active device opposite the first metal interconnection, the dielectric layer comprising a second metal interconnection that connects the first metal interconnection; and

a third wafer bonded to the dielectric layer, wherein the third wafer comprises:

a second active device on a second silicon-on-insulator (SOI) substrate; and

a third metal interconnection connected to the second active device, wherein the third metal interconnection contacts the second metal interconnection.

2. The semiconductor device of claim 1, wherein the first wafer comprises:

the deep trench capacitor in a substrate;

a first inter-layer dielectric (ILD) layer on the deep trench capacitor;

a first inter-metal dielectric (IMD) layer on the first ILD layer; and

a metal interconnection in the first ILD layer and the first IMD layer.

3. The semiconductor device of claim 2, wherein the second wafer comprises:

a second ILD layer on the first active device;

a second IMD layer on the second ILD layer; and

the first metal interconnection in the second ILD layer and the second IMD layer.

4. The semiconductor device of claim 3, wherein the first IMD layer contacts the second IMD layer.

5. The semiconductor device of claim 3, wherein the first metal interconnection contacts the metal interconnection in the first wafer.

6. The semiconductor device of claim 3, wherein

the second metal interconnection in the dielectric layer, the first SOI substrate, and the second ILD layer.

7. The semiconductor device of claim 6, wherein the third wafer comprises:

a third ILD layer on the second active device;

a third IMD layer on the third ILD layer; and

the third metal interconnection in the third IMD layer.

8. The semiconductor device of claim 7, wherein the third IMD layer contacts the dielectric layer.

9. A semiconductor device for a RF-front end module, the semiconductor device comprising:

a packaging substrate,

a first wafer on the packaging substrate, wherein the first wafer comprises a deep trench capacitor;

a second wafer on the packaging substrate and adjacent to the first wafer, wherein the second wafer comprises:

a first active device on a first silicon-on-insulator (SOI) substrate; and

a first metal interconnection connected to the first active device;

a dielectric layer formed on the first active device opposite the first metal interconnection, the dielectric layer comprising a second metal interconnection that connects the first metal interconnection; and

a third wafer on the dielectric layer, wherein the third wafer comprises:

a second active device on a second silicon-on-insulator (SOI) substrate; and

a third metal interconnection connected to the second active device, wherein the third metal interconnection contacts the first metal interconnection,

wherein the second metal interconnection is connected to the deep trench capacitor via the packaging substrate.

10. The semiconductor device of claim 9, wherein the first wafer comprise:

the deep trench capacitor in a substrate;

a inter-layer dielectric (ILD) layer on the deep trench capacitor; and

a metal interconnection in the ILD layer;

a first redistribution layer (RDL) between the ILD and the packaging substrate; and

a first bump connecting the first RDL and the packaging substrate.

11. The semiconductor device of claim 12, wherein the second wafer comprises:

a first interlayer dielectric (ILD) layer on the first active device;

a first inter-metal dielectric (IMD) layer on the first ILD layer;

a second redistribution layer (RDL) between the first SOI substrate and the packaging substrate;

the first metal interconnection in the first ILD layer, the first IMD layer, and the first SOI substrate and connecting the first active device and the second RDL; and

a second bump connecting the second RDL and the packaging substrate.

12. The semiconductor device of claim 11, wherein the third wafer comprises:

a second ILD layer on the second active device;

a second IMD layer on the second ILD layer; and

the third metal interconnection in the second IMD layer.