

FIG. 1

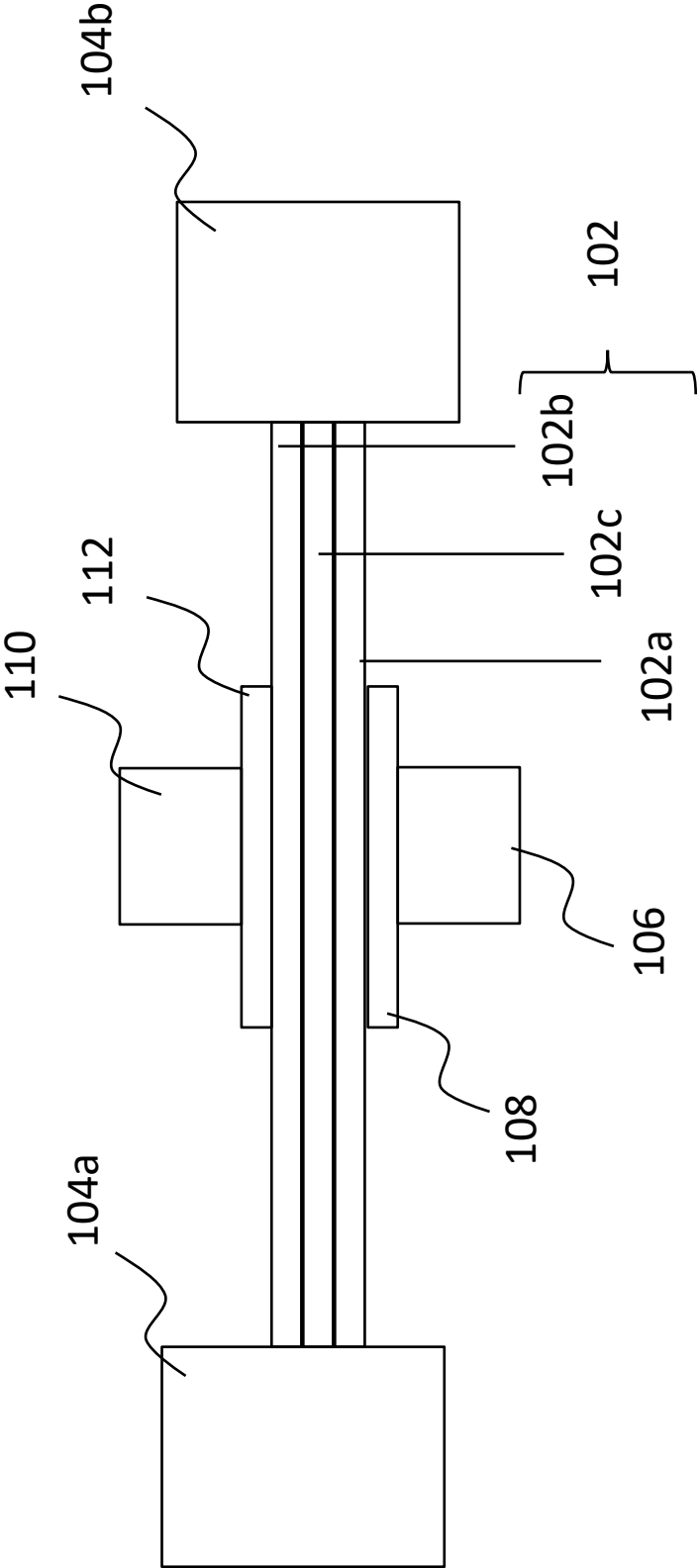


FIG. 2

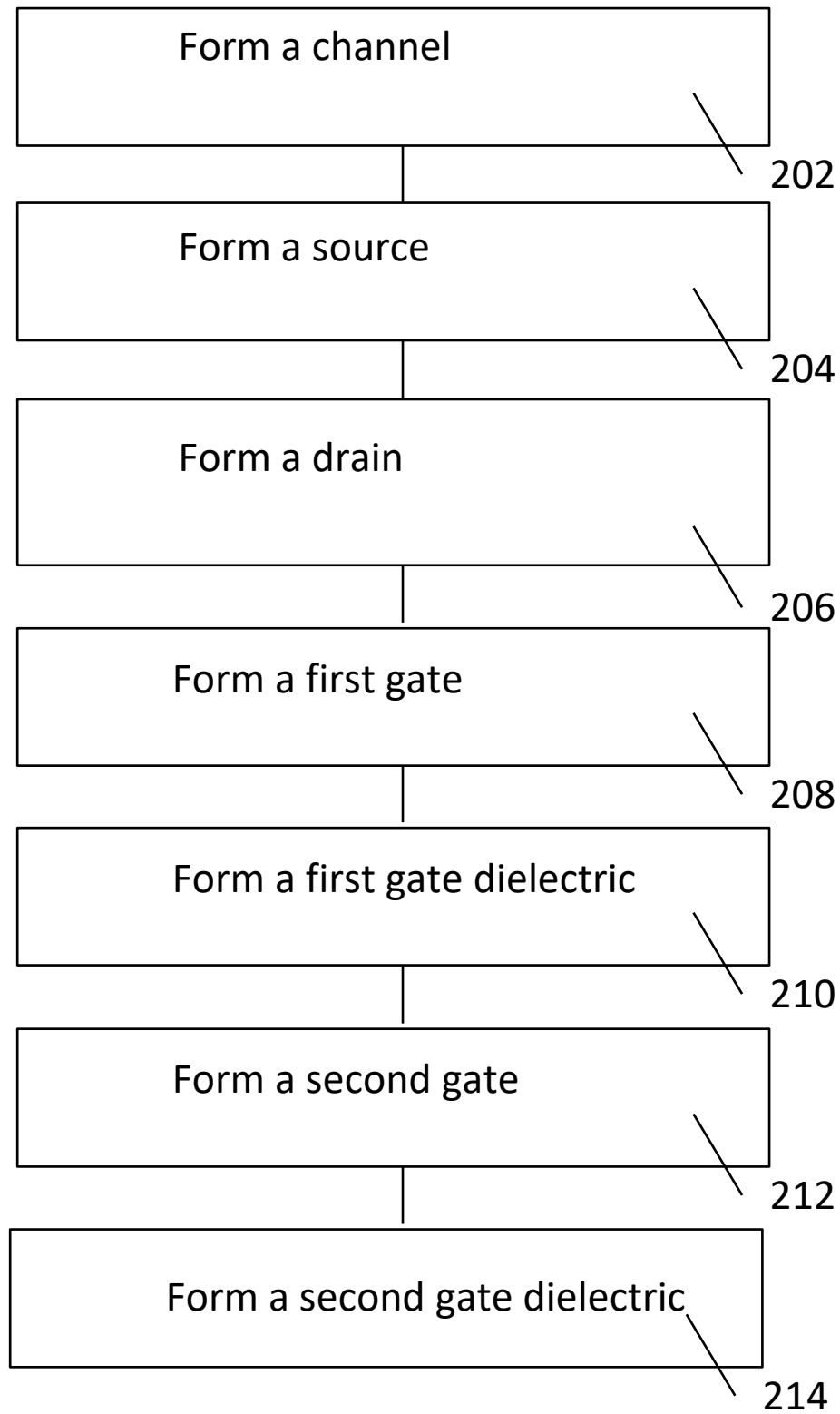


FIG. 3

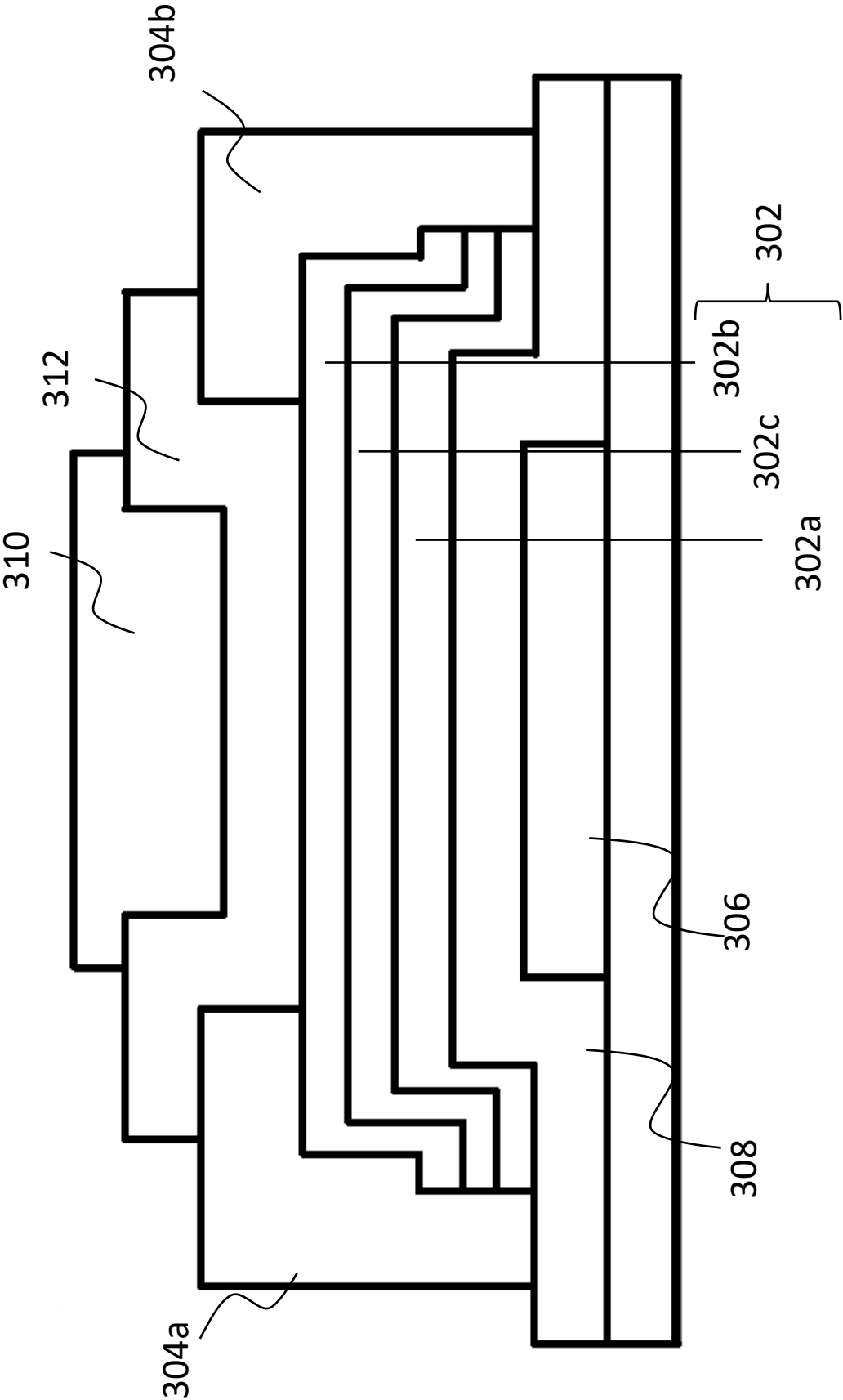


FIG. 4



FIG. 5A

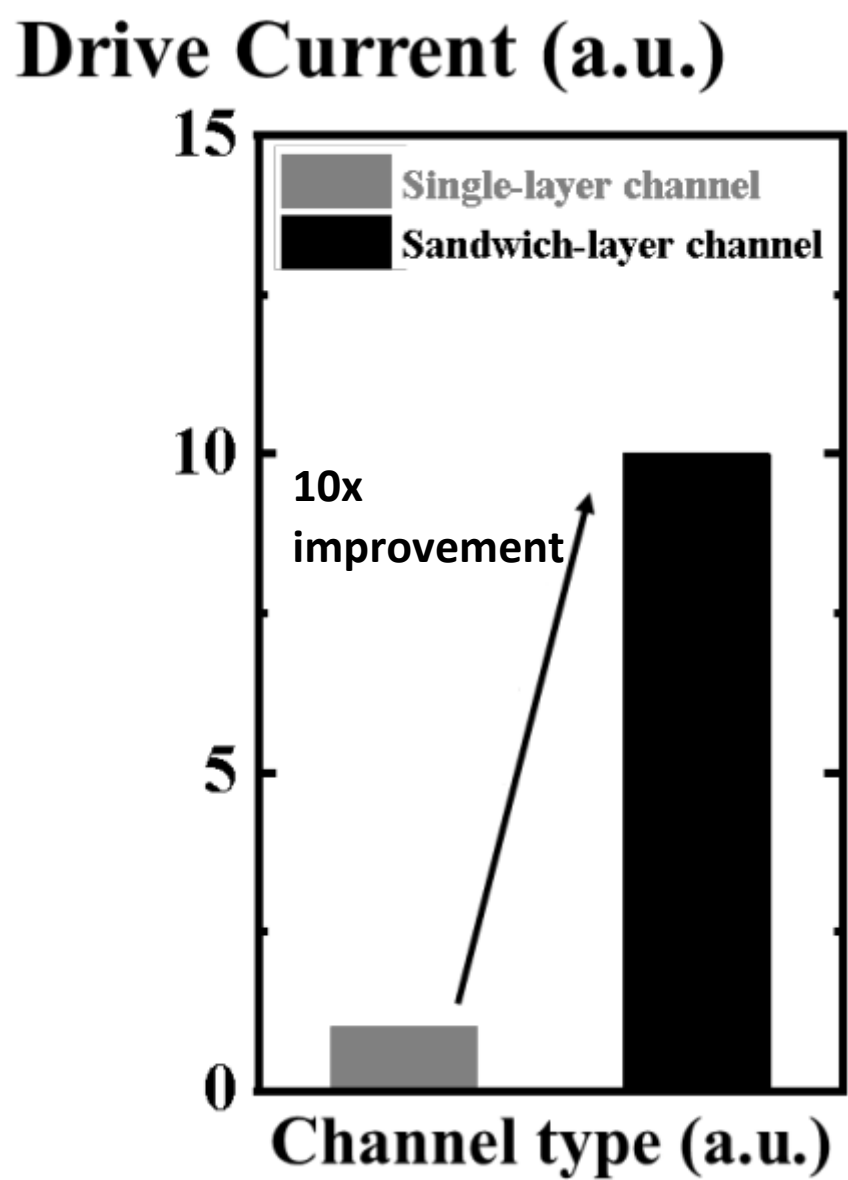


FIG. 5B

Subthreshold swing (a.u.)

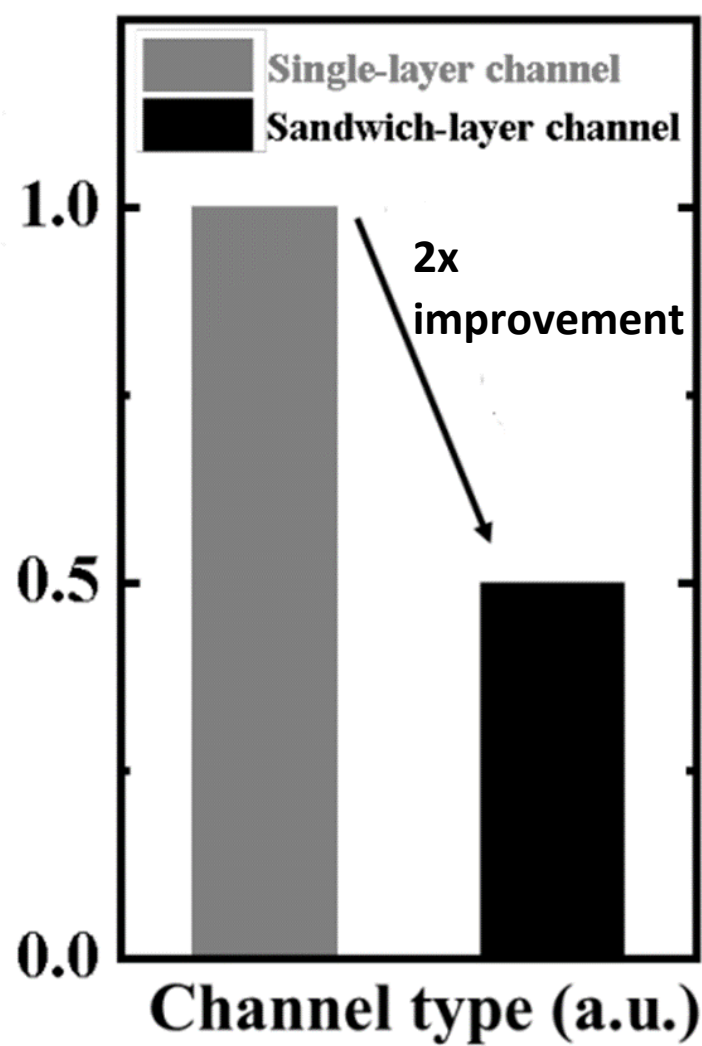


FIG. 5C

Defect Hysteresis (a.u.)

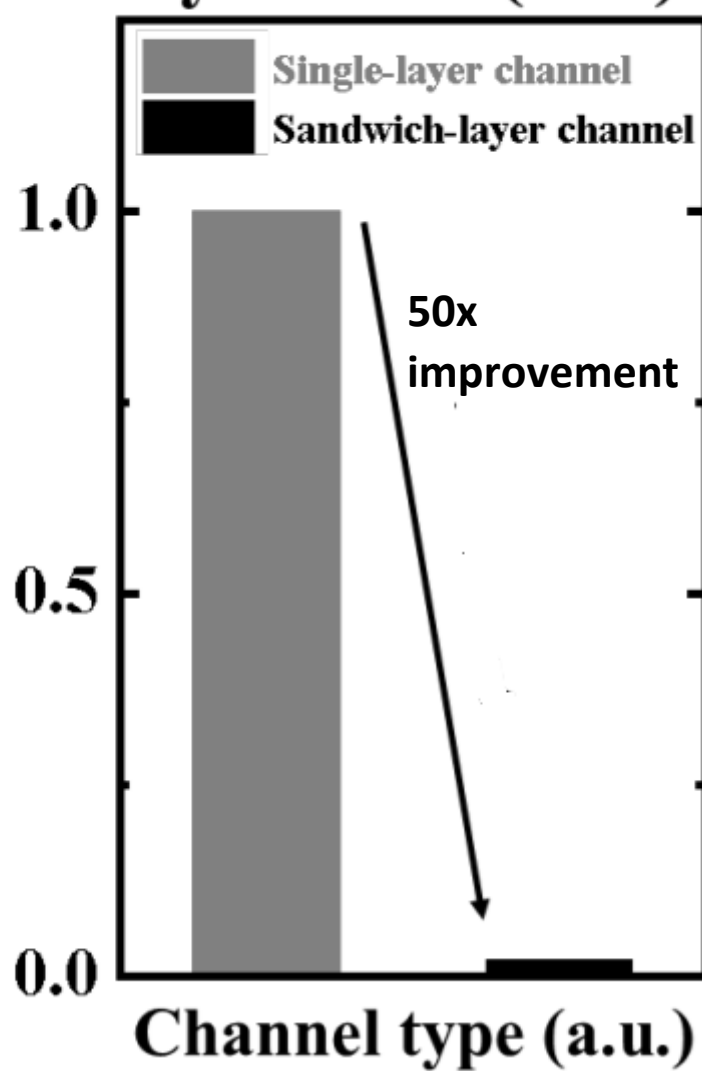


FIG. 5D

Defect Density (a.u.)

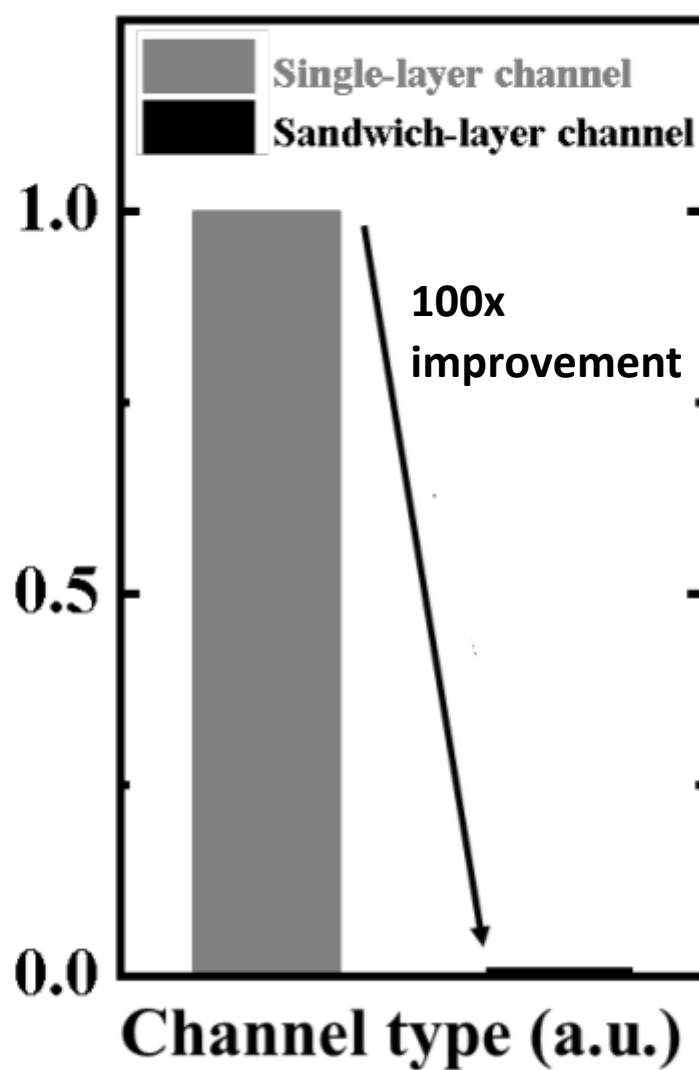


FIG. 6A

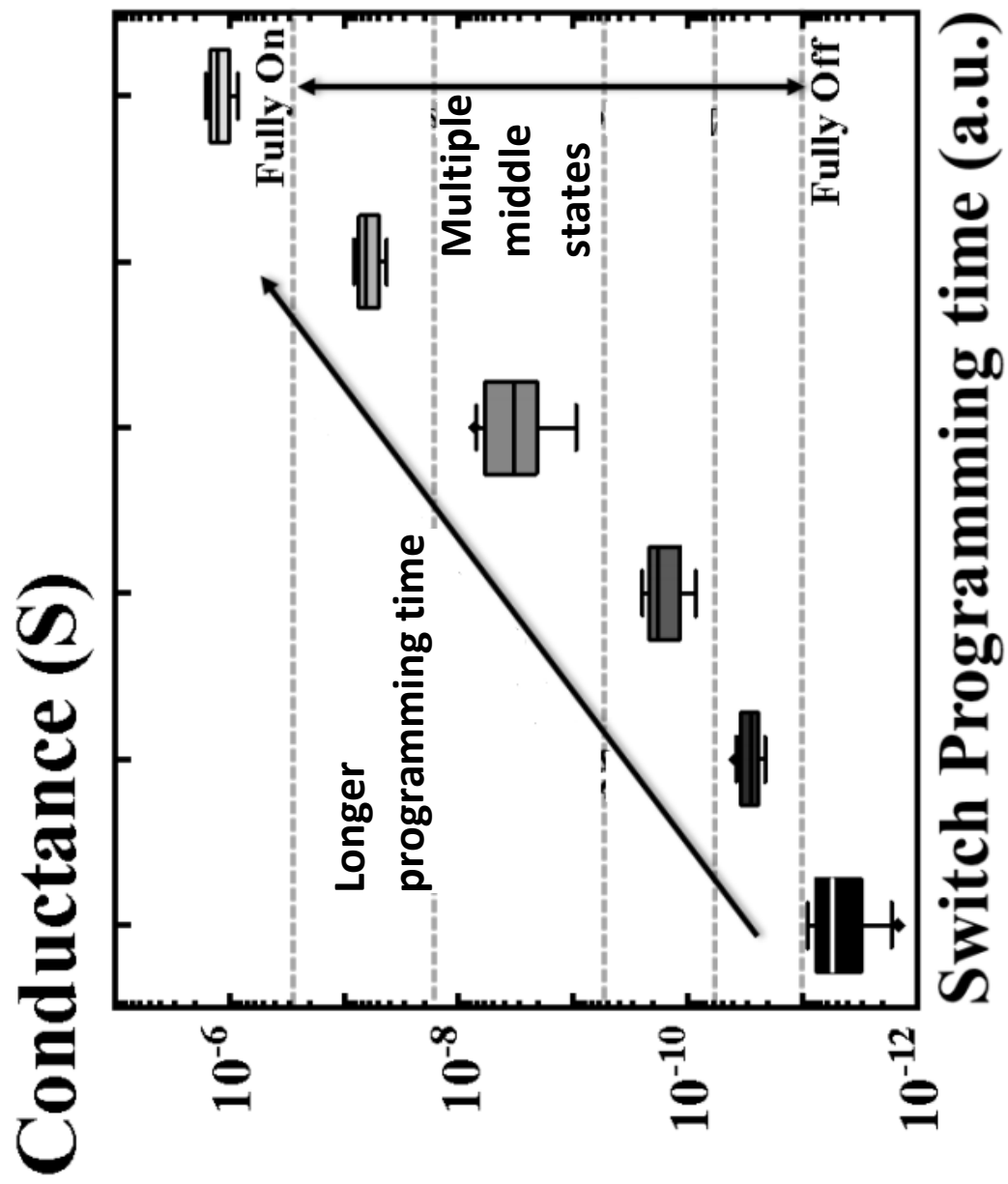


FIG. 6B

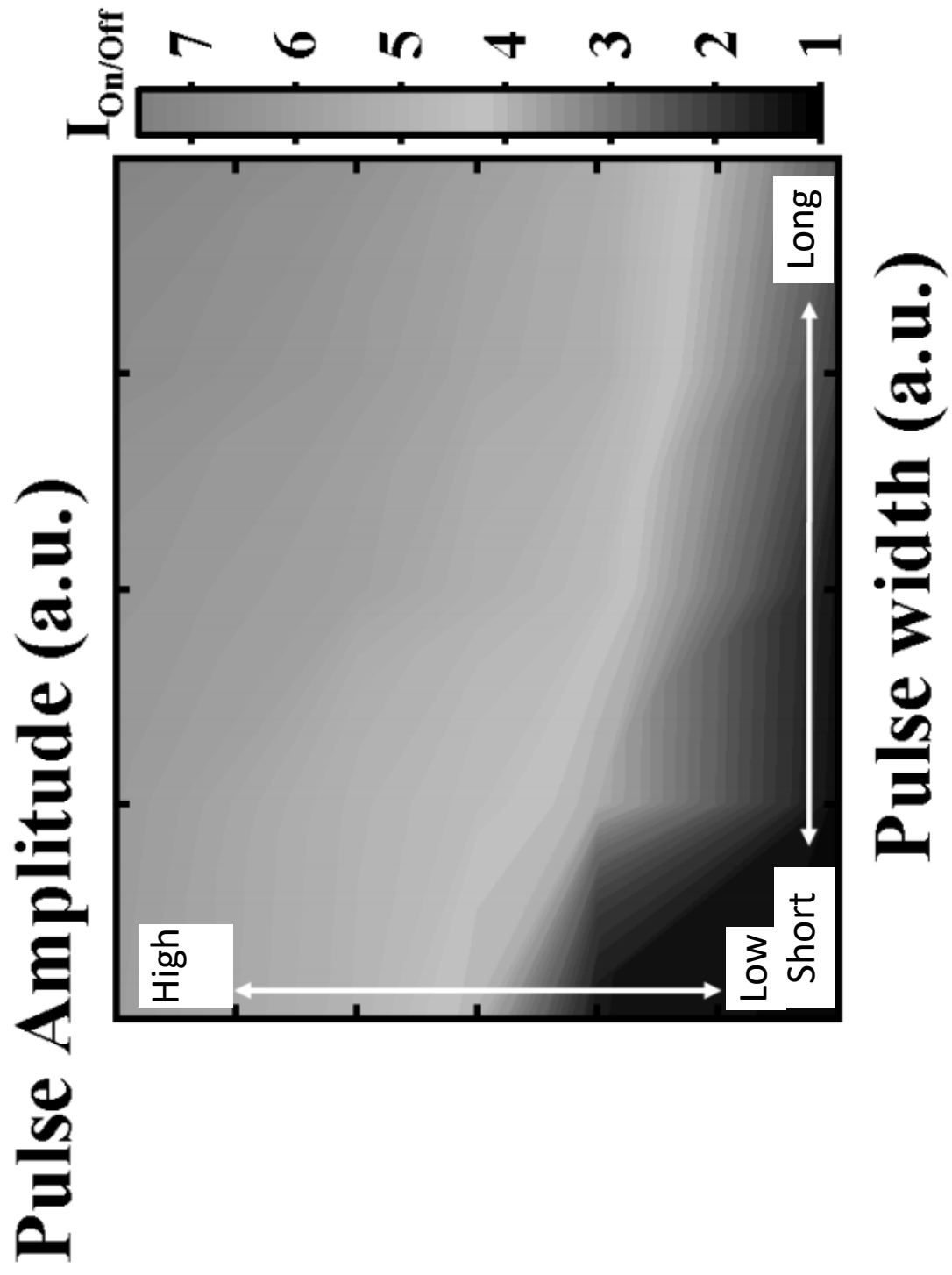


FIG. 7A

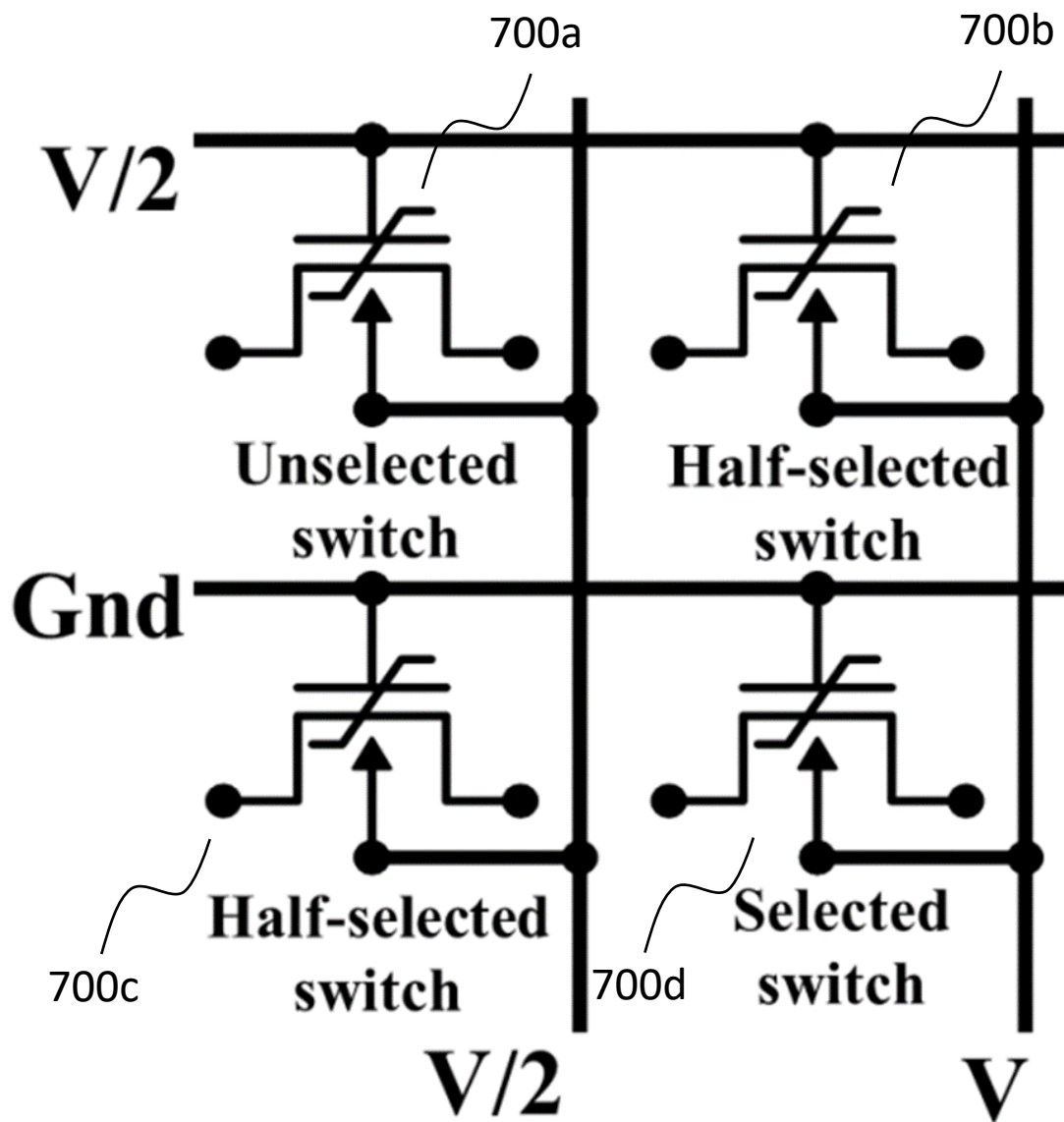


FIG. 7B

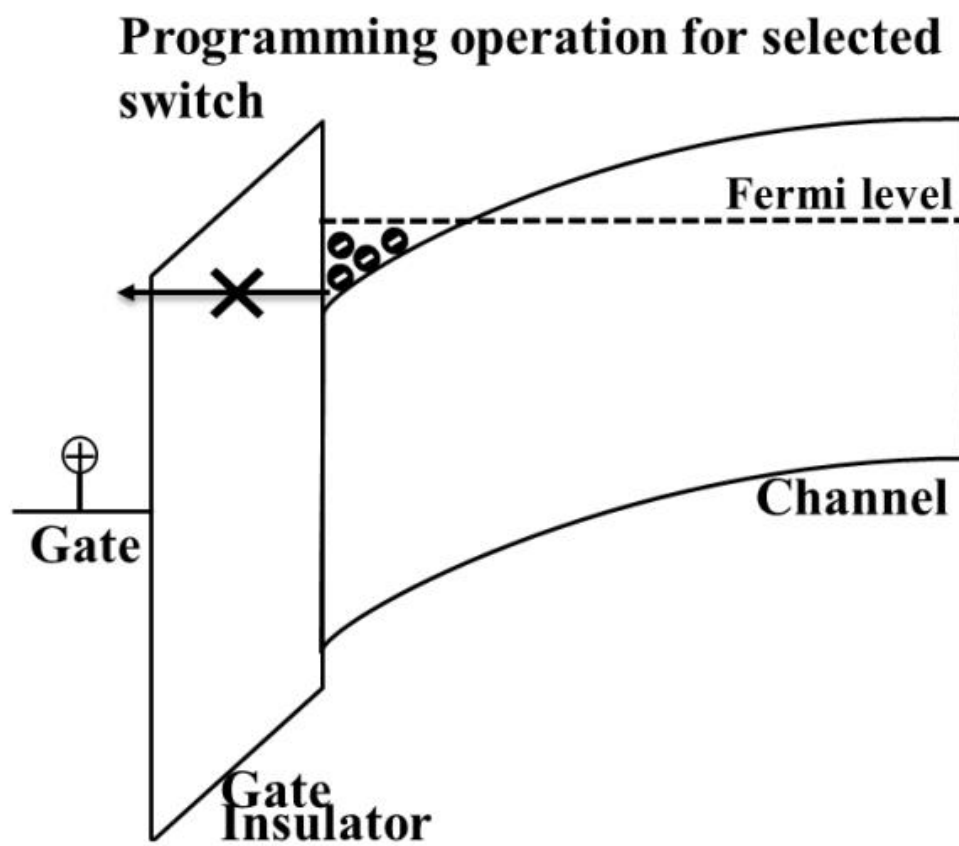


FIG. 7C

Array routing area (a.u.)

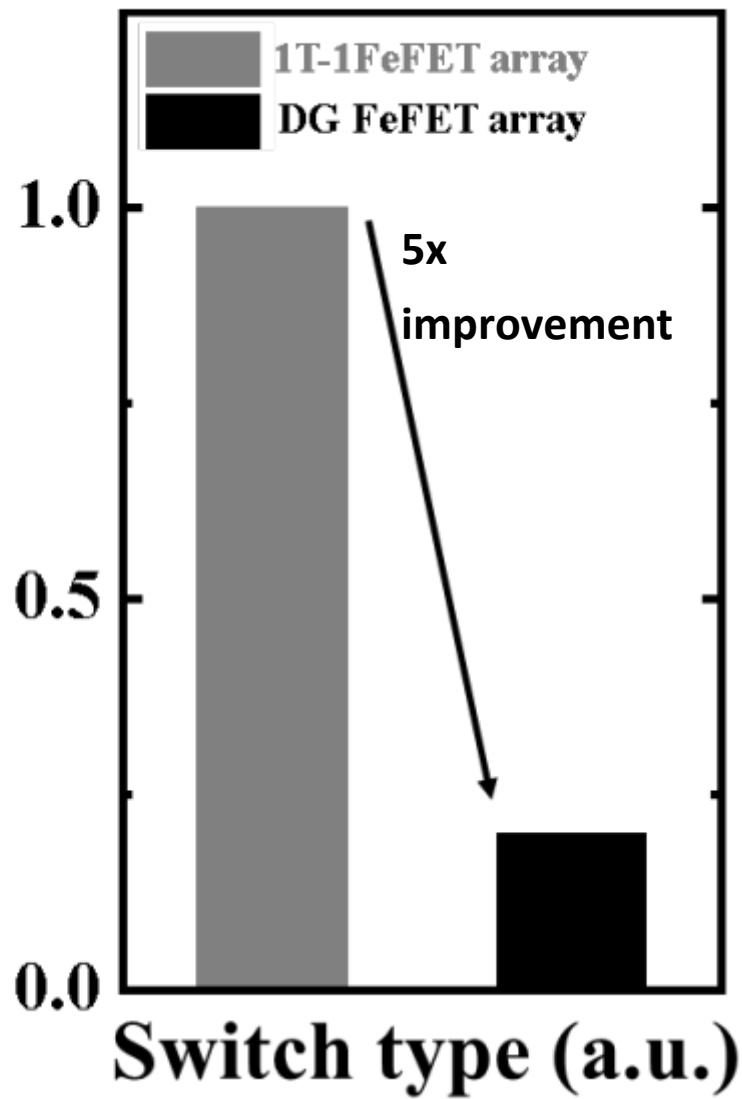


FIG. 8A

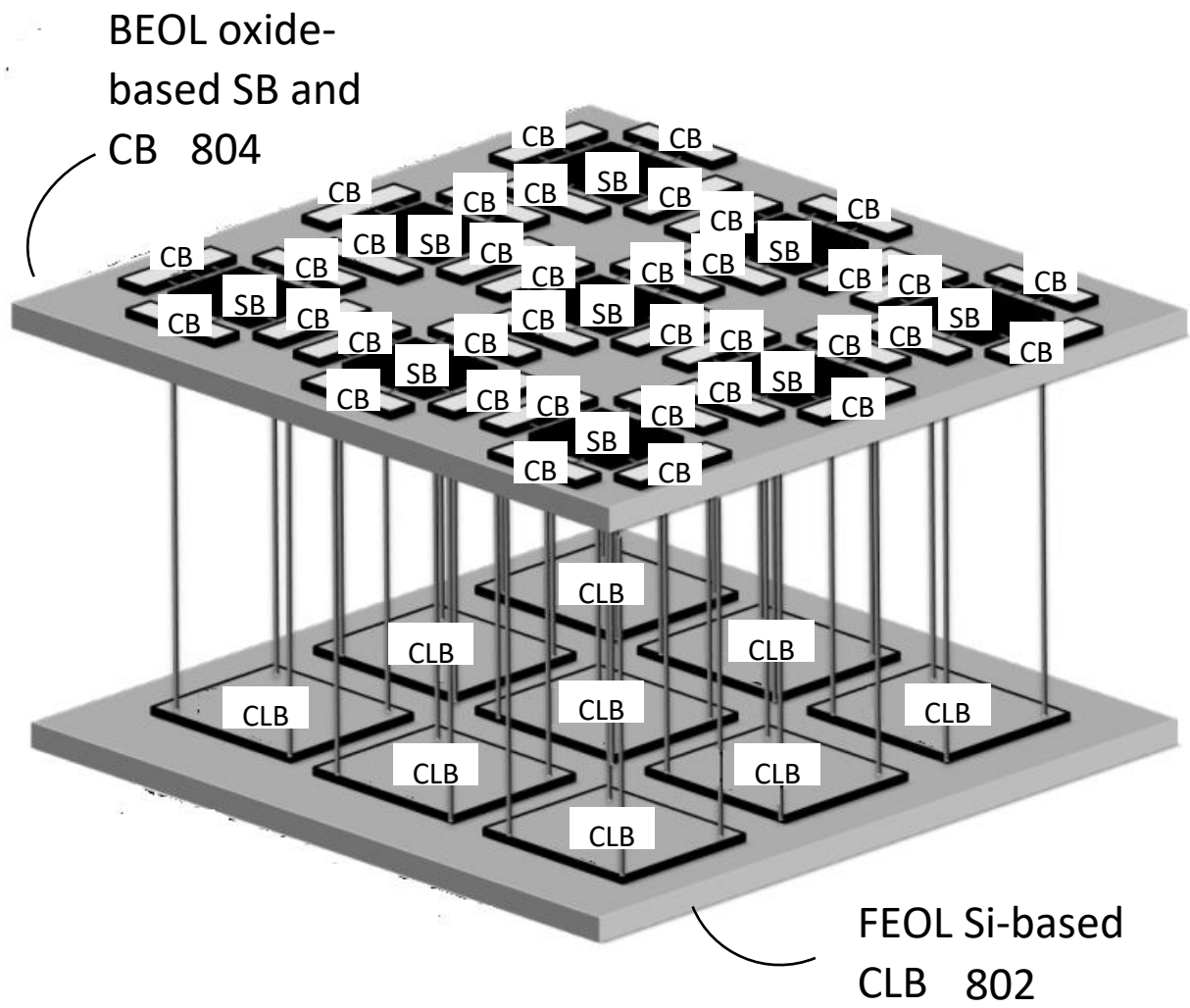


FIG. 8B

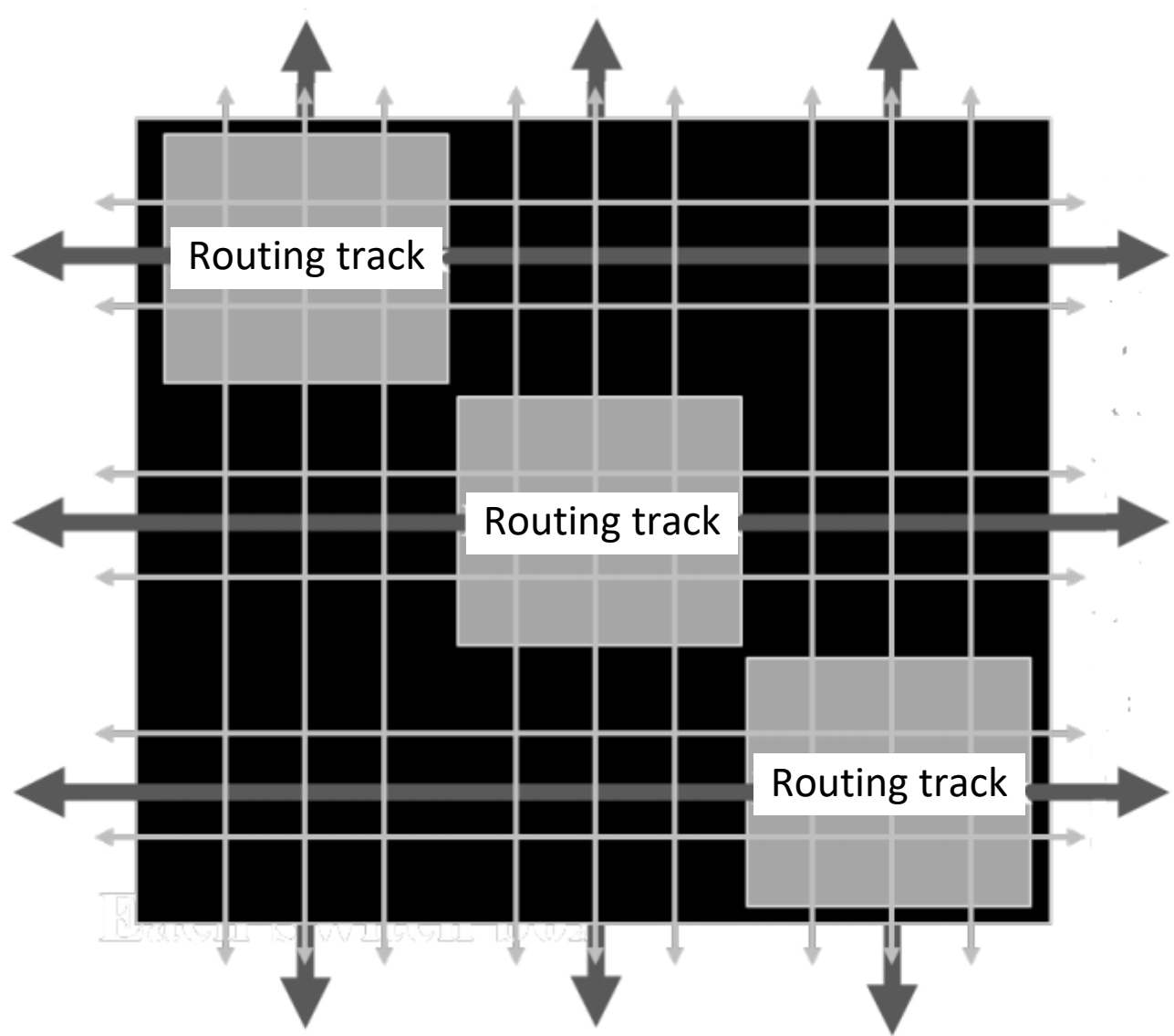


FIG. 9A

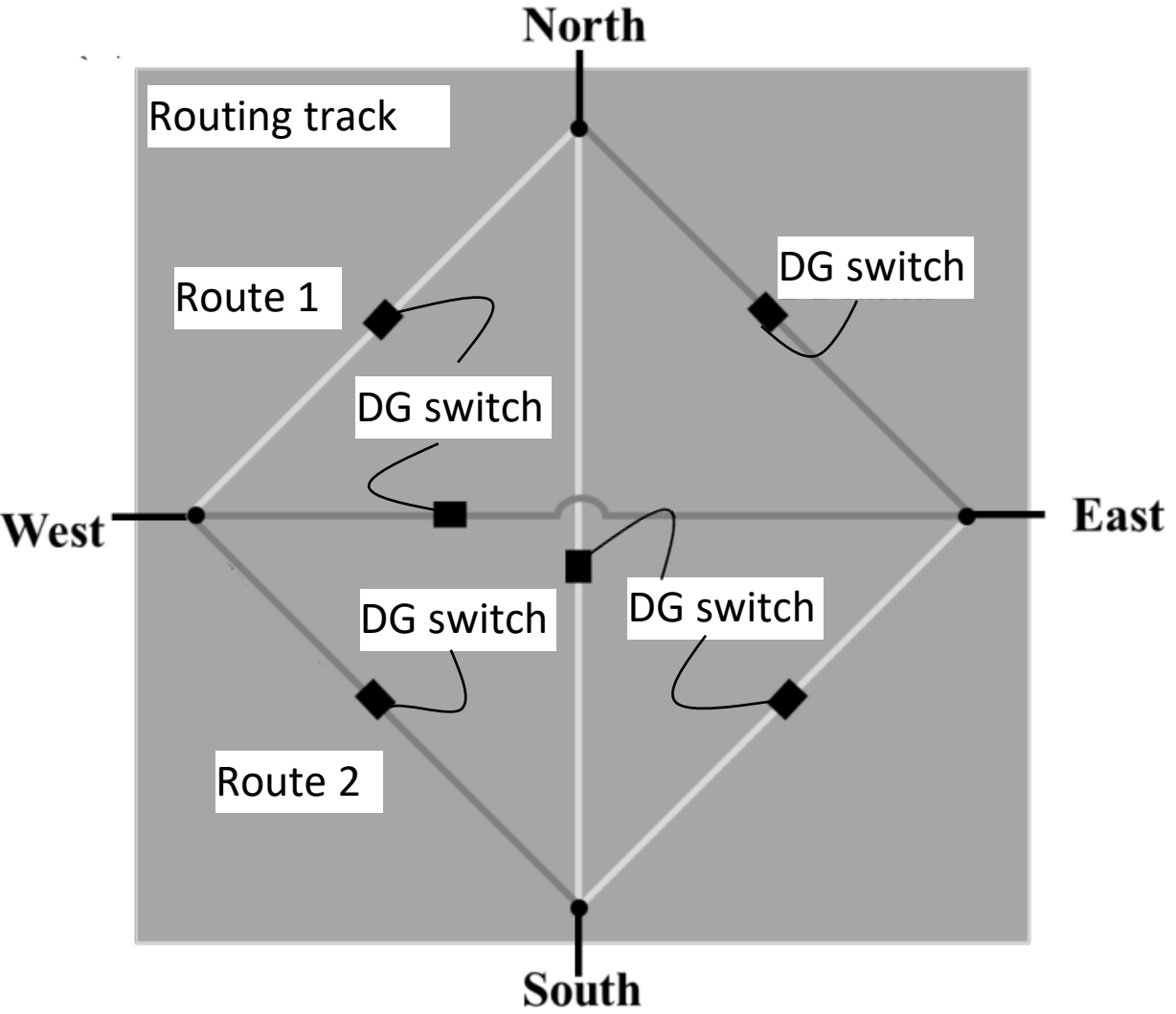


FIG. 9B

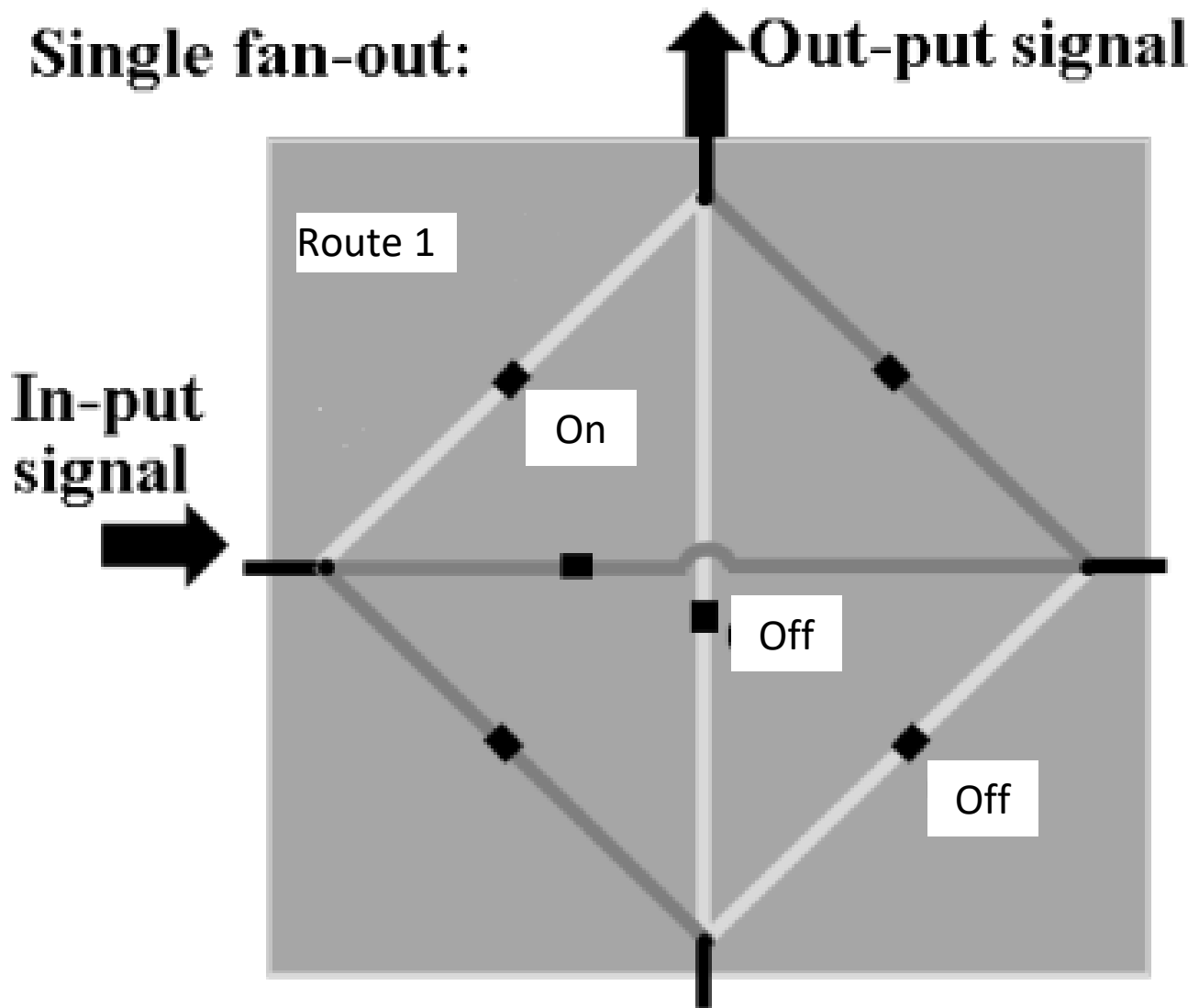


FIG. 9C

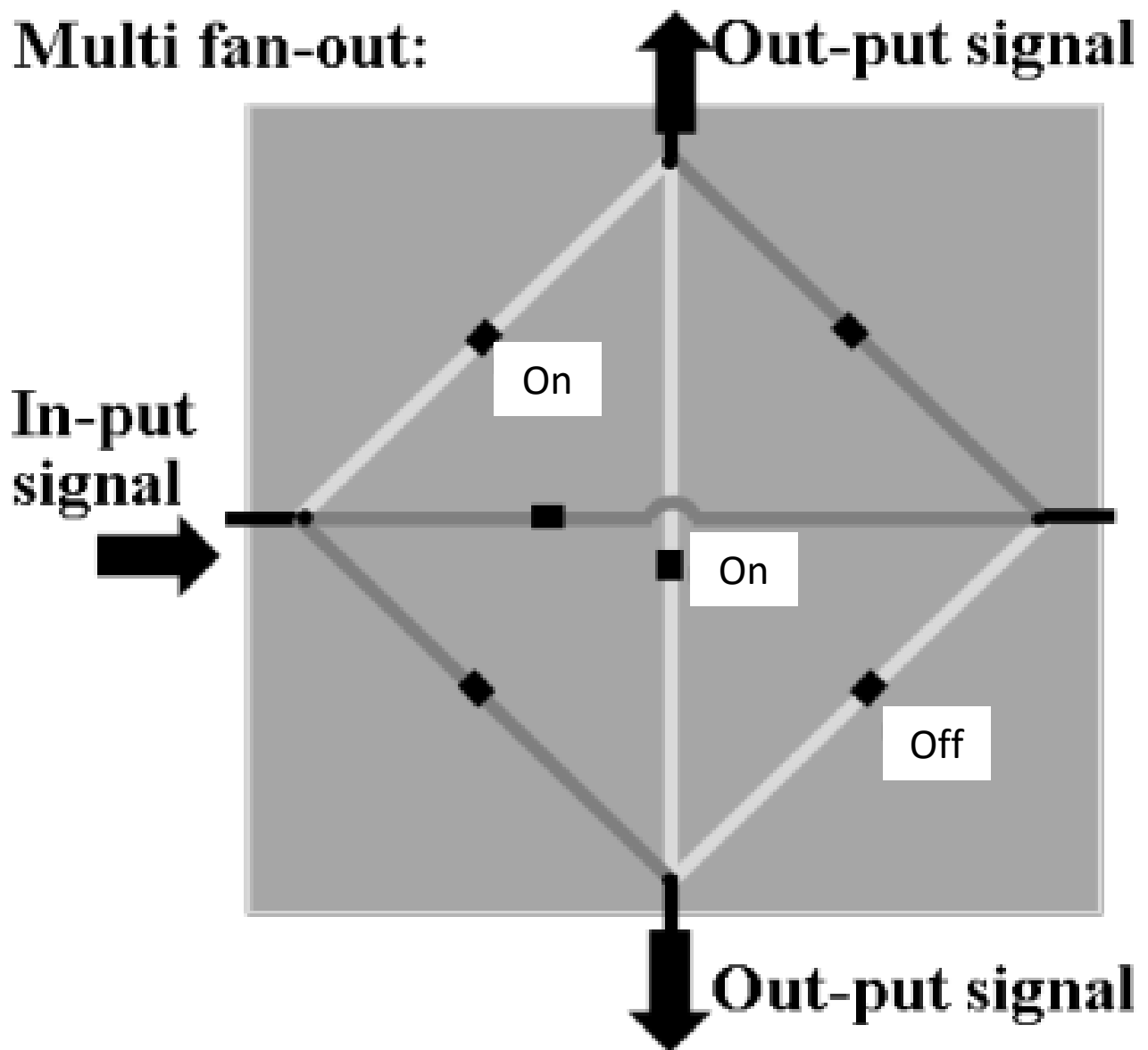


FIG. 10A

Total FPGA Area (a.u.)

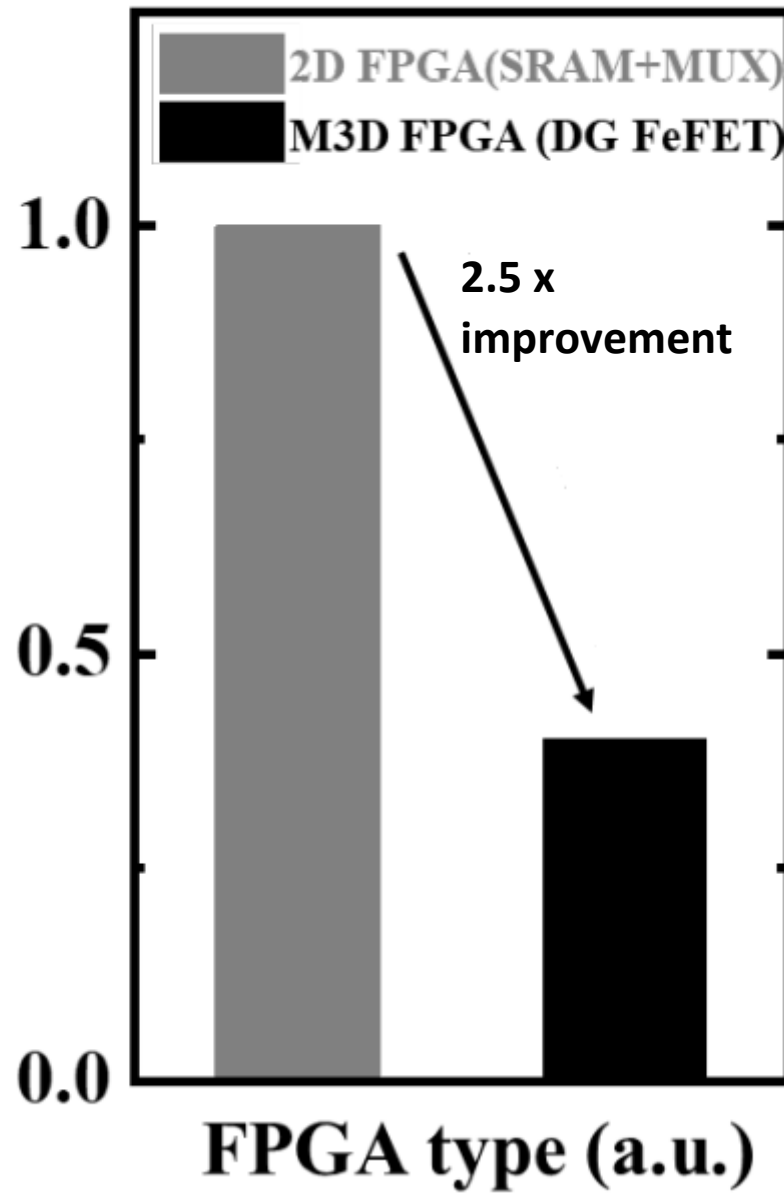


FIG. 10B

Total FPGA Energy (a.u.)

