ABSTRACT OF THE DISCLOSURE

PRESERVING THE ZERO MARK FOR WAFER ALIGNMENT

A method of preserving alignment marks through steps of depositing intermetal dielectric, depositing refractory metal, and planarizing the wafer is described. After deposition of a layer of first metal a layer of first intermetal dielectric is deposited on an integrated circuit wafer. The first intermetal dielectric is then etched away from the alignment region of the wafer. A layer of second metal is then deposited. A layer of second intermetal dielectric is then deposited. The layer of second intermetal dielectric is left in place in the alignment region, a layer of refractory metal is deposited, and the wafer is planarized. The refractory metal and second intermetal dielectric are then cleared from the alignment region. The second intermetal dielectric protects the alignment marks during wafer planarization. A layer of third metal can then be deposited and the alignment marks are be preserved.

(FIGURE 6 IS SUGGESTED FOR PUBLICATION)