# NONVOLATILE MEMORY HAVING HIGH GATE COUPLING CAPACITANCE

## CROSS-REFERENCE TO RELATED APPLICATIONS

The present application claims the benefit of priority under Title 35, United States Code § 119(e) of U.S. Provisional Application Number 60/151,458 filed August 30, 1999. The present application is related to the following commonly assigned applications: "Integrated Circuit Having Optimized Gate Coupling Capacitance", Application No. 09/387,710 filed August 30, 1999; "Integrated Circuit Having Improved Gate Coupling Capacitance", Application No. 09/385,534 filed August 30, 1999; and "Integrated Circuit Having Resistance To Silicide Crack", Application No. 09/385,164 filed August 30, 1999.

## TECHNICAL FIELD

The present invention relates generally to an integrated circuit having increased gate coupling capacitance. The present invention further relates to an integrated circuit having a conductive layer optimized for gate coupling capacitance.

## BACKGROUND ART

The present invention applies particularly to the fabrication of nonvolatile memory integrated circuits (e.g., flash, EPROM, EEPROM, etc.), but may find applications in other integrated circuits. Nonvolatile memory integrated circuits are used in a wide variety of commercial and military electronic devices, including hand held telephones, radios and digital cameras. The market for these electronic devices continues to demand lower voltage, lower power consumption and decreased chip size. Also, the demand for greater functionality is driving the design rule lower, from the 0.35 - 0.25 micron technology of today to 0.18 micron, 0.15 micron and lower.

A conventional flash memory cell of a flash memory IC is illustrated in FIGURES 1 and 2. FIG. 1 depicts a cross-sectional view along the bit line direction of a single flash memory cell 10 on a substrate 11. Cell 10 includes a first transistor 12 and a second transistor 14. Each of transistors 12, 14 includes a tunnel oxide layer 16, a first polysilicon layer 18, 20, an interpoly dielectric layer 22, 24, a second polysilicon layer 26, 28, a silicide layer 30, 32 and sidewall spacers 34, 36.

With reference first to FIGS. 2-7, a conventional flash memory cell fabrication process is illustrated. A substrate 11 is shown in FIGS. 2-7 in a cross-sectional view along the word line direction. Substrate 11 includes a shallow trench isolation structure (STI) 40 between devices (not shown), such as, metal-oxide-semiconductor field effect transistors (MOSFETs), memory cells, or other devices. STI 40 includes an oxide fill material 42. A tunnel oxide layer 16 is provided above substrate 11. First and second polysilicon wings 46, 48 are patterned in first polysilicon layer

20. Interpoly dielectric layer 24 is provided above polysilicon wings 46, 48 and also above STI 40. Second polysilicon layer 28 and silicide layer 32 are provided above interpoly dielectric layer 24.

Referring now to FIG. 3, STI 40 is formed by first applying a pad oxide layer 50 over substrate 11 and subsequently growing or depositing a nitride layer 52. A STI mask and etch step forms STI recess 54. Referring now to FIG. 4, an STI liner oxide 56 is provided to line recess 54 followed by a trench fill with a PECVD oxide fill material 58 (Plasma Enhanced Chemical Vapor Deposition). As shown in FIG. 5, a planarization step and a trench CMP (Chemical Mechanical Polishing) step are applied to PECVD oxide fill material 58 to remove the oxide above nitride layer 52 and partially along sides 60, 62 of nitride layer 52.

Referring now to FIG. 6, a nitride strip step removes nitride layer 52. Pad oxide layer 50 is removed by sacrificial oxidation. Subsequently, a tunnel oxide layer 62 is grown above substrate 11. Referring now to FIG. 7, a first polysilicon layer 20 is applied. Layer 20 is patterned (i.e., masked and etched) to form wings 46, 48. Referring again to FIG. 2, interpoly dielectric layer 24 (e.g., Oxide Nitride Oxide) is grown over wings 46, 48. Second polysilicon layer 28 is then deposited, followed by deposition of silicide layer 32.

In operation, a data element is stored on polysilicon layers 18, 20 (FIG. 1), also called the floating gate. Access to the data element is obtained via second polysilicon layers 26, 28, also called the control gate or wordline. While the voltage of the data element is typically on the order of 3.3 Volts, the voltage that must be applied to the control gate to access this data element is on the order of 9 Volts. Thus, a charge pump (not shown) is located on the flash memory IC to raise the chip voltage from 3.3 Volts to a target voltage of 9 Volts.

Charge pumps are large, taking up substantial space on the flash memory cell and further compromising the reliability of the IC. As design rules continue to decrease, the size of the charge pump becomes an obstacle in chip design. However, the size of the charge pump can be decreased by decreasing the target voltage. The target voltage can be decreased by increasing the gate coupling ratio ($\alpha$) of the memory cell. Gate coupling ratio ($\alpha$) is defined as:

$$\alpha = C_{ono} / (C_{ono} + C_{tox})$$

where $C_{ono}$ is the capacitance between first polysilicon layer 18, 20 and second polysilicon layer 26, 28 and $C_{tox}$ is the capacitance between substrate 11 and first polysilicon layer 26, 28.

Accordingly, what is needed is an IC and method of fabricating an IC to increase the gate coupling ratio, decreasing the target voltage of the charge pump, thereby decreasing power consumption of the IC, decreasing the size of the charge pump, and improving reliability.

## DISCLOSURE OF INVENTION

These and other limitations of the prior art are addressed by the present invention which is directed to an integrated circuit having an increased gate coupling capacitance. The integrated circuit includes a substrate having a surface, the substrate having a trench extending

below the surface. A trench fill material is disposed in the trench and has a portion extending above the surface. A first conductive layer is adjacent the trench fill material and has a portion extending over the portion of the insulative material. An insulative layer is adjacent the first conductive layer and a second conductive layer is adjacent the insulative layer.

According to another embodiment of the present invention, integrated circuit having an increased gate coupling capacitance is disclosed. The integrated circuit is fabricated by a process including forming a trench in the substrate, the trench extending below a surface of the substrate; providing a trench fill material in the trench such that the trench fill material extends above the surface of the substrate; and providing a first conductive layer over at least a portion of the trench fill material.

## BRIEF DESCRIPTION OF DRAWINGS

The invention will become more fully understood from the following detailed description, taken in conjunction with the accompanying drawings, wherein like reference numerals refer to like parts, and in which:

FIGURE 1 depicts a cross-sectional view of a conventional flash memory cell along the bit line direction;

FIGURE 2 depicts a cross-sectional view of the memory cell of FIG. 1 along the word line direction;

FIGURE 3 depicts steps in the process of fabrication of the conventional flash memory cell of FIGS. 1 and 2;

FIGURE 4 depicts steps in the process of fabrication of the conventional flash memory cell of FIGS. 1 and 2;

FIGURE 5 depicts steps in the process of fabrication of the conventional flash memory cell of FIGS. 1 and 2;

FIGURE 6 depicts steps in the process of fabrication of the conventional flash memory cell of FIGS. 1 and 2;

FIGURE 7 depicts steps in the process of fabrication of the conventional flash memory cell of FIGS. 1 and 2;

FIGURE 8 depicts a portion of an integrated circuit according to an exemplary embodiment of the present invention;

FIGURE 9 depicts steps in the process of fabrication of the portion of an integrated circuit of FIG. 8;

FIGURE 10 depicts steps in the process of fabrication of the portion of an integrated circuit of FIG. 8;

FIGURE 11 depicts steps in the process of fabrication of the portion of an integrated circuit of FIG. 8;

FIGURE 12 depicts steps in the process of fabrication of the portion of an integrated circuit of FIG. 8;

FIGURE 13 depicts steps in the process of fabrication of the portion of an integrated circuit of FIG. 8;

FIGURE 14 depicts steps in the process of fabrication of a portion of an integrated circuit according to a second exemplary embodiment of the present invention;

FIGURE 15 depicts steps in the process of fabrication of the portion of an integrated circuit of FIG. 14;

FIGURE 16 depicts steps in the process of fabrication of the portion of an integrated circuit of FIG. 14;

FIGURE 17 depicts steps in the process of fabrication of the portion of an integrated circuit of FIG. 14;

FIGURE 18 depicts steps in the process of fabrication of the portion of an integrated circuit according to a third exemplary embodiment of the present invention;

FIGURE 19 depicts steps in the process of fabrication of the portion of an integrated circuit of FIG. 18;

FIGURE 20 depicts steps in the process of fabrication of the portion of an integrated circuit of FIG. 18;

FIGURE 21 depicts steps in the process of fabrication of the portion of an integrated circuit of FIG. 18;

FIGURE 22 depicts steps in the process of fabrication of the portion of an integrated circuit of FIG. 18; and

FIGURE 23 depicts steps in the process of fabrication of the portion of an integrated circuit of FIG. 18.

## MODE(S) FOR CARRYING OUT THE INVENTION

As stated hereinabove, an increase in the gate coupling ratio is required to decrease the target voltage of the charge pump to, in turn, decrease the size of the charge pump. The present invention achieves an increase in the gate coupling ratio by increasing the capacitance across the interpoly dielectric layer between first and second polysilicon layers (a.k.a., "poly 1" and "poly 2", respectively). As will be shown, this increase is obtained by increasing the surface area across which poly 1 and poly 2 are in contact, thereby increasing the surface area of the capacitor formed by poly 1, poly 2 and the interpoly dielectric layer.

With reference now to FIG. 8, a portion 100 of an integrated circuit (IC) having an improved gate coupling ratio according to one embodiment of the present invention is shown in cross-section along the word line direction. The IC is a flash memory device, but may alternatively be another nonvolatile memory (e.g., EPROM, EEPROM, etc.) or other integrated circuit. A semiconductor substrate 102 (e.g., silicon, germanium, gallium arsenide, etc.) includes an isolation structure 104 defined in a recess or trench 106. In this embodiment, isolation structure 104 is a shallow trench isolation structure containing a trench fill material 108. Trench fill material 108 is an insulative material, such as, PECVD oxide. Trench fill material 108 extends from the bottom of recess 106 toward an upper surface 110 of substrate 102 and includes a portion 109 extending above upper surface 110. Recess 106 has a bottom surface 105 approximately 1000 to 7000 Angstroms (Å) below upper surface 110 and preferably about 4000 Å below upper surface 110.

A first insulative layer 111, such as, a tunnel oxide layer, is provided over upper surface 110 of substrate 102 and over side walls 112, 114 of recess 106. A first conductive layer 116, such as, doped polysilicon is provided adjacent first insulative layer 111 and trench fill material 108. First conductive layer 116 is masked and etched to form a first conductive wing or portion 118 and a second conductive wing or portion 120. First conductive layer 116 also defines a via 140 between conductive portions 118, 120. First and second conductive portions 118, 120 extend at least partially over portion 109 of trench fill material to increase the surface area that conductive layer 116 has exposed to the subsequent layers, relative to the prior art. This increase in surface area results in an increase in capacitance, which raises the gate coupling ratio as described hereinbefore. In this exemplary embodiment, an upper surface 134 of trench fill material 108 is at least 100 Å above upper surface 110 of substrate 102. Upper surface 134 may be as high as 5000 Å above upper surface 110 of substrate 102, and may be approximately 1000 to 2000 Å above upper surface 110 of substrate 102.

A second insulative layer 122, such as, an interlevel dielectric layer (e.g., Oxide Nitride Oxide) is provided over first conductive layer 116 and trench fill material 108. Insulative layer 122 forms an insulative barrier between conductive portions 118, 120. A second conductive layer 124, such as, doped polysilicon is provided over second insulative layer 122. Thus, insulative layer 122 also insulates layers 116 and 124 from one another. A silicide layer 126 is provided over second conductive layer 124.

Referring now to FIGS. 9-13, a method of fabricating portion 100 is described. In FIG. 9, isolation structure 104 is formed by providing an insulative layer 128 including an oxide material (e.g., a pad oxide material, such as, $SiO_2$) over substrate 102. Layer 128 is grown in a conventional thermal process, or applied by a chemical vapor deposition (CVD) or a physical vapor deposition (PVD) process. Subsequently, a barrier layer 130, preferably a silicon nitride layer, e.g., $Si_3N_4$, is applied over insulative layer 128 with a thickness of approximately 500 to 5000 Å,

preferably about 1000 to 2000 Å. Using a standard photolithographic process, an aperture 129 is formed in layers 128, 130 at the desired location. A conventional trench etching process, such as a dry or plasma etch, is then utilized to etch recess 106 in substrate 102. A liner oxidation step forms an insulative liner (not shown) along the walls of recess 106.

Next, recess 106 is filled with insulative trench fill material 108 by, for example, a PECVD oxide step. Trench fill material 108 is deposited with a thickness less than that of the conventional trench fill material 58 (FIG. 4). Specifically, trench fill material 108 is deposited with a thickness of less than approximately 7000 Å assuming a trench depth from upper surface 110 to bottom surface 105 of approximately 4000 Å.

Referring now to FIG. 10, a mask layer 131 (e.g., a photoresist layer) is applied over trench fill material 108. Mask layer 131 preferably is applied such that a lateral width of opening 133 is somewhat wider than a lateral width of barrier layer 130 to ensure that barrier layer 130 is completely removed by subsequent etching.

Referring now to FIG. 11, an etching step removes insulative layer 128, barrier layer 130, and a portion 135 of trench fill material 108. In this embodiment, trench fill material 108 is etched until upper surface 110 of substrate 102 is exposed. It can be seen that a portion 109 of trench fill material 108 extends above upper surface 110. Note that in the prior art (FIG. 6) only the nitride layer 52 is etched off by selective etching.

In FIG. 12, a sacrificial oxidation and strip off step is performed to round corners 136, 138. In sacrificial oxidation, a thin oxide layer is grown and then stripped off to get the trench corner rounding. This rounding prevents the "double hump effect" in the I-V characteristic curve of the transistor. During this sacrificial oxidation, the level of trench fill material 108 may or may not be lowered further from the etching associated with FIG. 11.

In FIG. 13, first insulative layer 111 is thermally grown over substrate 120 or otherwise provided over substrate 120 using a known deposition process (e.g., chemical vapor deposition, physical vapor deposition). In this embodiment, first insulative layer 111 is a tunnel oxide layer ($SiO_2$). Next, first conductive layer 116 ("poly 1") is deposited over first insulative layer 111 and trench fill material 108. Note that poly 1 layer 116 extends over portion 109 of trench fill material 108.

Referring again to FIG. 8, poly 1 layer 116 is masked and etched (i.e., patterned) to form via 140 between first and second conductive portions or wings 118, 120. Second insulative layer 122 is then provided or grown (e.g., ONO) adjacent first conductive layer 116. Second insulative layer 122 electrically isolates first and second conductive portions 118, 120. Next, second conductive layer 124 (e.g., polysilicon) is deposited, followed by deposition of silicide layer 126.

Referring now to FIGS. 14-17, an alternative embodiment of the present invention is disclosed. In this second embodiment, the provision of mask layer 131 as described in FIG. 10 of

the first embodiment is eliminated. With reference to FIG. 14, isolation structure 204 is formed by providing an insulative layer 228 including an oxide material (e.g., a pad oxide material, such as, $SiO_2$) over substrate 202. Layer 228 is provided similarly to layer 128 as described in FIG. 9 above. Subsequently, a barrier layer 230, preferably a silicon nitride layer, e.g., $Si_3N_4$, is applied over insulative layer 228 with a thickness somewhat greater than that of layer 128. For example, barrier layer 230 is between approximately 1000 Angstroms and 5000 Angstroms. Using a standard photolithographic process, an aperture 229 is formed in layers 228, 230 at the desired location. A conventional trench etching process, such as a dry or plasma etch, is then utilized to etch recess 206 in substrate 202. A liner oxidation step forms an insulative liner (not shown) along the walls of recess 206.

Next, recess 206 is filled with insulative trench fill material 208 by, for example, a PECVD oxide step. Trench fill material 208 is deposited over recess 206 and barrier layer 230 with a thickness less than that of the conventional trench fill material 58 (FIG. 4). Specifically, trench fill material 208 is deposited with a thickness of less than approximately 7000 Å, assuming a trench depth from upper surface 210 to bottom surface 205 of approximately 4000 Å. Next, trench fill material 208 is planarized (e.g., chemical mechanical planarization or CMP) until an upper surface 237 of material 208 is approximately coplanar with an upper surface of barrier layer 230. Thus, as will be seen, the thickness of barrier layer 229 assists in defining the extent to which trench fill material 208 extends above an upper surface 210 of substrate 202.

Referring now to FIG. 15, a strip step removes insulative layer 228 and barrier layer 230, leaving trench fill material 208. It can be seen that a portion 209 of trench fill material 208 extends above upper surface 210. Also in FIG. 15, a sacrificial oxidation and strip off step is performed to round corners 236, 238. During this sacrificial oxidation, the height and width of trench fill material 208 may or may not be selectively reduced.

In FIG. 16, first insulative layer 211 is thermally grown over substrate 220 or otherwise provided over substrate 220 using a known deposition process (e.g., chemical vapor deposition, physical vapor deposition). In this embodiment, first insulative layer 211 is a tunnel oxide layer ($SiO_2$). Next, first conductive layer 216 ("poly 1") is deposited over first insulative layer 211 and trench fill material 208. Note that poly 1 layer 216 extends over portion 209 of trench fill material 208.

Referring now to FIG. 17, poly 1 layer 216 is masked and etched (i.e., patterned) to form via 240 between first and second conductive portions or wings 218, 220. Second insulative layer 222 is then provided or grown (e.g., ONO) adjacent first conductive layer 216. Second insulative layer 222 electrically isolates first and second conductive portions 218, 220. Next, a second conductive layer (not shown) is deposited, followed by deposition of a silicide layer (not shown) in a similar manner as in the first embodiment.

Referring now to FIGS. 18-23, a third exemplary embodiment of the present invention is shown. In this third embodiment, the trench fill material includes a first trench fill material provided in a first fabrication step and a second trench fill material in a second fabrication step. In FIG. 18, isolation structure 304 is formed by providing an insulative layer 328 including an oxide material (e.g., a pad oxide material, such as, $SiO_2$) over substrate 302. Layer 328 is grown in a conventional thermal process, or applied by a chemical vapor deposition (CVD) or a physical vapor deposition (PVD) process. Subsequently, a barrier layer 330, preferably a nitride layer, e.g., $Si_3N_4$, is applied over insulative layer 328 with a thickness of approximately 1000 to 7000 Å, typically 2000 to 4000 Å. Note that this thickness is somewhat thicker than that of the embodiment described in FIG. 9. Using a standard photolithographic process, an aperture 329 is formed in layers 328, 330 at the desired location. A conventional trench etching process, such as a dry or plasma etch, is then utilized to etch recess 306 in substrate 302. A liner oxidation step forms an insulative liner (not shown) along the walls of recess 306.

Next, recess 306 is filled with insulative trench fill material 308 by, for example, a PECVD oxide step. Trench fill material 308 is deposited with a thickness less than that of the conventional trench fill material 58 (FIG. 4). Specifically, trench fill material 308 is deposited with a thickness of less than approximately 7000 Å. Next, trench fill material 308 is planarized (e.g., chemical mechanical planarization or CMP) until an upper surface 337 of material 308 is approximately coplanar with an upper surface of barrier layer 330.

Referring now to FIG. 19, an etching step removes insulative layer 328, barrier layer 330, and a portion 335 of trench fill material 308. In this embodiment, trench fill material 308 is etched until upper surface 310 of substrate 302 is exposed.

Referring now to FIG. 20, an insulative layer 342 (e.g., a CVD oxide) is applied over trench fill material 308 with a thickness of approximately 1000 to 5000 Å, typically 2000 to 4000 Å. Insulative layer 342 is then patterned (i.e., masked and etched, as described with reference to FIG. 10 above) to form a second trench fill material 346 (FIG. 21) above trench fill material 308. It can be seen that trench fill material 346 extends above upper surface 310.

In FIG. 22, a sacrificial oxidation and strip off step is performed to round corners 336, 338. During this sacrificial oxidation, the level of second trench fill material 346 may or may not be lowered further from the stripping associated with FIG. 19. A first insulative layer 311 is thermally grown over substrate 320 or otherwise provided over substrate 320 using a known deposition process (e.g., chemical vapor deposition, physical vapor deposition). In this embodiment, first insulative layer 311 is a tunnel oxide layer ($SiO_2$). Next, first conductive layer 316 ("poly 1") is deposited over first insulative layer 311 and trench fill material 308. In this embodiment, first poly 1 layer 316 also extends over second trench fill material 346.

Referring now to FIG. 23, poly 1 layer 316 is masked and etched (i.e., patterned) to form via 340 between first and second conductive portions or wings 318, 320. Second insulative layer 322 is then provided or grown (e.g., ONO) adjacent first conductive layer 316. Second insulative layer 322 electrically isolates first and second conductive portions 318, 320. Next, a second conductive layer (not shown) is deposited, followed by deposition of a silicide layer (not shown) in a similar manner as in the first embodiment.

While the embodiments illustrated in the FIGS. and described above are presently preferred, it should be understood that these embodiments are offered by way of example only. For example, the specific materials and dimensions utilized in the preferred embodiments disclosed herein are provided as examples and are not meant to preclude the substitution of like materials or dimensions. Also, while the embodiments disclosed are particularly suitable for a flash EPROM or other non-volatile memory, they may find application in non-memory devices. The invention is not limited to a particular embodiment, but extends to various modifications that nevertheless fall within the scope of the appended claims.

## CLAIMS

WHAT IS CLAIMED IS:

1. An integrated circuit (100) having an increased gate coupling capacitance, comprising a substrate (102) having a surface (110), the substrate (102) having a trench (106) extending below the surface (110) CHARACTERIZED BY:

a trench fill material (108) disposed in the trench (106) and having a portion (109) extending above the surface (110);

a first conductive layer (116) above the substrate (102) and adjacent the trench fill material (108) and having a portion (118) extending over the portion (109) of the trench fill material (108);

an insulative material (122) above the first conductive layer (116); and

a second conductive layer (124) adjacent the insulative material (122), whereby the integrated circuit (100) has an improved gate coupling ratio.

2. The integrated circuit (100) of claim 1, wherein the trench fill material (108) includes first and second layers of oxide (308, 342).

3. The integrated circuit (100) of claim 1, wherein the first conductive material (116) includes first and second wings (118, 120) separated by the insulative material (122).

4. The integrated circuit (100) of claim 1, wherein the first conductive material (116) defines a via (140) fabricated by a patterning process comprising a masking step and an etching step.

5. The integrated circuit (100) of claim 1, wherein the portion (109) of the trench fill material (108) extends above the surface (110) of the substrate (102) at least 1000 Angstroms.

6. The integrated circuit (100) of claim 1, wherein the substrate (102) defines a corner (136, 138) where an upper surface (110) of the substrate (102) contacts the trench (106), wherein the corner (136, 138) is rounded.

7. The integrated circuit (100) of claim 1, wherein the first conductive layer (116), insulative material (122) and second conductive layer (124) form part of a flash EPROM transistor.

8. The integrated circuit (100) of claim 1, wherein the first and second conductive layers (116, 124) comprise polysilicon.



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9. An integrated circuit (100) having an increased gate coupling capacitance, the integrated circuit (100) fabricated by a process comprising forming a trench (106) in the substrate (102), the trench (106) extending below a surface (110) of the substrate (102) CHARACTERIZED BY:

providing a trench fill material (108) in the trench (106) such that the trench fill material (108) extends above the surface (110) of the substrate (102); and

providing a first conductive layer (116) over at least a portion of the trench fill material (108).

10. The integrated circuit (100) of claim 9, the process further comprising:
providing an insulative material (122) over the first conductive layer (116); and
providing a second conductive layer (124) over the insulative material (122).

11. The integrated circuit (100) of claim 9, wherein the step of providing a trench fill material (108) includes:

providing a trench fill oxide (108) over the trench (106);
applying a photoresist mask (131) above the trench (106); and
etching the trench fill oxide (108).

12. The integrated circuit (100) of claim 9, further comprising providing a nitride layer (230) over the substrate (102), the nitride layer (230) having a thickness of between 1000 and 5000 Angstroms, wherein the trench fill material (108) and nitride layer (230) are planarized.

13. The integrated circuit (100) of claim 9, further comprising patterning the first conductive layer (116) to form first and second conductive wings (118, 120) and providing an insulative material (122) to electrically isolate the first and second conductive wings (118, 120).

14. The integrated circuit (100) of claim 9, further comprising providing an insulative material (342) over the trench fill material (108) and patterning the insulative material (342) to fabricate a second trench fill material (346) above the trench (106), the first conductive layer (116) extending over at least a portion of the second trench fill material (346).



