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Abstract

A horizontal panning control circuit (1200) counts horizontal lines, or half lines, and generates a vertical reset signal (VRST) delayed by a variable pan delay (VPHASE) relative to the vertical synchronizing component (VSYNC) of the video signal. The pan delay varies in a first range for vertically panning the video signal down and varies in a second range for vertically panning the video signal up. The first range is less than the number of horizontal lines in each field and the second range is greater than the number of horizontal lines in each field and less than the number of horizontal lines in each frame. The mutually exclusive ranges control interline flicker of the panned video signal when successive fields have different numbers of horizontal lines.

FIGURE 9

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