HIGH-DENSITY FLIP-CHIP INTERCONNECT

Background of the Invention



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Technical Field of the Invention

The present invention relates generally to interconnect technology for routing signals through a multi-layer board, and is especially useful with flip-chip packaging.

Background Art

FIG. 1 illustrates, in cross-section, a motherboard coupled, such as by solder balls, to an interposer or other substrate, hereinafter referred to as a "card". The card is coupled, such as by solder bumps, to a chip such as a flip-chip die, and illustrates one exemplary embodiment of the layers of such, according to the prior art. In the illustrated example, the card has five layers of structural material (board layers A-F), and six layers of traces or interconnects (trace layers 3F, 2F, 1FC, 1BC, 2B, and 3B), while a simplified motherboard is shown having only one structural layer (motherboard) and one trace or interconnect layer (m/b trace layer). The reader will appreciate that this is by way of example only.

Typically, the uppermost one or two interconnect layers, such as trace layer 3F and trace layer 2F, are used for routing of large numbers of input/output (I/O) signals, memory signals, clocks, strobes, voltage references, and the like (hereinafter collectively referred to as "I/O signals" for simplicity in explanation and not by way of limitation), while the lower layers are used for providing power, ground, shielding, and the like. Signals are routed between trace layers using vias. Power and ground planes may suitably be routed or coupled between adjacent layers using drilled vias. However, drilled vias may often be too large to be suitable for use in routing signals between the upper layers. In that case, one option is to use micro-vias (μvias) which may be formed by etching or the like at a much smaller scale than drilling would permit.

Please continue to make reference to FIG. 1 throughout the remainder of this patent.

FIG. 2 illustrates, in top view, an exemplary routing of such signals according to the prior art. For ease in reading FIG. 2, the various layers of the motherboard and card are not shown, but the general outline of the flip-chip die is shown by the dotted box 10. A



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plurality of bumps 12 are distributed on the flip-chip die and/or the card in a pattern. Some of those bumps are for carrying I/O signals and some are for carrying power and ground signals. Typically, the I/O signals will be connected to other chips (not shown) on the motherboard; thus, it is desirable to route those signals using the generally outer bumps (such as those labeled 14 and 16) of the flip-chip die, and to use the generally inner bumps (such as those labeled 12) for power and ground.

In some high-density or high-signal-count applications, the I/O signal count and/or the I/O bump density may be such that it is difficult or impossible to route all of the I/O signals on the uppermost trace layer 3F. In such applications, some of the I/O signals are routed on the uppermost trace layer (such as 24 and others illustrated by solid lines extending from their respective bump to the "to circuitry" indication), while other I/O signals are routed from their respective bumps down through micro-vias (not shown) to a lower trace layer such as trace layer 2F, outward to a location where the design rules and physical dimensions permit, then back up through a micro-via (such as 18) to the uppermost trace layer, and from there to their destinations. The signals which are carried below the uppermost layer are illustrated by dashed lines such as 20, and after being micro-viad back to the top layer they are illustrated by solid lines such as 22.

However, the prior art has limited ability to route large numbers of signals in high-density applications, and other limitations.

Brief Description of the Drawings

The invention will be understood more fully from the detailed description given below and from the accompanying drawings of embodiments of the invention which, however, should not be taken to limit the invention to the specific embodiments described, but are for explanation and understanding only.

FIG. 1 shows, in cross-section, a flip-chip die, a substrate, and a motherboard, with exemplary layers shown, according to the prior art.

FIG. 2 shows an interconnect routing system according to the prior art.

FIG. 3 shows one embodiment of the interconnect routing system of this invention.

FIG. 4 shows spacing details of one embodiment of the invention.

FIG. 5 shows routing details of one embodiment of the invention, particularly showing the routing of signals between micro-vias in a trace layer beneath the uppermost trace layer.

FIG. 6 shows routing details of one embodiment of the invention, particularly showing the routing of signals in the uppermost layer and a lower layer.

FIG. 7 shows one embodiment of an arrangement of micro-vias according to this invention.

Detailed Description

FIG. 3 illustrates one exemplary embodiment of the interconnect system of this invention. As before, the dotted box indicates the location of the flip-chip die. There are a plurality of bumps 30 distributed within the area where the die and card (meaning substrate, interposer, or the like) connect. Various groups of the bumps may be distributed in one or more repeating patterns. An instance of a group of bumps that repeats may be termed a "spline". The term "spline" may also be used to refer to a group of traces, bumps, vias, or combination thereof corresponding to a spline of the die. The illustrated pattern includes seven bumps 30A-G which make up a spline (Spline 1), and that pattern repeats itself to form additional splines (Spline 2 through Spline N). For ease in reference, the bumps may be considered as being arranged in rows, with an outermost row (row A) being nearest the flip-chip die's edge, and one or more additional rows (such as row B through row G) each residing sequentially closer to the center or core of the flip-chip die. As illustrated, the splines may in some embodiments mirror image at some point on the chip. For example, Spline 1 and Spline N are mirror images of each other. In the embodiment shown, the splines mirror image and leave some non-spline bumps between them.

The card has one or more rows of micro-vias (such as 30H and 30I) arranged in one or more rows (such as row H and row I). These micro-vias are for returning I/O signals from a deep layer to a less deep layer. Typically, this will be from the next-to-uppermost layer (2F) to the uppermost layer (3F), but the skilled reader will appreciate that the principles of this invention are not necessarily limited to that application. For ease in explanation only, this patent will use the terms "top layer" and "buried layer".

One or more of the splines may have corresponding groups of the distant micro-vias. Each such group may be termed a "riser", such as Riser 1 through Riser N.

The top layer traces and buried layer traces are illustrated for two splines and their associated risers, for simplicity in illustration. The skilled reader will appreciate that any number of the splines may be coupled to their respective I/O signal destinations in this manner.

FIG. 4 illustrates one exemplary spacing of the bumps and micro-vias in a spline and its riser. The skilled reader will appreciate that this is only an example, and not necessarily a limitation on the invention. The reader will further appreciate that it is not necessarily required that, for example, the bumps be circular, nor that the bumps all be of the same size, nor that the micro-vias be of the same size as the bumps, and so forth.

In one embodiment, a bump (such as bump 30A(a)) has a width "w", and the bumps in a row are on 2w centers (such as bumps 30A(g) and 30A(h)). In one embodiment, the risers are located such that the on-center distance from the outermost row of bumps (row A) to the nearest row of riser micro-vias (row H) (which may be termed the "breakout length") is approximately 12w (such as from bump 30A(d) to micro-via 30H(d). The micro-vias within a given riser are located on approximately 1.5w centers (such as from micro-via 30H(d) to micro-via 30I(d)), while the risers are at roughly 3w spacing (such as from micro-via 30I(d) to micro-via 30I(e)). The skilled reader will appreciate that this is but one example, and that the sizes and spacings for any particular application will be dictated by such things as the available manufacturing technology, the number and type of I/O signals, the cross-coupling and noise requirements, impedance targets, and so forth.

FIG. 5 illustrates one exemplary embodiment of the micro-vias, signal traces, and ground plane on the buried layer. Bumps 40, 42, and 44 are actually at the top layer, but are shown here for reference of the spacing. Micro-vias 48 and 50 route I/O signals down from the bumps through the top layer to the buried layer. Traces 58 and 60 carry those signals to micro-vias 54 and 56, which route the signals back to the top layer. The reader will appreciate that the traces 58 and 60 do not connect to bumps 40 or 44, as those bumps are not present on the buried layer; they merely overlay the traces 58 and 60.

By providing more than one row of riser micro-vias, an increased number of breakout signals may be utilized.

In one embodiment, a row of bumps between the top layer traces' bumps (such as rows A-C) and the buried layer traces' bumps (such as rows E-F) is used for ground, power, or other reference. In one such embodiment, that row is used in conjunction with a ground plane 62. The ground plane includes a plurality of "fingers" (such as 62a-c) which extend inward past the risers to connect to the micro-vias 46, which connect to ground bumps on the die. The fingers 62a-c carry the return path current for their respective splines' and risers' signals. Because the fingers 62a-c, the buried signal traces 58 and 60, and the micro-vias 48, 50, 54, and 56, are on the same layer, they should be fabricated so as to not touch each other. The fingers provide a ground (or power) return path for the signals, and they provide a reference plane for the signals which are breaking out on the top layer.

FIG. 6 illustrates further details of the exemplary embodiment shown in FIG. 5. At the top layer, the signal from bump 42 is routed on trace 66, the signal from bump 44 is routed on trace 68, and the signal from bump 40 is routed on trace 70 to their respective destinations. Also at the top layer, the signals coming back up from micro-vias 54 and 56 are routed on trace segments 72 and 74, respectively. Thus, for example, a logic or chip (not shown) coupled to the trace 72 is ultimately connected to the flip-chip connector coinciding with the bump 48.

The skilled reader will appreciate that, in order to minimize cross-coupling and other undesirable effects, it is desirable to minimize the distance over which top layer signals directly overlay buried layer signals.

In one embodiment, a maximum breakout signal count may be achieved by routing three I/O signals on the top layer and two I/O signals on the buried layer. In other embodiments, in which the design rules dictate otherwise, other signal counts may prove better.

In one embodiment, a given spline's top layer I/O signals are routed adjacent one another, and that spline's buried layer I/O signals are brought up to the top layer and then routed adjacent to that spline's top layer I/O signals.

In one embodiment, the top layer I/O signals are routed on an outermost side of the spline's riser micro-vias. For example, in the view of FIG. 3, the top layer I/O signals for the splines on the left half of the flip-chip die (beginning with Spline 1) are routed on the

left side of their respective corresponding risers, while the top layer I/O signals for the splines on the right half (ending with Spline N) are routed on the right side of their respective corresponding risers.

It is not necessarily the case that all risers must be equally spaced, as the reader will appreciate. For example, the two centermost risers may in some embodiments be placed much closer together than other adjacent pairs, in those embodiments where those risers' respective traces are routed on the outer sides of those risers. In some embodiments, the spacing may be different for each adjacent pair, depending upon design rules, varying numbers of signal traces that must pass between adjacent pairs, and so forth.

In one embodiment, in which for a spline three I/O signals are routed on the top layer and are taken from the outermost three rows of bumps (rows A-C), the trace from the third row bump (row C) is routed between the first and second row bumps.

In one embodiment, in which for a spline three I/O signals are routed on the top layer and two I/O signals are routed on the buried layer, the buried layer signals are taken from the fifth and sixth rows of bumps. In one embodiment, those buried layer signals are routed directly beneath the spline's first and third row bumps. In one embodiment, the fourth row bump is for ground. In one embodiment (such as shown in FIG. 3 as row G), a row of bumps inside the buried layer signal rows' bumps may be used to provide power.

FIG. 7 illustrates one embodiment of a placement of the riser micro-vias, which provides the shortest path for the signals on the buried layer to surface to the top layer. In applications where it is necessary to space the risers wider than the spacing of the splines, by distributing the risers generally in an arc, the buried layer I/O trace segments may be made to have reduced variation in their respective lengths. In one embodiment, the respective micro-vias within a given riser may still be placed in substantially rectilinear arrangement with respect to the rectilinear alignment of the splines. In other words, in one embodiment, the micro-vias in a riser do not need to be aligned in a radial tangent to the arc along which the risers are distributed. This rectilinear alignment may lend itself to easier simulation and validation, for example.

While the invention has been described with reference to embodiments utilizing solder bumps, non-drilled micro-vias, and other specifics, the reader will appreciate that the invention has ready applicability in conjunction with other technologies and that these

points of discussion should not be interpreted as any sort of limitation on the scope of the invention. The term "connector" is used in the claims below to refer generically to any and all methodologies of connecting one element (such as a flip-chip or the like) to another element (such as a card or the like).

The invention has been described in terms of electrical signals and traces suitable for transmitting them, but has applicability in other technologies, such as optical interconnect, microwave transmission, and so forth. The card has been described in terms of a multi-layer board having sandwiched structural layers and trace layers, but the reader should understand that the invention has applicability in other technologies, such as those in which there is no structural stiffness required and thus no structural layers as such, or such as those in which interconnects are not referred to as "traces" per se, so long as there are multiple layers of transmission signal wires, lines, traces, fibers, or the like and the requirement of using multiple such layers in order to increase the signal breakout count or density. However, the term "trace" will be used in the claims to generically refer to any and all such means. These and other points of invention will be understood by the skilled reader upon thoughtful consideration of this patent.

Reference in to "upper" or "outermost" or "top" or "buried" or the like should not be interpreted as requiring any particular absolute orientation of the apparatus.

Reference to "breakout length" should not be interpreted as necessarily requiring that the riser micro-vias be beyond the physical edges of the flip-chip die, but only that they be beyond the bump area of the flip-chip die in their vicinity.

Reference to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments, of the invention. The various appearances "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments.

If the specification states a component, feature, structure, or characteristic "may", "might", or "could" be included, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the element. If the specification or

claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

Those skilled in the art having the benefit of this disclosure will appreciate that many other variations from the foregoing description and drawings may be made within the scope of the present invention. Indeed, the invention is not limited to the details described above. Rather, it is the following claims including any amendments thereto that define the scope of the invention.

CLAIMS

What is claimed is:

1. An apparatus comprising:

(A) a first interconnect layer including at least one spline, each spline including,

(1) a plurality of first signal connectors,

(2) a plurality of first signal traces each coupled to a respective one of the plurality of first signal connectors,

(3) a plurality of second signal connectors, and

(4) a plurality of riser signal connectors spaced farther from the first and second signal connectors than a spacing between adjacent ones of the first and second signal connectors; and

(B) a second interconnect layer including, for each spline of the at least one spline,

(1) a plurality of second signal traces each coupled to a respective one of the plurality of second signal connectors and to a respective one of the plurality of riser connectors.

2. The apparatus of claim 1 wherein, in each spline:

the plurality of first signal connectors comprises three first signal connectors.

3. The apparatus of claim 1 wherein:

the first interconnect layer further includes, for each spline,

(5) a ground connector; and

the second interconnect layer further includes, for each spline,

(2) a ground finger coupled to the ground connector.

4. The apparatus of claim 1 wherein, in each spline:

the first and second signal connectors have a rectilinear orientation; and

the plurality of riser signal connectors are in substantially rectilinear orientation with the first and second signal connectors.

5. The apparatus of claim 1 wherein:

the first interconnect layer includes a plurality of splines; and

the pluralities of riser signal connectors of the plurality of splines are arranged in a substantially arced formation about an outermost edge of the splines.

6. The apparatus of claim 5 wherein:

corresponding ones of the respective pluralities of second signal traces of the plurality of splines have substantially equal lengths.

7. An apparatus comprising:

a core plurality of first signal connectors in a pattern having a substantially rectangular overall shape; and

a plurality of riser signal connectors in a pattern having a substantially arced overall shape and distributed about a side of the first signal connectors' rectangular overall shape at a distance from the core which is greater than a distance between adjacent ones of the first signal connectors.

8. The apparatus of claim 7 wherein:

respective ones of the riser signal connectors are coupled to respective ones of the first signal connectors; and

the arc of the shape of the pattern of the riser signal connectors has a curvature such that the distance from any given one of the riser signal connectors to its coupled first signal connector is substantially equal.

9. The apparatus of claim 8 wherein:

the plurality of first signal connectors comprises a plurality of splines; and

the plurality of riser signal connectors comprises a plurality of risers.

10. The apparatus of claim 9 wherein:

adjacent splines are separated by a first distance; and

adjacent risers are separated by a second distance greater than the first distance.

11. The apparatus of claim 10 wherein:

each spline comprises three first signal connectors and two second signal connectors; and

each riser comprises two riser signal connectors.

12. A multi-layer card comprising:

a first structural layer;

a first signal layer overlying the first structural layer and including a plurality of splines, each spline including,

at least two first signal connectors,

at least two first signal traces, each coupled to a corresponding respective first signal connector,

at least one second signal connector,

at least one riser signal connector, and

at least one riser signal trace, each coupled to a corresponding respective riser signal connector; and

a second signal layer underlying the first structural layer and including, for each of the splines,

at least one second signal trace coupled to a respective second signal connector and to a corresponding respective riser signal connector.

13. The apparatus of claim 12 wherein, in each spline:

the at least two first signal connectors comprise three first signal connectors;

the at least two first signal traces comprise three first signal traces;

the at least one second signal connector comprises two second signal connectors;

the at least one riser signal connector comprises two riser signal connectors;

the at least one riser signal trace comprises two riser signal traces; and

the at least one second signal trace comprises two second signal traces.

14. The apparatus of claim 13 wherein:

the three first signal traces are routed on a same side of the two riser signal connectors.

15. The apparatus of claim 14 wherein:

a middle one of the three first signal traces is coupled to a one of the three first signal connectors which is most distant from the two riser signal connectors.

16. The apparatus of claim 15 wherein:

a one of the riser signal traces which is coupled to a one of the riser signal connectors which is most distant from the second signal connectors is coupled to a one of the second signal connectors which is closest to the first signal connectors.

17. An apparatus comprising:

a structural layer;

an uppermost trace layer overlying the structural layer; and

a buried trace layer underlying the structural layer and including,

a plurality of splines each including at least one signal trace, and

a plurality of ground fingers each extending between and substantially the length of two respective adjacent splines.

18. The apparatus of claim 17 wherein the structural layer includes:

a first plurality of micro-vias each in contact with one of the signal traces; and

a second plurality of micro-vias each in contact with one of the ground fingers.

19. The apparatus of claim 18 wherein the uppermost trace layer includes:

a plurality of splines, corresponding to the plurality of splines of the buried trace layer, and each including a plurality of signal traces.

20. The apparatus of claim 19 further comprising:

a plurality of bumps including an outermost row of bumps; and

the plurality of splines of the uppermost trace layer are disposed between respective adjacent bumps in the outermost row.

21. The apparatus of claim 20 wherein:

the splines of the buried trace layer are disposed substantially beneath respective bumps in the outermost row.

22. A packaged semiconductor device comprising:

a flip-chip die having a plurality of connectors arranged in a substantially rectilinear pattern of a plurality of splines, wherein each spline includes,

a first plurality of M I/O connectors arranged in M rows of the pattern;

a second plurality of N I/O connectors arranged in N rows of the pattern, and

a card coupled to the flip-chip die and including,

a first trace layer having a plurality of groups of I/O traces, each group having

M I/O traces each coupled to a respective one of the M I/O connectors and arranged in groups corresponding to respective splines,

a second trace layer having a plurality of groups of I/O traces, each group having

N I/O traces each coupled to a respective one of the first plurality of N I/O connectors and arranged in groups corresponding to respective splines, and

M I/O traces; and

a structural layer between the first and second trace layers and including,

a first plurality of micro-vias each coupling a respective one of the M I/O connectors to a corresponding one of the M I/O traces of the first trace layer, and

a second plurality of micro-vias each coupling a respective one of the M I/O traces of the first trace layer to a respective one of the M I/O traces of the second trace layer.

23. The packaged semiconductor device of claim 22 wherein the M and N I/O connectors comprise:

bumps.

24. The packaged semiconductor device of claim 22 wherein the second trace layer comprises:

an uppermost trace layer.

25. The packaged semiconductor device of claim 24 wherein:

the N rows are outermost rows of the pattern.

26. The packaged semiconductor device of claim 22 wherein the first trace layer further comprises:

a plurality of ground plane fingers each extending between adjacent groups of M I/O traces.

27. The packaged semiconductor device of claim 26 wherein:

the plurality of ground plane fingers each extends substantially an entire length of the M I/O traces.

28. The packaged semiconductor device of claim 22 wherein:

the second plurality of micro-vias is distributed in a substantially arced pattern.

29. The packaged semiconductor device of claim 28 wherein:

the M and N I/O connectors are arranged in a substantially rectilinear pattern.

30. The packaged semiconductor device of claim 29 wherein:

a set of the second plurality of micro-vias corresponding to a set of the M and N I/O connectors along one side of the rectilinear pattern are distributed in an arc having a width greater than a width of the one side of the rectilinear pattern.

31. The packaged semiconductor device of claim 30 wherein:

the N I/O traces of each spline are disposed between that spline's second micro-vias and those of an adjacent spline.

32. A method of fabricating a package for a semiconductor device having a plurality of chip connectors disposed in a plurality of rows and having a repeated pattern of splines, wherein each spline of a plurality of the splines includes $N \geq 2$ first I/O signal connectors disposed in N of the rows and $M \geq 1$ second I/O signal connectors disposed in M of the rows, wherein the N rows are outside the M rows, the method comprising:

forming in a first layer of the package, for each spline, M second signal traces, the splines' second signal traces having a spacing substantially coinciding with a spacing of the splines' respective second I/O signal connectors;

forming in a second layer of the package overlying the first layer, for each second signal trace of each spline, a first via and a second via through the second layer and coupled to the second signal trace, the first vias having a spacing substantially coinciding with a spacing of the splines' respective second I/O signal connectors; and

forming in a third layer of the package overlying the second layer, for each spline, N first signal traces, the splines' first signal traces having a spacing substantially coinciding with a spacing of the splines' respective first I/O signal connectors;

wherein the second vias and the first signal traces extend beyond a perimeter of the semiconductor device.

33. The method of claim 32 further comprising:

forming in the third layer, for each spline, M first signal traces each coupled to a respective one of the spline's second vias.

34. The method of claim 32 wherein:

the first and second vias comprise micro-vias.

35. The method of claim 32 wherein, for each spline, the forming N first signal traces further comprises:

routing the N first signal traces on an outer side of the spline's M second vias.

36. The method of claim 32 wherein, for each spline, the forming M second signal traces in the first layer further comprises:

routing the M second signal traces substantially beneath the first signal connectors.

37. The method of claim 32 wherein:

the forming the second vias of the respective splines comprises disposing the second vias in a substantially arced pattern; and

the forming M second signal traces of the respective splines comprises forming the respective splines' M second signal traces with a substantially equal length.

38. The method of claim 37 wherein $M \geq 2$ and wherein the method further comprises, for each spline:

the forming the second vias comprises disposing the second vias in M rows.

39. The method of claim 38 wherein the semiconductor device's connectors are disposed in a substantially rectilinear pattern, the method further comprising, for each spline:

the forming the second vias further comprises forming the second vias in substantial alignment with the rectilinear pattern.

40. The method of claim 32 wherein N=3 and wherein, for each spline:

the forming the N first signal traces further comprises routing a middle of the first signal traces to couple to a one of the N first signal connectors that is in an innermost of the N rows.

41. The method of claim 32 wherein the semiconductor device further has at least one ground connector disposed in a ground row which is inside the N rows, the method further comprising:

forming in the first layer of the package, a plurality of ground plane fingers each extending between a respective pair of adjacent splines; and

forming in the second layer of the package, for each of the ground plane fingers, a via coupled to the ground plane finger and positioned to couple to the ground connector.

5