

## DESCRIPTION

### **Title of Invention:**

5 LAMINATED FILM, SEMICONDUCTOR CHIP WITH BONDING  
LAYER, METHOD FOR MANUFACTURING LAMINATED FILM,  
METHOD FOR MANUFACTURING SEMICONDUCTOR CHIP  
WITH BONDING LAYER, AND METHOD FOR  
MANUFACTURING SEMICONDUCTOR DEVICE

### **Technical Field**

10 [0001] The present disclosure relates to a laminated film, a  
semiconductor chip with a bonding layer, a method for manufacturing a  
laminated film, a method for manufacturing a semiconductor chip with  
a bonding layer, and a method for manufacturing a semiconductor device.

### **Background Art**

15 [0002] In recent years, stacked MCPs (Multi Chip Packages) having  
increased capacity by semiconductor chips stacked in multiple stages  
have become widespread. Examples of the stacked MCPs include chip-  
embedded semiconductor packages. The structure of a semiconductor  
package in which a semiconductor chip is embedded by an adhesive film  
20 is referred to as film over die (FOD). Examples of the semiconductor  
package employing FOD include a structure in which a controller chip  
arranged on one surface of a substrate is embedded between the substrate  
and a memory chip by an embedding portion using an adhesive film (see,  
for example, Patent Literature 1).

### 25 **Citation List**

#### **Patent Literature**

[0003] Patent Literature 1: Japanese Unexamined Patent Publication No. 2014-175459

## **Summary of Invention**

### **Technical Problem**

5 [0004] In manufacturing the semiconductor package having the FOD structure, the semiconductor chip is required to be sufficiently embedded by the embedding portion using the adhesive film (embedding property). Regarding the embedding property, achieving both suppression of bleed and suppression of voids is important. Bleed is a phenomenon in which  
10 the embedding portion extends out from between the substrate and the memory chip, and the void is a phenomenon in which a gap is generated in the embedding portion between the substrate and the memory chip. Suppression of bleed and suppression of voids are in a trade-off relationship due to the volume of the embedding portion and the like,  
15 and a technology that favorably achieves both suppression of bleed and suppression of voids has been desired.

[0005] The present disclosure has been made to solve the above problem, and an object of the present disclosure is to provide a laminated film, a semiconductor chip with a bonding layer, a method for manufacturing a  
20 laminated film, a method for manufacturing a semiconductor chip with a bonding layer, and a method for manufacturing a semiconductor device, each favorably achieving both suppression of bleed and suppression of voids in manufacturing a semiconductor package.

### **Solution to Problem**

25 [0006] The gist of the present disclosure is as follows.

[0007] [1] A laminated film including an elongated base material film

and label portions provided on one surface of the base material film at predetermined intervals in an extending direction of the base material film, in which the label portions have a bonding layer overlapping the base material film, a pressure-sensitive adhesive layer overlapping the bonding layer, and a base material layer overlapping the pressure-sensitive adhesive layer, a flow control portion is provided on a surface of the bonding layer facing the pressure-sensitive adhesive layer, and the flow control portion imparts anisotropy to fluidity of the bonding layer during thermocompression bonding.

[0008] In the laminated film, the flow control portion is provided on the surface of the bonding layer facing the pressure-sensitive adhesive layer, and fluidity of the bonding layer during thermocompression bonding has anisotropy. Therefore, when the bonding layer is used as an embedding portion for a semiconductor chip, suppression of bleed is achieved by, for example, sufficiently securing the volume of the embedding portion between the substrate and the memory chip to suppress voids while aligning a direction in which the bonding layer readily flows with a long-side direction of a planar shape of the memory chip. Therefore, the laminated film favorably achieves both suppression of bleed and suppression of voids in manufacturing a semiconductor package.

[0009] [2] The laminated film according to [1], in which the flow control portion is constituted by a recess extending in one in-plane direction of the facing surface. According to such a configuration, the recess appropriately reduces a part of the volume of the bonding layer. In addition, during thermocompression bonding of the bonding layer, flow of the bonding layer in an extending direction of the recess is promoted.

Therefore, both suppression of bleed and suppression of voids are more favorably achieved.

5 [0010] [3] The laminated film according to [1], in which the flow control portion is constituted by a modified portion extending in one in-plane direction of the facing surface. According to such a configuration, during thermocompression bonding of the bonding layer, flow of the bonding layer in an extending direction of the modified portion is promoted. Therefore, both suppression of bleed and suppression of voids are more favorably achieved.

10 [0011] [4] The laminated film according to [1], in which the flow control portion is constituted by a roughened portion extending in one in-plane direction of the facing surface. According to such a configuration, during thermocompression bonding of the bonding layer, flow of the bonding layer in an extending direction of the roughened portion is promoted. Therefore, both suppression of bleed and suppression of voids are more favorably achieved.

15 [0012] [5] The laminated film according to any one of [1] to [4], in which, in the label portions, the pressure-sensitive adhesive layer and the base material layer have a projecting portion projecting outward beyond an edge of the bonding layer, and the projecting portion overlaps one surface of the base material film. According to such a configuration, attachment of the pressure-sensitive adhesive layer and the base material layer to an object such as a semiconductor wafer is facilitated. In addition, because the bonding layer is covered with the pressure-sensitive adhesive layer and the base material layer, the flow control portion is protected.

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[0013] [6] A semiconductor chip with a bonding layer including a semiconductor chip and a bonding layer provided on one surface side of the semiconductor chip, in which a flow control portion is provided on an opposite surface of the bonding layer opposite from the semiconductor chip, the flow control portion imparts anisotropy to fluidity of the bonding layer during thermocompression bonding.

[0014] In the semiconductor chip with a bonding layer, the flow control portion is provided on the opposite surface of the bonding layer opposite from the semiconductor chip, and fluidity of the bonding layer during thermocompression bonding has anisotropy. Therefore, when the bonding layer is used as an embedding portion for a semiconductor chip, suppression of bleed is achieved by, for example, sufficiently securing the volume of the embedding portion between the substrate and the memory chip to suppress voids while aligning the direction in which the bonding layer readily flows with the long-side direction of the planar shape of the memory chip. Therefore, the semiconductor chip with a bonding layer favorably achieves both suppression of bleed and suppression of voids in manufacturing a semiconductor package.

[0015] [7] The semiconductor chip with a bonding layer according to [6], in which the flow control portion is constituted by a recess extending in one in-plane direction of the opposite surface. According to such a configuration, the recess appropriately reduces a part of the volume of the bonding layer. In addition, during thermocompression bonding of the bonding layer, flow of the bonding layer in the extending direction of the recess is promoted. Therefore, both suppression of bleed and suppression of voids are more favorably achieved.

[0016] [8] The semiconductor chip with a bonding layer according to [6], in which the flow control portion is constituted by a roughened portion extending in one in-plane direction of the opposite surface. According to such a configuration, during thermocompression bonding of the bonding layer, flow of the bonding layer in the extending direction of the roughened portion is promoted. Therefore, both suppression of bleed and suppression of voids are more favorably achieved.

[0017] [9] A method for manufacturing a laminated film including a preparation step of preparing an elongated base material film overlapping a bonding layer, a formation step of forming, on one surface of the bonding layer, a flow control portion imparting anisotropy to fluidity of the bonding layer during thermocompression bonding, and a lamination step of laminating a pressure-sensitive adhesive layer and a base material layer on the bonding layer such that the one surface of the bonding layer becomes a facing surface of the pressure-sensitive adhesive layer.

[0018] In the method for manufacturing a laminated film, the flow control portion is provided on the surface of the bonding layer facing the pressure-sensitive adhesive layer, thereby imparting anisotropy to fluidity of the bonding layer during thermocompression bonding. Therefore, when the bonding layer is used as an embedding portion for a semiconductor chip, suppression of bleed is achieved by, for example, sufficiently securing the volume of the embedding portion between the substrate and the memory chip to suppress voids while aligning the direction in which the bonding layer readily flows with the long-side direction of the planar shape of the memory chip. Use of the laminated

film obtained by the manufacturing method favorably achieves both suppression of bleed and suppression of voids in manufacturing a semiconductor package.

5 [0019] [10] The method for manufacturing a laminated film according to [9], in which, in the formation step, a recess extending in one in-plane direction of the one surface is formed as the flow control portion by pressing a bar coater against the one surface while heating the bonding layer. According to such a method, the recess extending in one in-plane direction is accurately formed on the surface to serve as the facing surface. By accurately forming the recess in accordance with the planar shape of the semiconductor chip and the like, both suppression of bleed and suppression of voids are more favorably achieved in manufacturing a semiconductor package.

15 [0020] [11] The method for manufacturing a laminated film according to [9], in which, in the formation step, a recess extending in one in-plane direction of the one surface is formed as the flow control portion by partially cutting the bonding layer by irradiation with laser light. According to such a method, the recess extending in one in-plane direction is accurately formed on the surface to serve as the facing surface. By accurately forming the recess in accordance with the planar shape of the semiconductor chip and the like, both suppression of bleed and suppression of voids are more favorably achieved in manufacturing a semiconductor package.

20 [0021] [12] The method for manufacturing a laminated film according to [9], in which, in the formation step, a modified portion extending in one in-plane direction of the one surface is formed as the flow control

portion by partially curing the bonding layer by light irradiation using a mask having a predetermined pattern. According to such a method, a modified portion extending in one in-plane direction is accurately formed on the surface to serve as the facing surface. By accurately forming the modified portion in accordance with the planar shape of the semiconductor chip and the like, both suppression of bleed and suppression of voids are more favorably achieved in manufacturing a semiconductor package.

[0022] [13] The method for manufacturing a laminated film according to [9], in which, in the formation step, a roughened portion extending in one in-plane direction of the one surface is formed as the flow control portion by partially modifying the bonding layer by irradiation with laser light. According to such a method, the roughened portion extending in one in-plane direction is accurately formed on the surface to serve as the facing surface. By accurately forming the roughened portion in accordance with the planar shape of the semiconductor chip and the like, both suppression of bleed and suppression of voids are more favorably achieved in manufacturing a semiconductor package.

[0023] [14] The method for manufacturing a laminated film according to any one of [9] to [13], in which, in the lamination step, the pressure-sensitive adhesive layer and the base material layer are precut such that a projecting portion projecting outward beyond an edge of the bonding layer is formed, and the projecting portion is overlaid on one surface of the base material film. According to such a configuration, in the manufactured laminated film, attachment of the pressure-sensitive adhesive layer and the base material layer to an object such as a

semiconductor wafer is facilitated. In addition, because the bonding layer is covered with the pressure-sensitive adhesive layer and the base material layer, the flow control portion is protected.

5 [0024] [15] A method for manufacturing a semiconductor chip with a bonding layer including a preparation step of preparing a semiconductor chip with a bonding layer including a semiconductor chip and a bonding layer provided on one surface side of the semiconductor chip, and a formation step of forming, on an opposite surface of the bonding layer opposite from the semiconductor chip, a flow control portion imparting anisotropy to fluidity of the bonding layer during thermocompression bonding.

10 [0025] In the method for manufacturing a semiconductor chip with a bonding layer, the flow control portion is provided on the opposite surface of the bonding layer opposite from the semiconductor chip, thereby imparting anisotropy to fluidity of the bonding layer during thermocompression bonding. Therefore, when the bonding layer is used as an embedding portion for a semiconductor chip, suppression of bleed is achieved by, for example, sufficiently securing the volume of the embedding portion between the substrate and the memory chip to suppress voids while aligning the direction in which the bonding layer readily flows with the long-side direction of the planar shape of the memory chip. Use of the semiconductor chip with a bonding layer obtained by the manufacturing method favorably achieves both suppression of bleed and suppression of voids in manufacturing a semiconductor package.

25 [0026] [16] The method for manufacturing a semiconductor chip with a

bonding layer according to [15], in which, in the formation step, a recess extending in one in-plane direction of the opposite surface is formed as the flow control portion by cutting the opposite surface by irradiation with laser light. According to such a method, the recess extending in one in-plane direction is accurately formed on the opposite surface. By accurately forming the recess in accordance with the planar shape of the semiconductor chip and the like, both suppression of bleed and suppression of voids are more favorably achieved in manufacturing a semiconductor package.

[0027] [17] The method for manufacturing a semiconductor chip with a bonding layer according to [15], in which, in the formation step, a roughened portion extending in one in-plane direction of the opposite surface is formed as the flow control portion by partially modifying the bonding layer by irradiation of the opposite surface with laser light. According to such a method, the roughened portion extending in one in-plane direction is accurately formed on the opposite surface. By accurately forming the roughened portion in accordance with the planar shape of the semiconductor chip and the like, both suppression of bleed and suppression of voids are more favorably achieved in manufacturing a semiconductor package.

[0028] [18] A method for manufacturing a semiconductor device including preparing the semiconductor chip with a bonding layer according to any one of [6] to [8] and a substrate on which a semiconductor chip is mounted, thermocompression-bonding the semiconductor chip with a bonding layer to the substrate such that the bonding layer faces the substrate, and forming an embedding portion

between the semiconductor chip of the semiconductor chip with a bonding layer and the substrate.

[0029] In the method for manufacturing a semiconductor device, use of the semiconductor chip with a bonding layer described above causes fluidity of the bonding layer during thermocompression bonding to have anisotropy. Therefore, when the bonding layer is used as an embedding portion for a semiconductor chip, suppression of bleed is achieved by, for example, sufficiently securing the volume of the embedding portion between the substrate and the memory chip to suppress voids while aligning the direction in which the bonding layer readily flows with the long-side direction of the planar shape of the memory chip. Therefore, the method for manufacturing a semiconductor device favorably achieves both suppression of bleed and suppression of voids.

#### **Advantageous Effects of Invention**

[0030] According to the present disclosure, both suppression of bleed and suppression of voids are favorably achieved.

#### **Brief Description of Drawings**

[0031] FIG. 1 is a schematic sectional view illustrating an example of a semiconductor package.

FIG. 2 is a schematic plan view illustrating an example of a laminated film.

FIG. 3 is a sectional view taken along line III-III in FIG. 2.

FIG. 4(a) is a schematic sectional view illustrating an attachment step, FIG. 4(b) is a schematic sectional view illustrating a dicing step, and FIG. 4(c) is a schematic sectional view illustrating an irradiation step.

FIG. 5(a) is a schematic sectional view illustrating a pickup step,

and FIG. 5(b) is a schematic sectional view illustrating a die attach step.

FIG. 6(a) is a schematic sectional view illustrating bleed, and FIG. 6(b) is a schematic sectional view illustrating a void.

FIG. 7 is a schematic plan view illustrating a main part of a laminated film having a flow control portion.

FIG. 8 is a schematic plan view illustrating an action of the flow control portion.

FIG. 9(a) and FIG. 9(b) are schematic sectional views illustrating recesses that are examples of the flow control portion.

FIG. 10(a) is a schematic view illustrating an example of a wireless bar used for forming the recess illustrated in FIG. 9(a), and FIG. 10(b) is a schematic view illustrating parameters of a groove portion.

FIG. 11(a) is a schematic view illustrating an example of a wire bar used for forming the recess illustrated in FIG. 9(b), and FIG. 11(b) is a schematic view illustrating parameters of the wire.

FIG. 12 is a schematic sectional view illustrating a manner of forming the recess of FIG. 9(b).

FIG. 13(a) is a schematic sectional view illustrating a modified portion that is an example of the flow control portion, and FIG. 13(b) is a schematic sectional view illustrating a manner of forming the modified portion.

FIG. 14(a) is a schematic sectional view illustrating a roughened portion that is an example of the flow control portion, and FIG. 14(b) is a schematic sectional view illustrating a manner of forming the roughened portion.

FIG. 15 is a flowchart illustrating an example of a method for

manufacturing a laminated film having a flow control portion.

FIG. 16(a) is a schematic sectional view illustrating a semiconductor chip with a bonding layer having a recess that is an example of the flow control portion, and FIG. 16(b) is a schematic sectional view illustrating a manner of forming the recess.

FIG. 17(a) is a schematic sectional view illustrating a semiconductor chip with a bonding layer having a roughened portion that is an example of the flow control portion, and FIG. 17(b) is a schematic sectional view illustrating a manner of forming the roughened portion.

FIG. 18 is a flowchart illustrating an example of a method for manufacturing a semiconductor chip with a bonding layer having a flow control portion.

### **Description of Embodiments**

[0032] Hereinafter, preferred embodiments of a laminated film, a semiconductor chip with a bonding layer, a method for manufacturing a laminated film, a method for manufacturing a semiconductor chip with a bonding layer, and a method for manufacturing a semiconductor device according to one aspect of the present disclosure will be described in detail with reference to the drawings.

[0033] In the following description, constituent elements, including steps and the like, are not essential unless specifically stated. The sizes of constituent elements in the drawings are conceptual, and the relative size relationships among the constituent elements are not limited to the relationships illustrated in the drawings. Exemplified numerical values and ranges thereof also do not limit the present disclosure.

[0034] In the following description, a numerical range indicated using "to" indicates a range including the numerical values stated before and after "to" as a minimum value and a maximum value, respectively. In addition, in numerical ranges stated stepwise, an upper limit value or a lower limit value stated in one numerical range may be replaced with an upper limit value or a lower limit value of another numerical range stated stepwise. An upper limit value or a lower limit value of a numerical range may be replaced with a value shown in Examples.

[0035] FIG. 1 is a schematic sectional view illustrating an example of a semiconductor package. Here, a semiconductor device such as a NAND-type flash memory is exemplified as a semiconductor package (semiconductor device) 1. As illustrated in FIG. 1, the semiconductor package 1 includes a substrate 2, a first semiconductor chip (semiconductor chip) 3, a second semiconductor chip (semiconductor chip) 4, an embedding portion 5, and a sealing portion 6. The substrate 2 is, for example, an organic substrate. The substrate 2 may be a metal substrate such as a lead frame. Predetermined circuit patterns 7 and 8 are formed on one surface of the substrate 2.

[0036] The first semiconductor chip 3 is, for example, a controller chip. The first semiconductor chip 3 is electrically connected to the circuit pattern 7 via a bonding layer 9. The first semiconductor chip 3 is electrically connected to the circuit pattern 8 via a first wire 10. The second semiconductor chip 4 is, for example, a memory chip. The second semiconductor chip 4 is arranged on the one-surface side of the substrate 2 with a predetermined interval from the first semiconductor chip 3. The second semiconductor chip 4 is electrically connected to the

circuit pattern 8 via a second wire 11.

[0037] The embedding portion 5 formed by a bonding layer 24 of a laminated film 21 to be described later is provided between the second semiconductor chip 4 and the substrate 2. The first semiconductor chip 3, the circuit pattern 7, and the first wire 10 are each embedded by the embedding portion 5 between the second semiconductor chip 4 and the substrate 2. The first semiconductor chip 3, the second semiconductor chip 4, the first wire 10, and the second wire 11 are sealed on the one-surface side of the substrate 2 by the sealing portion 6 forming an outer periphery relative to the embedding portion 5.

[0038] FIG. 2 is a schematic plan view illustrating an example of a laminated film. In addition, FIG. 3 is a sectional view taken along line III-III of FIG. 2. The laminated film 21 illustrated in FIGS. 2 and 3 is an elongated film used in the manufacturing process of the semiconductor package 1 described above for fixing a semiconductor wafer in a dicing step, forming the embedding portion 5 in a die attach step, and the like. The laminated film 21 is generally stored in a state of being wound in roll form and is fed out from a roll in accordance with a required amount during use.

[0039] As illustrated in FIGS. 2 and 3, the laminated film 21 has an elongated base material film 22 and label portions 23 provided on one surface of the base material film 22 at predetermined intervals in an extending direction of the base material film 22. The label portion 23 is constituted by a bonding layer 24 overlapping the base material film 22, a pressure-sensitive adhesive layer 25 overlapping the bonding layer 24, and a base material layer 27 overlapping the pressure-sensitive adhesive

layer 25. In plan view, the label portion 23 has, for example, a circular shape.

[0040] The base material film 22 is, for example, a resin film. Examples of the resin material constituting the base material film 22 include polytetrafluoroethylene, polyethylene, polypropylene, polymethylpentene, polyethylene terephthalate, and polyimide. The thickness of the base material film 22 may be, for example, 60  $\mu\text{m}$  to 200  $\mu\text{m}$ , and may be 70  $\mu\text{m}$  to 170  $\mu\text{m}$ . A release treatment using silicone or the like may be performed on a surface of the base material film 22.

[0041] The bonding layer 24 is, for example, a film-shaped portion referred to as a die attach film. Examples of a constituent material of the bonding layer 24 include an electrically insulating thermosetting resin. Examples of the thermosetting resin include an epoxy resin, a bismaleimide resin, a triazine resin, a polyimide resin, a polyamide resin, a cyanoacrylate resin, a phenol resin, an unsaturated polyester resin, a melamine resin, a urea resin, a polyurethane resin, a polyisocyanate resin, a furan resin, a resorcinol resin, a xylene resin, a benzoguanamine resin, a diallyl phthalate resin, a silicone resin, a polyvinyl butyral resin, a siloxane-modified epoxy resin, a siloxane-modified polyamide-imide resin, and an acrylate resin. These materials may be used alone or as a mixture of two or more kinds. The bonding layer 24 may contain acrylic rubber.

[0042] The pressure-sensitive adhesive layer 25 and the base material layer 27 are, for example, film-shaped portions referred to as a dicing tape. The pressure-sensitive adhesive layer 25 may be either a single layer or multiple layers. The pressure-sensitive adhesive layer 25

preferably has tackiness at room temperature and has necessary adhesion to an adherend. The pressure-sensitive adhesive layer 25 preferably has a characteristic of curing, with a decrease in tackiness, by high-energy rays such as radiation or by heat. More preferably, the pressure-sensitive adhesive layer 25 is easily peelable from the base material film 22 and the bonding layer 24 even without application of high-energy rays such as radiation or heat. The pressure-sensitive adhesive layer 25 may be a pressure-sensitive type pressure-sensitive adhesive layer. The pressure-sensitive adhesive layer 25 may be formed using, for example, an acrylic resin, various synthetic rubbers, natural rubber, or a polyimide resin. The base material layer 27 is made of, for example, a resin such as polyolefin, polypropylene, or ionomer. The thickness of the pressure-sensitive adhesive layer 25 including the base material layer 27 may be, for example, 10  $\mu\text{m}$  to 200  $\mu\text{m}$ , and may be 20  $\mu\text{m}$  to 150  $\mu\text{m}$ .

[0043] In the present embodiment, as illustrated in FIGS. 2 and 3, in the label portion 23, the pressure-sensitive adhesive layer 25 and the base material layer 27 have an annular projecting portion P projecting outward beyond an edge of the bonding layer 24. The projecting portion P overlaps one surface of the base material film 22. As a result, the bonding layer 24 on the one surface of the base material film 22 is in a state of being covered with the pressure-sensitive adhesive layers 25 and 27.

[0044] In the present embodiment, protective portions 26 and 26 are provided so as to surround the periphery of the label portion 23. Each protective portion 26 is a portion that protects the label portion 23 from pressure when the laminated film 21 is wound into a roll. The protective

portions 26 are arranged symmetrically in a width direction at both edge portions in a width direction of the one surface of the base material film 22 and extend in an extending direction of the base material film 22. In the present embodiment, the protective portions 26 are constituted by the pressure-sensitive adhesive layer 25 and the base material layer 27. The label portion 23 and the protective portions 26 are formed by laminating the pressure-sensitive adhesive layer 25 and the base material layer 27 so as to cover the bonding layer 24 on the one surface of the base material film 22, thereafter precutting the pressure-sensitive adhesive layer 25 and the base material layer 27 in a predetermined pattern, and peeling unnecessary portions from the one surface of the base material film 22. [0045] Next, a method for manufacturing the semiconductor package 1 using the laminated film 21 described above will be described. [0046] The method for manufacturing the semiconductor package 1 of the present embodiment includes an attachment step, a dicing step, an irradiation step, a pickup step, and a die attach step. The attachment step is a step of attaching the pressure-sensitive adhesive layer 25 and the base material layer 27 together with the bonding layer 24 to a semiconductor wafer W. In the attachment step, as illustrated in FIG. 4(a), after the label portion 23 is attached to one surface of the semiconductor wafer W such that the bonding layer 24 faces the semiconductor wafer W side, the base material film 22 is peeled from the label portion 23. In the attachment step, a peripheral edge portion of the pressure-sensitive adhesive layer 25 is fixed to a ring frame not illustrated, and the semiconductor wafer W is supported inside the ring frame.

[0047] The dicing step is a step of dicing the semiconductor wafer W to form semiconductor chips 31 with a bonding layer. In the dicing step, using cutting means such as a blade or laser light, the semiconductor wafer W is cut together with the bonding layer 24 in a predetermined pattern, for example, a lattice pattern, as illustrated in FIG. 4(b). As a result, multiple semiconductor chips 31 with a bonding layer are formed on the pressure-sensitive adhesive layer 25. A chip portion 32 in each semiconductor chip 31 with a bonding layer becomes the second semiconductor chip 4 described above in the manufactured semiconductor package 1. In cutting the semiconductor wafer W and the bonding layer 24, by making a cutting line reach the pressure-sensitive adhesive layer 25, adjacent semiconductor chips 31 and 31 with a bonding layer are more reliably separated from each other.

[0048] The irradiation step is a step of irradiating light onto the pressure-sensitive adhesive layer 25 to cure the pressure-sensitive adhesive layer 25. In the irradiation step, as illustrated in FIG. 4(c), ultraviolet light V is irradiated onto the pressure-sensitive adhesive layer 25 to reduce tackiness of the pressure-sensitive adhesive layer 25. The pickup step is a step of picking up the semiconductor chip 31 with a bonding layer from the pressure-sensitive adhesive layer 25. In the pickup step, using pickup means such as a collet C, the semiconductor chip 31 with a bonding layer is picked up from the pressure-sensitive adhesive layer 25 having reduced tackiness, as illustrated in FIG. 5(a). In the method for manufacturing the semiconductor package 1, the semiconductor chip 31 with a bonding layer may be prepared in advance, and subsequent steps may be carried out.

[0049] The die attach step is a step of arranging the semiconductor chip 31 with a bonding layer on the substrate 2. In the example of FIG. 5(b), the first semiconductor chip 3 is electrically connected to the circuit pattern 7 of the substrate 2 via the bonding layer 9, and the first semiconductor chip 3 is electrically connected to the circuit pattern 8 via the first wire 10. In this state, the semiconductor chip 31 with a bonding layer is thermocompression-bonded such that the bonding layer 24 faces the substrate 2. As a result, the embedding portion 5 embedding the first semiconductor chip 3, the circuit pattern 7, and the first wire 10 is formed between the second semiconductor chip 4 and the substrate 2.

[0050] When a heating temperature during thermocompression bonding is increased, the bonding layer 24 softens, and the embedding property tends to further improve. A duration of the thermocompression bonding may be, for example, 0.5 seconds to 20 seconds, and may be 1 second to 5 seconds. A pressure during the thermocompression bonding may be 0.01 MPa to 5 MPa, and may be 0.02 MPa to 2 MPa.

[0051] After the pressure bonding, a structure including the bonding layer 24 may be further heated to advance curing of the bonding layer 24. In this case, the temperature and the temperature are appropriately set on the basis of a curing temperature of the bonding layer 24 and the like. The temperature may be changed stepwise. A heating temperature may be 40°C to 300°C, and may be 60°C to 200°C. A heating time may be 30 minutes to 300 minutes.

[0052] Thereafter, the second semiconductor chip 4 is electrically connected to the circuit pattern 8 by the second wire 11, and the first semiconductor chip 3, the second semiconductor chip 4, the first wire 10,

and the second wire 11 are sealed by the sealing portion 6, and thereby the semiconductor package 1 illustrated in FIG. 1 is obtained. The sealing portion 6 is formed by, for example, injection molding using a mold. After formation of the sealing portion 6, the sealing portion 6 may be further heated to advance curing of the sealing portion 6. In this case, the heating temperature may be 165°C to 185°C. The heating time may be 0.5 hours to 8 hours.

[0053] In manufacturing the semiconductor package 1 as described above, the first semiconductor chip 3 is required to be sufficiently embedded by the embedding portion 5 using the bonding layer 24 (embedding property). Regarding the embedding property, achieving both suppression of bleed and suppression of voids is important. Bleed is, for example, as illustrated in FIG. 6(a), a phenomenon in which the embedding portion 5 extends out from between the substrate 2 and the second semiconductor chip 4. When bleed occurs, problems may arise such as interference with other elements on the substrate 2 and a decrease in workability in connecting a wire, for example, the second wire 11.

[0054] In addition, a void is, for example, as illustrated in FIG. 6(b), a phenomenon in which, for example, a gap G is generated in the embedding portion 5 between the substrate 2 and the second semiconductor chip 4. When the void occurs, reliability may be reduced due to defective embedding of the first semiconductor chip 3, and a phenomenon such as bowing, in which the embedding portion 5 bulges upward together with the second semiconductor chip 4 in accordance with the volume of the gap G, may also further occur.

[0055] Suppression of bleed and suppression of voids are in a trade-off

relationship due to the volume of the embedding portion 5 and the like. For example, when the volume of the embedding portion 5 becomes excessive, the embedding portion 5 readily extends out from between the substrate 2 and the second semiconductor chip 4, and when the volume of the embedding portion 5 is insufficient, the gap G readily occurs in the embedding portion 5 between the substrate 2 and the second semiconductor chip 4.

[0056] In response to such a problem, in the laminated film 21, as illustrated in FIG. 7 and other drawings, a flow control portion 41 that imparts anisotropy to fluidity of the bonding layer 24 during thermocompression bonding is provided on a facing surface 24a of the bonding layer 24 facing the pressure-sensitive adhesive layer 25. The facing surface 24a of the bonding layer 24 becomes an opposite surface 24b facing opposite from the surface attached to the semiconductor wafer W in the semiconductor chip 31 with a bonding layer produced in the manufacturing process of the semiconductor package 1 described above (see, for example, FIG. 16(a)). The facing surface 24a becomes the surface pressed against the substrate 2 and the first semiconductor chip 3 on the substrate when the semiconductor chip 31 with a bonding layer is thermocompression-bonded to the substrate 2 (see FIG. 5(b)).

[0057] The flow control portion 41 is formed so as to extend in one in-plane direction of the facing surface 24a. In the example of FIG. 7, multiple flow control portions 41 are arrayed in the width direction of the base material film 22 in the in-plane direction of the facing surface 24a. Each of the flow control portions 41 is formed in a linear shape continuous in a direction along the extending direction of the base

material film 22. When the semiconductor package 1 is manufactured using the laminated film 21 having such a configuration, flow of the bonding layer 24 is guided by the flow control portions 41 when the semiconductor chip 31 with a bonding layer is thermocompression-bonded to the substrate 2. For this reason, as illustrated in FIG. 8, fluidity of the bonding layer 24 in a direction intersecting (orthogonal to) the flow control portions 41 is made relatively low, while fluidity of the bonding layer 24 in a direction along the flow control portions 41 is made relatively high.

[0058] In the example of FIG. 8, the planar shape of the second semiconductor chip 4 is rectangular. In this case, by thermocompression-bonding the semiconductor chip 31 with a bonding layer to the substrate 2 in a state in which an extending direction of the flow control portion 41, namely, the direction in which the bonding layer 24 readily flows, is aligned with the long-side direction of the second semiconductor chip 4, extension of the embedding portion 5 from between the substrate 2 and the second semiconductor chip 4 is suitably suppressed.

[0059] The L/S (line-and-space) of the flow control portion 41 is set in accordance with the planar shape of the first semiconductor chip 3 embedded by the embedding portion 5. The L/S of the flow control portion 41 is set such that, for example, one or multiple flow control portions 41 overlap the first semiconductor chip 3 when the semiconductor chip 31 with a bonding layer is thermocompression-bonded to the substrate 2. As one example, when the planar dimensions of the first semiconductor chip 3 are 5 mm × 10 mm, the L/S of the flow

control portion 41 may be  $2500\ \mu\text{m}/5\ \mu\text{m}$  to  $5\ \mu\text{m}/2500\ \mu\text{m}$ .

[0060] The flow control portion 41 may be configured in various forms. In the examples of FIG. 9(a) and FIG. 9(b), the flow control portion 41 is constituted by a recess 42 extending in one in-plane direction of the facing surface 24a. The cross-sectional shape of a recess 42A illustrated in FIG. 9(a) is, for example, arcuate. The cross-sectional shape of a recess 42B illustrated in FIG. 9(b) is rectangular. By the recess 42, a part of the bonding layer 24 is reduced in thickness at the facing surface 24a. The reduction amount in thickness of the bonding layer 24 by the recess 42 (volume reduction amount) is not particularly limited as long as anisotropy arises in fluidity of the bonding layer 24 during thermocompression bonding, but, for example, a design may be adopted such that, in each semiconductor chip 31 with a bonding layer produced using the laminated film 21, a sum total of the reduction amounts in thickness of the bonding layer 24 by the recess 42 becomes approximately equal to the volume of the first semiconductor chip 3. The depth of the recess 42 is designed, for example, on the basis of the volume of the first semiconductor chip 3 and the L/S of the recess 42. The depth of the recess 42 may be, for example,  $5\ \mu\text{m}$  to  $1200\ \mu\text{m}$ .

[0061] The recess 42A having a wavy or arcuate cross-sectional shape as illustrated in FIG. 9(a) may be formed, for example, by a bar coater 43. As the bar coater 43, a wireless bar 44 as illustrated in FIG. 10(a) may be used, for example. The wireless bar 44 has groove portions 44a formed on a peripheral surface of a stainless steel shaft. When the recess 42A is formed using the wireless bar 44, the bonding layer 24 is heated to a predetermined temperature, and while the groove portions 44a on

the peripheral surface of the wireless bar 44 are pressed against one surface of the bonding layer 24 (a surface to serve as the facing surface 24a), the wireless bar 44 is linearly moved in the in-plane direction of the one surface of the bonding layer 24. As a result, the recess 42A having a wavy or arcuate cross-sectional shape corresponding to the shape of the groove portions 44a is formed on the one surface of the bonding layer 24. By adjusting a pitch P and a depth H of the groove portions 44a of the wireless bar 44, a pocket area A between the groove portions 44a and 44a (see FIG. 10(b)), and the like, the recess 42A having a desired shape and L/S is formed on the facing surface 24a of the bonding layer 24.

[0062] In addition, as the bar coater 43, a wire bar 45 as illustrated in FIG. 11(a) may be used, for example. The wire bar 45 has a wire 45a wound around a peripheral surface of a stainless steel shaft. When the recess 42A is formed using the wire bar 45, similarly to the case of using the wireless bar 44, the bonding layer 24 is heated to a predetermined temperature, and while the wire 45a on the peripheral surface of the wire bar 45 is pressed against one surface of the bonding layer 24 (a surface to serve as the facing surface 24a), the wire bar 45 is linearly moved in the in-plane direction of the one surface of the bonding layer 24. As a result, the recess 42A having a wavy or arcuate cross-sectional shape corresponding to the shape of the wire 45a is formed on the one surface of the bonding layer 24. By adjusting a diameter D of the wire 45a of the wire bar 45, the pocket area A between the wires 45a and 45a (see FIG. 11(b)), and the like, the recess 42A having a desired shape and L/S is formed on the facing surface 24a of the bonding layer 24.

[0063] The recess 42B having a rectangular cross-sectional shape as illustrated in FIG. 9(b) may be formed, for example, as illustrated in FIG. 12, by partially cutting the bonding layer 24 by irradiation with laser light L. As the laser light L used for processing the recess 42B, a green laser, a CO<sub>2</sub> laser, and the like may be used, for example. The green laser is obtained by converting a fundamental wave having a wavelength of 1064 nm from a YAG laser or a semiconductor laser into a second harmonic wave having a wavelength of 532 nm using a nonlinear optical crystal or the like. The CO<sub>2</sub> laser is a laser in an infrared band having a wavelength of approximately 10 μm, obtained by amplifying light using CO<sub>2</sub> as a medium.

[0064] By linearly moving the laser light L in the in-plane direction of the one surface of the bonding layer 24, a part of the bonding layer 24 is cut, and the recess 42B having a rectangular cross-sectional shape is formed on the one surface of the bonding layer 24. By adjusting irradiation conditions of the laser light L, the recess 42B having a desired cross-sectional shape and L/S is formed on the one surface of the bonding layer 24. The cross-sectional shape of the recess 42B is not limited to a rectangular shape, and various shapes such as a triangular shape, a semicircular shape, a U-shape, and a step shape may be applied. For example, when a femtosecond green laser is used for processing the recess 42B, the output may be 0.1 W to 0.3 W, the scanning speed may be 500 mm/second, and the repetition frequency may be 100 kHz.

[0065] In the example of FIG. 13(a), the flow control portion 41 is constituted by a modified portion 46 extending in one in-plane direction of the facing surface 24a. The modified portion 46 may be formed, for

example, as illustrated in FIG. 13(b), by partially curing the bonding layer 24 by light irradiation using a mask M having a predetermined pattern. Light F used for curing the bonding layer 24 is, for example, ultraviolet light. As a light source, a mercury lamp or the like may be used, for example. The output of the ultraviolet light may be 1 W/cm to 100 W/cm. The integrated light quantity of the ultraviolet light may be 10 mJ/cm<sup>2</sup> to 1000 mJ/cm<sup>2</sup>.

[0066] In the example of FIG. 14(a), the flow control portion 41 is constituted by a roughened portion 47 extending in one in-plane direction of the facing surface 24a. The roughened portion 47 may be formed, for example, as illustrated in FIG. 14(b), by partially modifying the bonding layer 24 by irradiation with laser light L. As the laser light L used for processing the roughened portion 47, a green laser, a CO<sub>2</sub> laser, and the like may be used, for example, similarly to the case of forming the recess 42B. In processing using a green laser, the surface of the bonding layer 24 in the roughened portion 47 tends to become fibrous with a constant depth in the depth direction. In addition, in processing using a CO<sub>2</sub> laser, the constituent material of the bonding layer 24 becomes in a state as if melted and solidified, and tends to become smoother in uneven shape than in the case of using a green laser. The surface roughness of the roughened portion 47 is not particularly limited as long as anisotropy arises in fluidity of the bonding layer 24 during thermocompression bonding, but, for example, the arithmetic average roughness Ra may be 0.1 μm to 2.0 μm.

[0067] Next, the method for manufacturing the laminated film 21 described above will be described.

[0068] FIG. 15 is a flowchart illustrating an example of a method for manufacturing the laminated film having the flow control portion 41. As illustrated in FIG. 15, the method for manufacturing the laminated film 21 includes a preparation step (step S01), a formation step (step S02), and a lamination step (step S03). These steps are carried out, for example, by a roll to roll method.

[0069] The preparation step S01 is a step of preparing the elongated base material film 22 overlapping the bonding layer 24. In the preparation step S01, a stock roll of the elongated base material film 22 provided with the bonding layer 24 on one-surface side is unwound from an unwinding roller. The formation step S02 is a step of forming, on one surface of the bonding layer 24, the flow control portion 41 that imparts anisotropy to fluidity of the bonding layer 24 during thermocompression bonding. In the formation step S02, one surface of the pressure-sensitive adhesive layer 25 is processed, and the flow control portion 41 is formed on the one surface. In the formation step S02, processing to be carried out differs depending on the type of the flow control portion 41 to be formed.

[0070] When the recess 42 is formed using the bar coater 43, the bar coater 43 is pressed against one surface of the bonding layer 24 while the bonding layer 24 is heated, thereby forming the recess 42 extending in one in-plane direction of the one surface of the bonding layer 24 (see FIGS. 10(a) and 11(a)). When the bonding layer 24 is partially cut, the laser light L is linearly moved in the in-plane direction of the one surface of the bonding layer 24, thereby cutting a part of the bonding layer 24 and forming the recess 42 extending in one in-plane direction of the one

surface of the bonding layer 24 (see FIG. 12).

[0071] When the bonding layer 24 is partially cured, the light F is irradiated onto one surface of the bonding layer 24 through the mask M having a predetermined pattern, thereby forming the modified portion 46 extending in one in-plane direction of the one surface of the bonding layer 24 (see FIG. 13(b)). When the bonding layer 24 is partially modified, the laser light L is linearly moved in the in-plane direction of the one surface of the bonding layer 24, thereby modifying a part of the bonding layer 24 and forming the roughened portion 47 extending in one in-plane direction of the one surface of the bonding layer 24 (see FIG. 14(b)).

[0072] The lamination step S03 is a step of laminating the pressure-sensitive adhesive layer 25 and the base material layer 27 on the bonding layer 24 such that one surface of the bonding layer 24 becomes the facing surface 24a facing the pressure-sensitive adhesive layer 25. Here, a film in which the pressure-sensitive adhesive layer 25 is laminated on the base material layer 27 is prepared, and the pressure-sensitive adhesive layer 25 and the base material layer 27 are laminated on one surface of the base material film 22 such that the pressure-sensitive adhesive layer 25 faces the bonding layer 24. After lamination, the pressure-sensitive adhesive layer 25 and the base material layer 27 are precut into a circular shape. As a result, the label portion 23 is formed on the one surface of the base material film 22, and the laminated film 21 illustrated in FIGS. 2 and 3 is obtained. In precutting the pressure-sensitive adhesive layer 25 and the base material layer 27, the projecting portion P projecting outward beyond an edge of the bonding layer 24 is formed, and the

projecting portion P is overlaid on one surface of the base material film 22. As a result, the bonding layer 24 on the one surface of the base material film 22 comes to be in a state of being covered with the pressure-sensitive adhesive layer 25 and the base material layer 27.

5 [0073] As described above, in the laminated film 21, the flow control portion 41 is provided on the facing surface 24a of the bonding layer 24 facing the pressure-sensitive adhesive layer 25, and fluidity of the bonding layer 24 during thermocompression bonding has anisotropy. Therefore, when the bonding layer 24 is used as the embedding portion  
10 5 for a semiconductor chip, suppression of bleed is achieved by, for example, sufficiently securing the volume of the embedding portion 5 between the substrate 2 and the second semiconductor chip 4 (memory chip) to suppress voids while aligning the direction in which the bonding layer 24 readily flows with the long-side direction of the planar shape of  
15 the memory chip. Therefore, the laminated film 21 favorably achieves both suppression of bleed and suppression of voids in manufacturing the semiconductor package 1.

[0074] In the present embodiment, the flow control portion 41 may be constituted by the recess 42 extending in one in-plane direction of the  
20 facing surface 24a. According to such a configuration, the recess 42 appropriately reduces a part of the volume of the bonding layer 24. In addition, during thermocompression bonding of the bonding layer 24, flow of the bonding layer 24 in an extending direction of the recess 42 is promoted. In the present embodiment, the flow control portion 41 may  
25 be constituted by the modified portion 46 or the roughened portion 47 extending in one in-plane direction of the facing surface 24a. Even in

such a configuration, during thermocompression bonding of the bonding layer 24, flow of the bonding layer 24 in an extending direction of the modified portion 46 or the roughened portion 47 is promoted. According to these configurations, suppression of bleed and suppression of voids are more favorably achieved in manufacturing the semiconductor package 1.

[0075] In addition, in the present embodiment, in the label portion 23, the pressure-sensitive adhesive layer 25 and the base material layer 27 have the projecting portion P projecting outward beyond an edge of the bonding layer 24, and the projecting portion P overlaps one surface of the base material film 22. According to such a configuration, attachment of the pressure-sensitive adhesive layer 25 and the base material layer 27 to an object such as the semiconductor wafer W is facilitated. In addition, because the bonding layer 24 is covered with the pressure-sensitive adhesive layer 25 and the base material layer 27, protection of the flow control portion 41 is achieved.

[0076] In the above embodiment, the flow control portion 41 is formed on the facing surface 24a of the bonding layer 24 of the laminated film 21, but, as illustrated in FIG. 16(a), the flow control portion 41 may be formed in the bonding layer 24 of the semiconductor chip 31 with a bonding layer. In the semiconductor chip 31 with a bonding layer of FIG. 16(a), the flow control portion 41 is provided on the opposite surface 24b of the bonding layer 24 opposite from the chip portion (semiconductor chip) 32.

[0077] In the example of FIG. 16(a), the flow control portion 41 is constituted by a recess 52 extending in one in-plane direction of the

opposite surface 24b of the bonding layer 24. The recess 52 may be formed, for example, as illustrated in FIG. 16(b), by partially cutting the bonding layer 24 by irradiation with laser light L. In this case, for example, in a state in which the chip portion 32 side of the semiconductor chip 31 with a bonding layer is held by the collet C, the laser light L is linearly moved in the in-plane direction of the opposite surface 24b of the bonding layer 24. As a result, a part of the bonding layer 24 is cut, and the recess 52 is formed on the opposite surface 24b of the bonding layer 24.

[0078] In the example of FIG. 17(a), the flow control portion 41 is constituted by a roughened portion 53 extending in one in-plane direction of the opposite surface 24b of the bonding layer 24. The roughened portion 53 may be formed, for example, as illustrated in FIG. 17(b), by partially modifying the bonding layer 24 by irradiation with laser light L. In this case, for example, in a state in which the chip portion 32 side of the semiconductor chip 31 with a bonding layer is held by the collet C, the laser light L is linearly moved in the in-plane direction of the opposite surface 24b of the bonding layer 24. As a result, a part of the bonding layer 24 is modified, and the roughened portion 53 is formed on the opposite surface 24b of the bonding layer 24.

[0079] Next, the method for manufacturing the semiconductor chip 31 with a bonding layer described above will be described.

[0080] FIG. 18 is a flowchart illustrating an example of a method for manufacturing the semiconductor chip with a bonding layer having the flow control portion 41. As illustrated in FIG. 18, the method for manufacturing the semiconductor chip 31 with a bonding layer includes

a preparation step (step S11) and a formation step (step S12).

[0081] The preparation step S11 is a step of preparing the semiconductor chip 31 with a bonding layer including the chip portion (semiconductor chip) 32 and the bonding layer 24 provided on one-surface side of the chip portion 32. In the preparation step S11, for example, the attachment step, the dicing step, the irradiation step, and the pickup step in the method for manufacturing the semiconductor package 1 described above are each carried out, and a state in which the chip portion 32 side of the semiconductor chip 31 with a bonding layer is held by the collet C is formed.

[0082] The formation step S12 is a step of forming, on the opposite surface 24b of the bonding layer 24 opposite from the chip portion 32, the flow control portion 41 that imparts anisotropy to fluidity of the bonding layer 24 during thermocompression bonding. In the formation step S12, processing to be carried out differs depending on the type of the flow control portion 41 to be formed. When the bonding layer 24 is partially cut, the laser light L is linearly moved in the in-plane direction of the opposite surface 24b of the bonding layer 24, thereby cutting a part of the bonding layer 24 and forming the recess 52 extending in one in-plane direction of the opposite surface 24b of the bonding layer 24 (see FIG. 16(b)). When the bonding layer 24 is partially modified, the laser light L is linearly moved in the in-plane direction of the opposite surface 24b of the bonding layer 24, thereby modifying a part of the bonding layer 24 and forming the roughened portion 53 extending in one in-plane direction of the opposite surface 24b of the bonding layer 24 (see FIG. 17(b)).

[0083] Also in such a semiconductor chip 31 with a bonding layer, the flow control portion 41 is provided on the opposite surface 24b of the bonding layer 24 opposite from the chip portion 32, and fluidity of the bonding layer 24 during thermocompression bonding has anisotropy. Therefore, when the bonding layer 24 is used as the embedding portion 5 for a semiconductor chip, suppression of bleed is achieved by, for example, sufficiently securing the volume of the embedding portion 5 between the substrate 2 and the memory chip (the second semiconductor chip 4) to suppress voids while aligning the direction in which the bonding layer 24 readily flows with the long-side direction of the planar shape of the memory chip. Therefore, the semiconductor chip 31 with a bonding layer favorably achieves both suppression of bleed and suppression of voids in manufacturing the semiconductor package 1.

[0084] In the present embodiment, the flow control portion 41 may be constituted by the recess 52 extending in one in-plane direction of the opposite surface 24b. According to such a configuration, the recess 52 appropriately reduces a part of the volume of the bonding layer 24. In addition, during thermocompression bonding of the bonding layer 24, flow of the bonding layer 24 in an extending direction of the recess 52 is promoted. In the present embodiment, the flow control portion 41 may be constituted by the roughened portion 53 extending in one in-plane direction of the opposite surface 24b. Even in such a configuration, during thermocompression bonding of the bonding layer 24, flow of the bonding layer 24 in an extending direction of the roughened portion 53 is promoted. According to these configurations, suppression of bleed and suppression of voids are more favorably achieved in manufacturing

the semiconductor package 1.

[0085] The present disclosure is not limited to the above embodiment. For example, in the above embodiment, the linear flow control portion 41 is formed in a direction along the extending direction of the base material film 22 in the in-plane direction of the facing surface 24a in the laminated film 21, but the extending direction of the flow control portion 41 is not limited thereto and may be along a direction obliquely intersecting the extending direction of the base material film 22 or may be along a direction orthogonal to the extending direction of the base material film 22.

[0086] In addition, in the above embodiment, the continuous linear flow control portion 41 is exemplified, but the shape of the flow control portion 41 is not limited thereto. For example, the flow control portion 41 may have a dotted or dashed shape, or may have a wavy-line shape. In addition, when multiple flow control portions 41 are formed, widths, cross-sectional shapes, arrangement intervals, and the like of the respective flow control portions 41 may differ from each other.

#### **Reference Signs List**

|        |    |                                                |
|--------|----|------------------------------------------------|
| [0087] | 1  | Semiconductor package (semiconductor device)   |
|        | 2  | Substrate                                      |
|        | 3  | First semiconductor chip (semiconductor chip)  |
|        | 4  | Second semiconductor chip (semiconductor chip) |
|        | 5  | Embedding portion                              |
|        | 21 | Laminated film                                 |
|        | 22 | Base material film                             |
|        | 23 | Label portion                                  |

|    |              |                                       |
|----|--------------|---------------------------------------|
|    | 24           | Bonding layer                         |
|    | 24a          | Facing surface                        |
|    | 24b          | Opposite surface                      |
|    | 25           | Pressure-sensitive adhesive layer     |
| 5  | 27           | Base material layer                   |
|    | 31           | Semiconductor chip with bonding layer |
|    | 32           | Chip portion (semiconductor chip)     |
|    | 41           | Flow control portion                  |
|    | 42(42A, 42B) | Recess                                |
| 10 | 43           | Bar coater                            |
|    | 52           | Recess                                |
|    | 46           | Modified portion                      |
|    | 47, 53       | Roughened portion                     |
|    | L            | Laser light                           |
| 15 | M            | Mask                                  |
|    | P            | Projecting portion                    |

## CLAIMS

[Claim 1] A laminated film comprising:

an elongated base material film; and

label portions provided on one surface of the base material film

5 at predetermined intervals in an extending direction of the base material film,

wherein the label portions have a bonding layer overlapping the base material film, a pressure-sensitive adhesive layer overlapping the bonding layer, and a base material layer overlapping the pressure-sensitive adhesive layer, and

10 a flow control portion is provided on a surface of the bonding layer facing the pressure-sensitive adhesive layer, the flow control portion imparting anisotropy to fluidity of the bonding layer during thermocompression bonding.

15 [Claim 2] The laminated film according to claim 1, wherein the flow control portion is constituted by a recess extending in one in-plane direction of the facing surface.

[Claim 3] The laminated film according to claim 1, wherein the flow control portion is constituted by a modified portion extending in one in-plane direction of the facing surface.

[Claim 4] The laminated film according to claim 1, wherein the flow control portion is constituted by a roughened portion extending in one in-plane direction of the facing surface.

[Claim 5] The laminated film according to any one of claims 1 to 4, wherein, in the label portions, the pressure-sensitive adhesive layer and the base material layer have a projecting portion projecting

outward beyond an edge of the bonding layer, and

the projecting portion overlaps one surface of the base material film.

[Claim 6] A semiconductor chip with a bonding layer comprising:

5 a semiconductor chip; and

a bonding layer provided on one surface side of the semiconductor chip,

wherein a flow control portion is provided on an opposite surface of the bonding layer opposite from the semiconductor chip, and the flow control portion imparts anisotropy to fluidity of the bonding layer during thermocompression bonding.

[Claim 7] The semiconductor chip with a bonding layer according to claim 6, wherein the flow control portion is constituted by a recess extending in one in-plane direction of the opposite surface.

15 [Claim 8] The semiconductor chip with a bonding layer according to claim 6, wherein the flow control portion is constituted by a roughened portion extending in one in-plane direction of the opposite surface.

[Claim 9] A method for manufacturing a laminated film comprising:

20 a preparation step of preparing an elongated base material film overlapping a bonding layer;

a formation step of forming, on one surface of the bonding layer, a flow control portion imparting anisotropy to fluidity of the bonding layer during thermocompression bonding; and

25 a lamination step of laminating a pressure-sensitive adhesive layer and a base material layer on the bonding layer such that the one

surface of the bonding layer becomes a facing surface of the pressure-sensitive adhesive layer.

5 [Claim 10] The method for manufacturing a laminated film according to claim 9, wherein, in the formation step, a recess extending in one in-plane direction of the one surface is formed as the flow control portion by pressing a bar coater against the one surface while heating the bonding layer.

10 [Claim 11] The method for manufacturing a laminated film according to claim 9, wherein, in the formation step, a recess extending in one in-plane direction of the one surface is formed as the flow control portion by partially cutting the bonding layer by irradiation with laser light.

15 [Claim 12] The method for manufacturing a laminated film according to claim 9, wherein, in the formation step, a modified portion extending in one in-plane direction of the one surface is formed as the flow control portion by partially curing the bonding layer by light irradiation using a mask having a predetermined pattern.

20 [Claim 13] The method for manufacturing a laminated film according to claim 9, wherein, in the formation step, a roughened portion extending in one in-plane direction of the one surface is formed as the flow control portion by partially modifying the bonding layer by irradiation with laser light.

25 [Claim 14] The method for manufacturing a laminated film according to any one of claims 9 to 13, wherein, in the lamination step, the pressure-sensitive adhesive layer and the base material layer are precut such that a projecting portion projecting outward beyond an edge

of the bonding layer is formed, and the projecting portion is overlaid on one surface of the base material film.

[Claim 15] A method for manufacturing a semiconductor chip with a bonding layer comprising:

5 a preparation step of preparing a semiconductor chip with a bonding layer including a semiconductor chip and a bonding layer provided on one surface side of the semiconductor chip; and

a formation step of forming, on an opposite surface of the bonding layer opposite from the semiconductor chip, a flow control portion imparting anisotropy to fluidity of the bonding layer during thermocompression bonding.

[Claim 16] The method for manufacturing a semiconductor chip with a bonding layer according to claim 15, wherein, in the formation step, a recess extending in one in-plane direction of the opposite surface is formed as the flow control portion by cutting the opposite surface by irradiation with laser light.

[Claim 17] The method for manufacturing a semiconductor chip with a bonding layer according to claim 15, wherein, in the formation step, a roughened portion extending in one in-plane direction of the opposite surface is formed as the flow control portion by partially modifying the bonding layer by irradiation of the opposite surface with laser light.

[Claim 18] A method for manufacturing a semiconductor device comprising: preparing the semiconductor chip with a bonding layer according to any one of claims 6 to 8 and a substrate on which a semiconductor chip is mounted; thermocompression-bonding the

semiconductor chip with a bonding layer to the substrate such that the bonding layer faces the substrate; and forming an embedding portion between the semiconductor chip of the semiconductor chip with a bonding layer and the substrate.

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