CLAIMS

1. A non-volatile semiconductor memory device including: a plurality of memory cell column wirings to which a charge accumulating voltage or a charge accumulating prevention voltage is applied; and a plurality of memory cell transistors having an N-channel type structure and disposed in a row and column matrix with respect to the plurality of memory cell column wirings and a plurality of word lines, the non-volatile semiconductor memory device causing a selected memory cell transistor in the plurality of memory cell transistors to accumulate electric charges based on a voltage difference between the charge accumulating voltage and a voltage to be applied to the word lines, the non-volatile semiconductor memory device comprising:

a plurality of first semiconductor switches formed by PMOS transistors, the first semiconductor switches being provided for the respective memory cell column wirings; and

a plurality of second semiconductor switches formed by NMOS transistors, the second semiconductor switches being provided for the respective memory cell column wirings,

wherein, in a non-selected memory cell column wiring in which only non-selected memory cell transistors except for the selected memory transistor are disposed, the first semiconductor switches are configured to be switched on by means of a first gate voltage and to apply the charge accumulating prevention voltage to the non-selected memory cell transistors whereas,

in a selected memory cell column wiring in which the selected memory cell transistor is disposed, the second semiconductor switches are configured to be switched on by means of a second gate voltage and to apply the charge accumulating voltage to the selected memory cell transistor.

2. The non-volatile semiconductor memory device according to claim 1, further comprising:

a first selection gate line equally applying the first gate voltage to the respective first semiconductor switches; and

a second selection gate line equally applying the second gate voltage to the respective second semiconductor switches,

wherein the first semiconductor switches are configured to be switched on by means of a voltage difference between the charge accumulating prevention voltage and the first gate voltage and to apply the charge accumulating prevention voltage to the non-selected memory cell transistors, and

the second semiconductor switches are configured to be switched on by means of a voltage difference between the charge accumulating voltage and the second gate voltage and to apply the charge accumulating voltage to the selected memory cell transistor.

3. The non-volatile semiconductor memory device according to claim 1,

wherein each of the memory cell column wirings is formed by a bit line and a source line, and

each of the memory cell transistors is connected at one terminal thereof to the bit line and is connected at the other terminal thereof to the source line.

4. The non-volatile semiconductor memory device according to claim 3,

wherein the bit line is formed by a higher order bit line and a lower order bit line connected to the higher order bit line through the first semiconductor switch, and

each of the memory cell transistors is connected at the one terminal thereof to the lower order bit line.

5. The non-volatile semiconductor memory device according to claim 3 or 4,

wherein the source line is formed by a higher order source line and a lower order source line connected to the higher order source line through the second semiconductor switch, and

each of the memory cell transistors is connected to at the other

terminal thereof to the lower order source line.

6. The non-volatile semiconductor memory device according to claim 1, wherein either the first semiconductor switch or the second semiconductor switch has a gate insulating layer disposed between a gate and a semiconductor substrate, the gate insulating film having a film thickness of less than 13[nm].

7. The non-volatile semiconductor memory device according to claim 1, wherein the memory cell transistors, the first semiconductor switches and the second semiconductor switches are formed on a unit well structure divided into a predetermined number of wells.

8. The non-volatile semiconductor memory device according to claim 1, wherein a memory array in which the memory cell transistors are aligned is formed on a plurality of P-wells and the PMOS transistors are formed on an N-well electrically insulating the P-wells.

CLAIMS

1. A non-volatile semiconductor memory device including: a plurality of memory cell column wirings to which a charge accumulating voltage or a charge accumulating prevention voltage is applied; and a plurality of memory cell transistors having an N-channel type structure and disposed in a row and column matrix with respect to the plurality of memory cell column wirings and a plurality of word lines, the non-volatile semiconductor memory device causing a selected memory cell transistor in the plurality of memory cell transistors to accumulate electric charges based on a voltage difference between the charge accumulating voltage and a voltage to be applied to the word lines, the non-volatile semiconductor memory device comprising:

a plurality of first semiconductor switches formed by PMOS transistors, the first semiconductor switches being provided for the respective memory cell column wirings; and

a plurality of second semiconductor switches formed by NMOS transistors, the second semiconductor switches being provided for the respective memory cell column wirings,

wherein, in a non-selected memory cell column wiring in which only non-selected memory cell transistors except for the selected memory transistor are disposed, the first semiconductor switches are configured to be switched on by means of a first gate voltage and to apply the charge accumulating prevention voltage to the non-selected memory cell transistors whereas,

in a selected memory cell column wiring in which the selected memory cell transistor is disposed, the second semiconductor switches are configured to be switched on by means of a second gate voltage and to apply the charge accumulating voltage to the selected memory cell transistor.

2. The non-volatile semiconductor memory device according to claim 1, further comprising:

a first selection gate line equally applying the first gate voltage to the respective first semiconductor switches; and

a second selection gate line equally applying the second gate voltage to the respective second semiconductor switches,

wherein the first semiconductor switches are configured to be switched on by means of a voltage difference between the charge accumulating prevention voltage and the first gate voltage and to apply the charge accumulating prevention voltage to the non-selected memory cell

transistors, and

the second semiconductor switches are configured to be switched on by means of a voltage difference between the charge accumulating voltage and the second gate voltage and to apply the charge accumulating voltage to the selected memory cell transistor.

3. The non-volatile semiconductor memory device according to claim 1,

wherein each of the memory cell column wirings is formed by a bit line and a source line, and

each of the memory cell transistors is connected at one terminal thereof to the bit line and is connected at the other terminal thereof to the source line.

4. The non-volatile semiconductor memory device according to claim 3,

wherein the bit line is formed by a higher order bit line and a lower order bit line connected to the higher order bit line through the first semiconductor switch, and

each of the memory cell transistors is connected at the one terminal thereof to the lower order bit line.

5. The non-volatile semiconductor memory device according to claim 3 or 4,

wherein the source line is formed by a higher order source line and a lower order source line connected to the higher order source line through the second semiconductor switch, and

each of the memory cell transistors is connected to at the other terminal thereof to the lower order source line.

6. The non-volatile semiconductor memory device according to claim 1, wherein either the first semiconductor switch or the second semiconductor switch has a gate insulating layer disposed between a gate and a semiconductor substrate, the gate insulating film having a film thickness of less than 13[nm].

7. The non-volatile semiconductor memory device according to claim 1, wherein the memory cell transistors, the first semiconductor switches and the second semiconductor switches are formed on a unit well structure divided into a predetermined number of wells.

8. The non-volatile semiconductor memory device according to claim 1, wherein a memory array in which the memory cell transistors are aligned is formed on a plurality of P-wells and the PMOS transistors are formed on an N-well electrically insulating the P-wells.

9. The non-volatile semiconductor memory device according to claim 4, wherein either the first semiconductor switch or the second semiconductor switch has a gate insulating layer disposed between a gate and a semiconductor substrate, the gate insulating film having a film thickness of less than 13[nm].