BUMP ON VIA - PACKAGING AND METHODOLOGIES

ABSTRACT

A semiconductor package with a semiconductor chip having under bump metallizations (UBMs) on a first surface and a substrate having open vias. The substrate is attached to the semiconductor chip with the UBMs in alignment with the open vias. An encapsulant surrounds the semiconductor chip and the substrate and a conductor fills the open vias to form external package connections. A method of forming a semiconductor package having external package connections includes providing a semiconductor chip having under bump metallizations (UBMs) on a first surface; attaching the first surface of the semiconductor chip to a substrate, the UBMs of the semiconductor chip being in alignment with open vias formed in the substrate; encapsulating the semiconductor chip and the substrate; and filling with open vias with a conductor to form the external package connections.

FIG. 1E