CLAIMS:

1. A method of forming a plurality of conductive lines in the fabrication of integrated circuitry, comprising:

forming a trench into a damascene material received over a substrate, the trench having first and second opposing trench sidewalls, the first trench sidewall being longitudinally elongated to comprise a longitudinal contour of a first sidewall of one of the plurality of conductive lines being formed, the second trench sidewall being longitudinally elongated to comprise a longitudinal contour of a first sidewall of another of the plurality of conductive lines being formed;

depositing conductive material to within the trench to span between the first and the second trench sidewalls; and

etching through the conductive material longitudinally between the first and second trench sidewalls to form the longitudinal contour of a second sidewall of the one conductive line within the trench and to form the longitudinal contour of a second sidewall of the another conductive line within the trench.

2. The method of claim 1 comprising forming no more than two conductive lines within the trench.

3. The method of claim 1 wherein a minimum space between the longitudinal contours within each of the one and the another conducive lines is no greater than 20 nanometers.

4. The method of claim 1 wherein the etching forms the one conductive line and the another conductive line to be of the same shape in lateral cross section along at least a majority of length of the one conductive line and the another conductive line.

5. The method of claim 4 wherein the etching forms the one conductive line and the another conductive line to be mirror images of one another in lateral cross section along at least the majority of length of the one conductive line and the another conductive line.

6. The method of claim 1 wherein the conductive material is deposited to overfill the trench, and further comprising planarizing the conductive material back at least to the damascene material prior to the etching through the conductive material.

7. A method of forming a pair of conductive lines in the fabrication of integrated circuitry, comprising:

forming a trench into a damascene material received over a substrate, the trench having first and second opposing trench sidewalls and a minimum width there-between which is at least about $3W_m$ where W_m is the minimum width of the conductive lines being formed, the first trench sidewall being longitudinally elongated to comprise a longitudinal contour of a first sidewall of a first of the pair of conductive lines being formed, the second trench sidewall being longitudinally elongated to comprise a longitudinal contour of a first sidewall of a second of the pair of conductive lines being formed;

depositing conductive material to within the trench to span between the first and second trench sidewalls; and

etching through the conductive material longitudinally between the first and second trench sidewalls to form the longitudinal contour of a second sidewall of the first conductive line within the trench and to form the longitudinal contour of a second sidewall of the second conductive line within the trench.

8. The method of claim 7 wherein the trench minimum width is about $3W_m$.

9. The method of claim 8 wherein the integrated circuitry is fabricated using photolithography and W_m is F, where F is the minimum photolithographic feature size with which the integrated circuitry is fabricated.

10. The method of claim 8 wherein the integrated circuitry is fabricated using photolithography and W_m is less than F, where F is the minimum photolithographic feature size with which the integrated circuitry is fabricated.

11. The method of claim 7 wherein the etching forms the first and second conductive lines to be of the same shape in lateral cross section along at least a majority of length of the first and second conductive lines.

12. The method of claim 11 wherein the trench minimum width is about 1.5P, where P is pitch of the first and second conductive lines.

13. The method of claim 11 wherein the etching forms the first and second conductive lines to be mirror images of one another in lateral cross section along at least a majority of length of the first and second conductive lines.

14. The method of claim 11 wherein the trench minimum width is about $3W_m$.

15. The method of claim 14 wherein the trench minimum width is about 1.5P, where P is pitch of the first and second conductive lines.

16. The method of claim 7 wherein the etching forms a space within the trench between the first and second conductive lines, and further comprising filling the space with a dielectric material.

17. The method of claim 16 wherein the dielectric material comprises a void between the first and second conductive lines.

18. The method of claim 7 wherein the etching forms a space within the trench between the first and second conductive lines, the space being equal to about W_m in lateral cross section.

19. The method of claim 7 wherein the conductive material within the trench comprises a conductive liner comprising a first composition and a conductive fill material comprising a different second composition received over the conductive liner.

20. The method of claim 19 wherein the etching forms each of the first and second conductive lines to have the first sidewall of the first composition and a base layer of the first composition, the etching forming the second sidewall above the base layer of each of the first and second conductive lines to be of the second composition.

21. The method of claim 19 wherein second composition is of higher electrical conductivity than the first composition.

22. A method of forming a plurality of parallel conductive lines in the fabrication of integrated circuitry, comprising:

forming a plurality of parallel oriented trenches into a damascene material received over a substrate, the trenches individually having first and second opposing trench sidewalls and a minimum width there-between which is at least about $3W_m$ where W_m is the minimum width of a pair of conductive lines being formed within each trench, the first trench sidewall of each trench being longitudinally elongated to comprise a longitudinal contour of a first sidewall of a first of the pair of conductive lines being formed within each trench, the second trench sidewall being longitudinally elongated to comprise a longitudinal contour of a second sidewall of a second of the pair of conductive lines being formed within each trench;

depositing conductive material to within each trench to span between the first and second trench sidewalls of each trench; and

etching through the conductive material longitudinally between the first and second trench sidewalls to form the longitudinal contour of a second sidewall of the first conductive line within each trench and to form the longitudinal contour of a second sidewall of the second conductive line within each trench.

23. The method of claim 22 wherein W_m is no greater than 20 nanometers.

24. The method of claim 22 wherein the etching is conducted through openings between masking blocks, the masking blocks individually spanning between and partially masking respective immediately adjacent of two of the trenches.

25. The method of claim 22 wherein the etching forms the first and second conductive lines to be mirror images of one another in lateral cross section along at least a majority of length of the first and second conductive lines.

26. The method of claim 22 comprising forming the damascene material to comprise insulative material at least some of which remains a part of the finished integrated circuitry.

27. The method of claim 22 comprising forming the damascene material to comprise at least one of semiconductive material and conductive material.

28. A method of forming a pair of conductive lines in the fabrication of integrated circuitry, comprising:

forming a trench into a damascene material received over a substrate, the trench having first and second opposing trench sidewalls which span an elevation of the damascene material, the first trench sidewall being longitudinally elongated to comprise a longitudinal contour of a first sidewall of a first of a pair of conductive lines being formed within the trench, the second trench sidewall being longitudinally elongated to comprise a longitudinal contour of a first sidewall of a second of the pair of conductive lines being formed within the trench;

depositing conductive material to within the trench to span between the first and second trench sidewalls;

recessing the conductive material within the trench and forming a first trench-wall and a second trench-wall over the recessed conductive material, the first trench-wall and the second trench-wall being received within said elevation of the damascene material;

forming a first etch mask against the first trench-wall and a second etch mask against the second trench-wall; and

using the first etch mask and the second etch mask as masking, etching through the conductive material longitudinally between the first and second trench sidewalls to form the longitudinal contour of a second sidewall of the first conductive line within the trench and to form the longitudinal contour of a second sidewall of the second conductive line within the trench.

29. The method of claim 28 wherein the first trench-wall is formed to comprise an upper portion of the first trench sidewall and the second trench-wall is formed to comprise an upper portion of the second trench sidewall.

30. The method of claim 28 wherein the first and second etch masks are formed to comprise an interconnected ring.

31. The method of claim 28 wherein the first and second conductive lines are initially formed to comprise an interconnected ring of the conductive material, and further comprising breaking the ring of the conductive material in at least two locations to separate the first and second conductive lines from being interconnected.

32. The method of claim 28 wherein at least a majority of each of the first and second etch masks remains as part of the finished integrated circuitry.

33. The method of claim 28 wherein forming the first and second etch masks comprises:

depositing a spacer-forming layer to less than fill remaining volume of the trench after the recessing; and

anisotropically etching the spacer-forming layer to form the first and second etch masks to respectively comprise a sidewall spacer received against the first trench-wall and against the second trench-wall.

34. The method of claim 33 wherein the anisotropic etching is conducted without any mask being received over the spacer-forming layer.

35. The method of claim 33 wherein the first trench-wall is formed to comprise an upper portion of the first trench sidewall and the second trench-wall is formed to comprise an upper portion of the second trench sidewall.

36. The method of claim 33 wherein the first and second conductive lines are initially formed to comprise an interconnected ring of the conductive material, and further comprising breaking the ring of the conductive material in at least two locations to separate the first and second conductive lines from being interconnected.

37. The method of claim 33 wherein at least a majority of each of the first and second etch masks remains as part of the finished integrated circuitry.

38. The method of claim 28 wherein,

the first trench-wall is formed to comprise an upper portion of the first trench sidewall and the second trench-wall is formed to comprise an upper portion of the second trench sidewall;

the forming of the first and second etch masks comprises:

depositing a spacer-forming layer to less than fill remaining volume of the trench after the recessing; and

anisotropically etching the spacer-forming layer to form the first and second etch masks to respectively comprise a sidewall spacer received against the first trench-wall and against the second trench-wall;

the first and second conductive lines are initially formed to comprise an interconnected ring of the conductive material, and further comprising breaking the ring of the conductive material in at least two locations to separate the first and second conductive lines from being interconnected; and

at least a majority of each of the first and second etch masks remains as part of the finished integrated circuitry.

39. A method of forming a plurality of parallel conductive lines in the fabrication of integrated circuitry, comprising:

forming a plurality of parallel oriented trenches into a damascene material received over a substrate, the trenches individually having first and second opposing trench sidewalls and a minimum width there-between which is at least about $3W_m$ where W_m is the minimum width of a pair of conductive lines being formed within each trench, the first and second opposing trench sidewalls spanning an elevation of the damascene material, the first trench sidewall of each trench being longitudinally elongated to comprise a longitudinal contour of a first sidewall of a first of the pair of conductive lines being formed within each trench, the second trench sidewall being longitudinally elongated to comprise a longitudinal contour of a second sidewall of a second of the pair of conductive lines being formed within each trench;

depositing conductive material to within each trench to span between the first and second trench sidewalls of each trench;

recessing the conductive material within each trench and forming a first trench-wall and a second trench-wall over the recessed conductive material within each trench, the first trench-wall and the second trench-wall within each trench being received within said elevation of the damascene material;

forming a first etch mask against the first trench-wall and a second etch mask against the second trench-wall within each trench; and

using the first etch masks and the second etch masks as masking, etching through the conductive material longitudinally between the first and second trench sidewalls to form the longitudinal contour of a second sidewall of the first conductive line within each trench and to form the longitudinal contour of a second sidewall of the second conductive line within each trench.

40. The method of claim 39 wherein the first trench-wall is formed to comprise an upper portion of the first trench sidewall of each trench and the second trench-wall is formed to comprise an upper portion of the second trench sidewall of each trench.

41. The method of claim 39 wherein forming the first and second etch masks comprises:

depositing a spacer-forming layer to less than fill remaining volume of each of the trenches after the recessing; and

anisotropically etching the spacer-forming layer to form the first and second etch masks to respectively comprise a sidewall spacer received against the first trench-wall and against the second trench-wall.

42. The method of claim 39 wherein the first and second etch masks are formed to comprise an interconnected ring.

43. The method of claim 39 wherein the first and second conductive lines are initially formed to comprise an interconnected ring of the conductive material within each trench, and further comprising breaking the ring of the conductive material within each trench in at least two locations to separate the first and second conductive lines from being interconnected within each trench.

44. The method of claim 39 wherein at least a majority of each of the first and second etch masks remains as part of the finished integrated circuitry.

45. A method of forming a pair of conductive lines in the fabrication of integrated circuitry, comprising:

forming a trench into a damascene material received over a substrate;

depositing conductive material over the damascene material and to within the trench to overfill the trench;

removing the conductive material back at least to the damascene material to leave at least some of the conductive material remaining in the trench; and

longitudinally etching through the conductive material within the trench to form first and second conductive lines within the trench which are mirror images of one another in lateral cross section along at least a majority of length of the first and second conductive lines.

46. A method of forming an array of conductive lines in the fabrication of integrated circuitry, comprising:

forming a plurality of elongated conductive lines over a substrate; and

providing first and second alternating regions of dielectric material between the conductive lines laterally across the array, the first regions comprising a singular void received within solid insulative material between two immediately adjacent of the conductive lines, the second regions being at least in part characterized by an absence of any void space within solid insulative material between two immediately adjacent conductive lines.

47. The method of claim 46 comprising forming the first and second regions at different times.

48. The method of claim 47 comprising forming the first regions after forming the second regions.

49. Integrated circuitry comprising an array of conductive lines, comprising:

a plurality of elongated conductive lines received over a substrate; and

first and second alternating regions of dielectric material received between the conductive lines laterally across the array, the first regions comprising a singular void received within solid insulative material between two immediately adjacent of the conductive lines, the second regions being at least in part characterized by an absence of any void space within solid insulative material between two immediately adjacent of the conductive lines.

50. Integrated circuitry comprising an array of conductive lines, comprising:

a plurality of elongated conductive lines received over a substrate, the conductive lines being at least in part characterized by repeating pairs of immediately adjacent conductive lines which are mirror images of one another in lateral cross section along at least a majority of length of the repeating pairs; and

dielectric material received between the conductive lines over the substrate laterally across the array.

51. The integrated circuitry according to claim 50 wherein the dielectric material comprises first and second alternating regions received between the conductive lines laterally across the array, the first regions comprising a singular void received within solid insulative material between two immediately adjacent of the conductive lines, the second regions being at least in part characterized by an absence of any void space within solid insulative material between two immediately adjacent of the conductive lines.

52. The integrated circuitry of claim 51 wherein the first regions are received with each pair between the immediately adjacent conductive lines which are mirror images of one another.

CLAIMS:

1. A method of forming a plurality of conductive lines in the fabrication of integrated circuitry, comprising:

forming a trench into a damascene material received over a substrate, the trench having first and second opposing trench sidewalls, the first trench sidewall being longitudinally elongated to comprise a longitudinal contour of a first sidewall of one of the plurality of conductive lines being formed, the second trench sidewall being longitudinally elongated to comprise a longitudinal contour of a first sidewall of another of the plurality of conductive lines being formed;

depositing conductive material to within the trench to span between the first and the second trench sidewalls; and

etching through the conductive material longitudinally along and elevationally between the first and second trench sidewalls to form the longitudinal contour of a second sidewall of the one conductive line within the trench and to form the longitudinal contour of a second sidewall of the another conductive line within the trench.

2. The method of claim 1 comprising forming no more than two conductive lines within the trench.

3. The method of claim 1 wherein a minimum space between the longitudinal contours within each of the one and the another conducive lines is no greater than 20 nanometers.

4. The method of claim 1 wherein the etching forms the one conductive line and the another conductive line to be of the same shape in lateral cross section along at least a majority of length of the one conductive line and the another conductive line.

5. The method of claim 4 wherein the etching forms the one conductive line and the another conductive line to be mirror images of one another in lateral cross section along at least the majority of length of the one conductive line and the another conductive line.

6. The method of claim 1 wherein the conductive material is deposited to overfill the trench, and further comprising planarizing the conductive material back at least to the damascene material prior to the etching through the conductive material.

7. A method of forming a pair of conductive lines in the fabrication of integrated circuitry, comprising:

forming a trench into a damascene material received over a substrate, the trench having first and second opposing trench sidewalls and a minimum width there-between which is at least about $3W_m$ where W_m is the minimum width of the conductive lines being formed, the first trench sidewall being longitudinally elongated to comprise a longitudinal contour of a first sidewall of a first of the pair of conductive lines being formed, the second trench sidewall being longitudinally elongated to comprise a longitudinal contour of a first sidewall of a second of the pair of conductive lines being formed;

depositing conductive material to within the trench to span between the first and second trench sidewalls; and

etching through the conductive material longitudinally along and elevationally between the first and second trench sidewalls to form the longitudinal contour of a second sidewall of the first conductive line within the trench and to form the longitudinal contour of a second sidewall of the second conductive line within the trench.

8. The method of claim 7 wherein the trench minimum width is about $3W_m$.

9. The method of claim 8 wherein the integrated circuitry is fabricated using photolithography and W_m is F, where F is the minimum photolithographic feature size with which the integrated circuitry is fabricated.

10. The method of claim 8 wherein the integrated circuitry is fabricated using photolithography and W_m is less than F, where F is the minimum photolithographic feature size with which the integrated circuitry is fabricated.

11. The method of claim 7 wherein the etching forms the first and second conductive lines to be of the same shape in lateral cross section along at least a majority of length of the first and second conductive lines.

12. The method of claim 11 wherein the trench minimum width is about 1.5P, where P is pitch of the first and second conductive lines.

13. The method of claim 11 wherein the etching forms the first and second conductive lines to be mirror images of one another in lateral cross section along at least a majority of length of the first and second conductive lines.

14. The method of claim 11 wherein the trench minimum width is about $3W_m$.

15. The method of claim 14 wherein the trench minimum width is about 1.5P, where P is pitch of the first and second conductive lines.

16. The method of claim 7 wherein the etching forms a space within the trench between the first and second conductive lines, and further comprising filling the space with a dielectric material.

17. The method of claim 16 wherein the dielectric material comprises a void between the first and second conductive lines.

18. The method of claim 7 wherein the etching forms a space within the trench between the first and second conductive lines, the space being equal to about W_m in lateral cross section.

19. The method of claim 7 wherein the conductive material within the trench comprises a conductive liner comprising a first composition and a conductive fill material comprising a different second composition received over the conductive liner.

20. The method of claim 19 wherein the etching forms each of the first and second conductive lines to have the first sidewall of the first composition and a base layer of the first composition, the etching forming the second sidewall above the base layer of each of the first and second conductive lines to be of the second composition.

21. The method of claim 19 wherein second composition is of higher electrical conductivity than the first composition.

22. A method of forming a plurality of parallel conductive lines in the fabrication of integrated circuitry, comprising:

forming a plurality of parallel oriented trenches into a damascene material received over a substrate, the trenches individually having first and second opposing trench sidewalls and a minimum width there-between which is at least about $3W_m$ where W_m is the minimum width of a pair of conductive lines being formed within each trench, the first trench sidewall of each trench being longitudinally elongated to comprise a longitudinal contour of a first sidewall of a first of the pair of conductive lines being formed within each trench, the second trench sidewall being longitudinally elongated to comprise a longitudinal contour of a second sidewall of a second of the pair of conductive lines being formed within each trench;

depositing conductive material to within each trench to span between the first and second trench sidewalls of each trench; and

etching through the conductive material longitudinally along and elevationally between the first and second trench sidewalls to form the longitudinal contour of a second sidewall of the first conductive line within each trench and to form the longitudinal contour of a second sidewall of the second conductive line within each trench.

23. The method of claim 22 wherein W_m is no greater than 20 nanometers.

24. The method of claim 22 wherein the etching is conducted through openings between masking blocks, the masking blocks individually spanning between and partially masking respective immediately adjacent of two of the trenches.

25. The method of claim 22 wherein the etching forms the first and second conductive lines to be mirror images of one another in lateral cross section along at least a majority of length of the first and second conductive lines.

26. The method of claim 22 comprising forming the damascene material to comprise insulative material at least some of which remains a part of the finished integrated circuitry.

27. The method of claim 22 comprising forming the damascene material to comprise at least one of semiconductive material and conductive material.

28. A method of forming a pair of conductive lines in the fabrication of integrated circuitry, comprising:

forming a trench into a damascene material received over a substrate, the trench having first and second opposing trench sidewalls which span an elevation of the damascene material, the first trench sidewall being longitudinally elongated to comprise a longitudinal contour of a first sidewall of a first of a pair of conductive lines being formed within the trench, the second trench sidewall being longitudinally elongated to comprise a longitudinal contour of a first sidewall of a second of the pair of conductive lines being formed within the trench;

depositing conductive material to within the trench to span between the first and second trench sidewalls;

recessing the conductive material within the trench and forming a first trench-wall and a second trench-wall over the recessed conductive material, the first trench-wall and the second trench-wall being received within said elevation of the damascene material;

forming a first etch mask against the first trench-wall and a second etch mask against the second trench-wall; and

using the first etch mask and the second etch mask as masking, etching through the conductive material longitudinally between the first and second trench sidewalls to form the longitudinal contour of a second sidewall of the first conductive line within the trench and to form the longitudinal contour of a second sidewall of the second conductive line within the trench.

29. A method of forming a plurality of parallel conductive lines in the fabrication of integrated circuitry, comprising:

forming a plurality of parallel oriented trenches into a damascene material received over a substrate, the trenches individually having first and second opposing trench sidewalls and a minimum width there-between which is at least about $3W_m$ where W_m is the minimum width of a pair of conductive lines being formed within each trench, the first and second opposing trench sidewalls spanning an elevation of the damascene material, the first trench sidewall of each trench being longitudinally elongated to comprise a longitudinal contour of a first sidewall of a first of the pair of conductive lines being formed within each trench, the second trench sidewall being longitudinally elongated to comprise a longitudinal contour of a second sidewall of a second of the pair of conductive lines being formed within each trench;

depositing conductive material to within each trench to span between the first and second trench sidewalls of each trench;

recessing the conductive material within each trench and forming a first trench-wall and a second trench-wall over the recessed conductive material within each trench, the first trench-wall and the second trench-wall within each trench being received within said elevation of the damascene material;

forming a first etch mask against the first trench-wall and a second etch mask against the second trench-wall within each trench; and

using the first etch masks and the second etch masks as masking, etching through the conductive material longitudinally between the first and second trench sidewalls to form the longitudinal contour of a second sidewall of the first conductive line within each trench and to form the longitudinal contour of a second sidewall of the second conductive line within each trench.

30. A method of forming a pair of conductive lines in the fabrication of integrated circuitry, comprising:

forming a trench into a damascene material received over a substrate;

depositing conductive material over the damascene material and to within the trench to overfill the trench;

removing the conductive material back at least to the damascene material to leave at least some of the conductive material remaining in the trench; and

longitudinally etching through the conductive material within the trench to form first and second conductive lines within the trench which are mirror images of one another within the trench in lateral cross section along at least a majority of length of the first and second conductive lines.

31. A method of forming an array of conductive lines in the fabrication of integrated circuitry, comprising:

forming a plurality of elongated conductive lines over a substrate; and

providing first and second alternating regions of dielectric material between the conductive lines laterally across the array, the first regions comprising a singular void received within solid insulative material between two immediately adjacent of the conductive lines, the second regions being at least in part characterized by an absence of any void space within solid insulative material between two immediately adjacent conductive lines.

32. The method of claim 28 wherein the first trench-wall is formed to comprise an upper portion of the first trench sidewall and the second trench-wall is formed to comprise an upper portion of the second trench sidewall.

33. The method of claim 28 wherein the first and second etch masks are formed to comprise an interconnected ring.

34. The method of claim 28 wherein the first and second conductive lines are initially formed to comprise an interconnected ring of the conductive material, and further comprising breaking the ring of the conductive material in at least two locations to separate the first and second conductive lines from being interconnected.

35. The method of claim 28 wherein at least a majority of each of the first and second etch masks remains as part of the finished integrated circuitry.

36. The method of claim 28 wherein forming the first and second etch masks comprises:

depositing a spacer-forming layer to less than fill remaining volume of the trench after the recessing; and

anisotropically etching the spacer-forming layer to form the first and second etch masks to respectively comprise a sidewall spacer received against the first trench-wall and against the second trench-wall.

37. The method of claim 36 wherein the anisotropic etching is conducted without any mask being received over the spacer-forming layer.

38. The method of claim 36 wherein the first trench-wall is formed to comprise an upper portion of the first trench sidewall and the second trench-wall is formed to comprise an upper portion of the second trench sidewall.

39. The method of claim 36 wherein the first and second conductive lines are initially formed to comprise an interconnected ring of the conductive material, and further comprising breaking the ring of the conductive material in at least two locations to separate the first and second conductive lines from being interconnected.

40. The method of claim 36 wherein at least a majority of each of the first and second etch masks remains as part of the finished integrated circuitry.

41. The method of claim 28 wherein, the first trench-wall is formed to comprise an upper portion of the first trench sidewall and the second trench-wall is formed to comprise an upper portion of the second trench sidewall;

the forming of the first and second etch masks comprises:

depositing a spacer-forming layer to less than fill remaining volume of the trench after the recessing; and

anisotropically etching the spacer-forming layer to form the first and second etch masks to respectively comprise a sidewall spacer received against the first trench-wall and against the second trench-wall;

the first and second conductive lines are initially formed to comprise an interconnected ring of the conductive material, and further comprising breaking the ring of the conductive material in at least two locations to separate the first and second conductive lines from being interconnected; and

at least a majority of each of the first and second etch masks remains as part of the finished integrated circuitry.

42. The method of claim 29 wherein the first trench-wall is formed to comprise an upper portion of the first trench sidewall of each trench and the second trench-wall is formed to comprise an upper portion of the second trench sidewall of each trench.

43. The method of claim 29 wherein forming the first and second etch masks comprises:

depositing a spacer-forming layer to less than fill remaining volume of each of the trenches after the recessing; and

anisotropically etching the spacer-forming layer to form the first and second etch masks to respectively comprise a sidewall spacer received against the first trench-wall and against the second trench-wall.

44. The method of claim 29 wherein the first and second etch masks are formed to comprise an interconnected ring.

45. The method of claim 29 wherein the first and second conductive lines are initially formed to comprise an interconnected ring of the conductive material within each trench, and further comprising breaking the ring of the conductive material within each trench in at least two locations to separate the first and second conductive lines from being interconnected within each trench.

46. The method of claim 29 wherein at least a majority of each of the first and second etch masks remains as part of the finished integrated circuitry.