

ABSTRACT

SELF-ALIGNED HALO PROCESS FOR REDUCING JUNCTION CAPACITANCE

A method for forming an LDD structure using a self-aligned halo process is described. A gate silicon oxide layer is provided over the surface of a semiconductor substrate. A gate electrode is formed overlying the gate silicon oxide layer. A silicon oxide layer is grown on the sidewalls of the gate electrode and silicon nitride spacers are formed on the sidewalls of the silicon oxide layer. First ions are implanted into the semiconductor substrate and the substrate is annealed whereby heavily doped source and drain regions are formed within the semiconductor substrate not covered by the gate electrode and the silicon oxide and silicon nitride spacers. An oxide layer is grown over the heavily doped source and drain regions. Thereafter, the silicon nitride spacers are removed. Second ions are implanted to form lightly doped regions in the semiconductor substrate not covered by the oxide layer. Third ions are implanted to form a halo having opposite dosage and a deeper junction than the lightly doped regions. An insulating layer is deposited over the surface of the substrate. An opening is provided through the insulating layer to one of the source and drain regions. A conducting layer is deposited overlying the insulating layer and within the opening and patterned completing the fabrication of the integrated circuit device.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)