ABSTRACT OF THE DISCLOSURE

It is intended to provide a semiconductor device which comprises an SGT-based, highly-integrated, high-speed, at least two-stage CMOS inverter cascade circuit configured to allow a pMOS SGT to have a gate width two times greater than that of an nMOS SGT. A semiconductor device of the present invention comprises a CMOS inverter cascade circuit having at least two-stage CMOS inverter, wherein: a first CMOS inverter includes two pMOS SGT arranged at respective ones of an intersection of the 1st row and the 1st column and an intersection of the 2nd row and the 1st column, and an nMOS SGT arranged at an intersection of the 1st row and the 2nd column; and a second CMOS inverter includes two pMOS SGT arranged at respective ones of an intersection of the 1st row and the 3rd column and an intersection of the 2nd row and the 3rd column, and an nMOS SGT arranged at an intersection of the 2nd row and the 2nd column. An output terminal line is connected to an input terminal line, wherein the output terminal line is arranged to interconnect a drain diffusion layer of each of the two SGTS at respective ones of the intersection of the 1st row and the intersection of the 2nd row and the 1st column and the 1st column, and a drain diffusion layer of the SGT at the intersection of the 1st row and the 2nd column, through an island-shaped semiconductor lower layer, and the an input terminal line is arranged to interconnect a gate of each of the two SGTs at respective ones of the intersection of the 1st row and the 3rd column and the intersection of the 2nd row and the 3rd column, and a gate of the SGT at and the intersecting of the 2nd row and 2nd column.