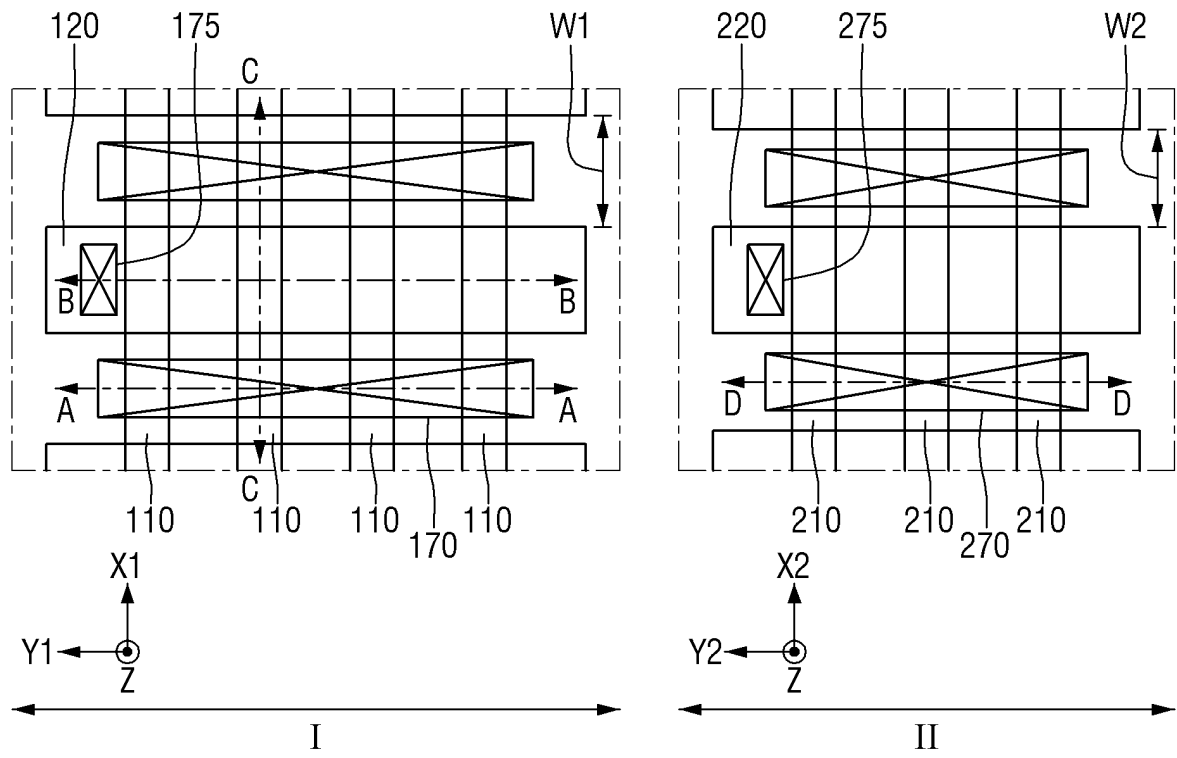


FIG. 1



$$\begin{array}{cc} & 205 \\ & \swarrow \quad \searrow \\ 206 & 207 \end{array}$$


FIG. 3

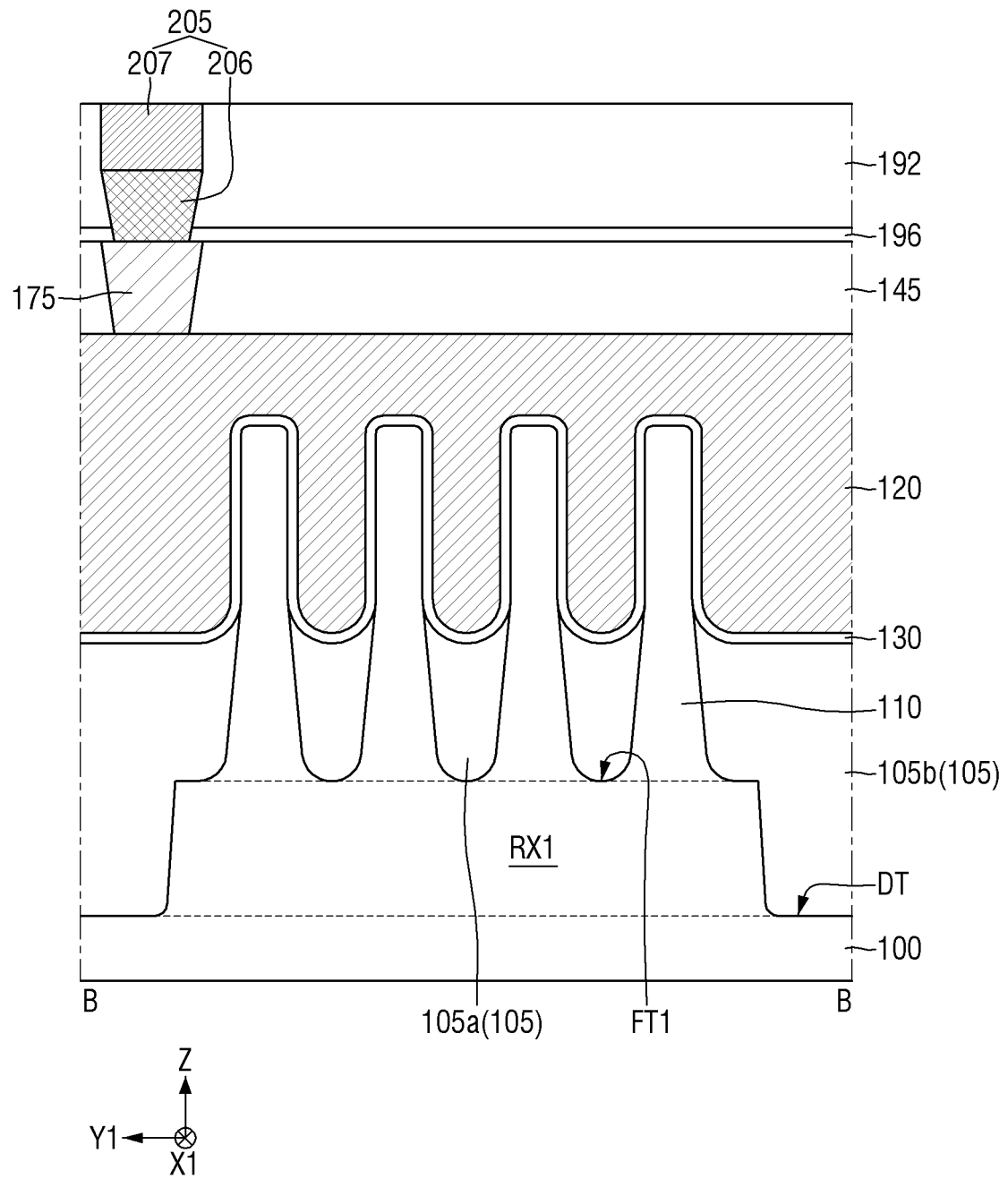


FIG. 4

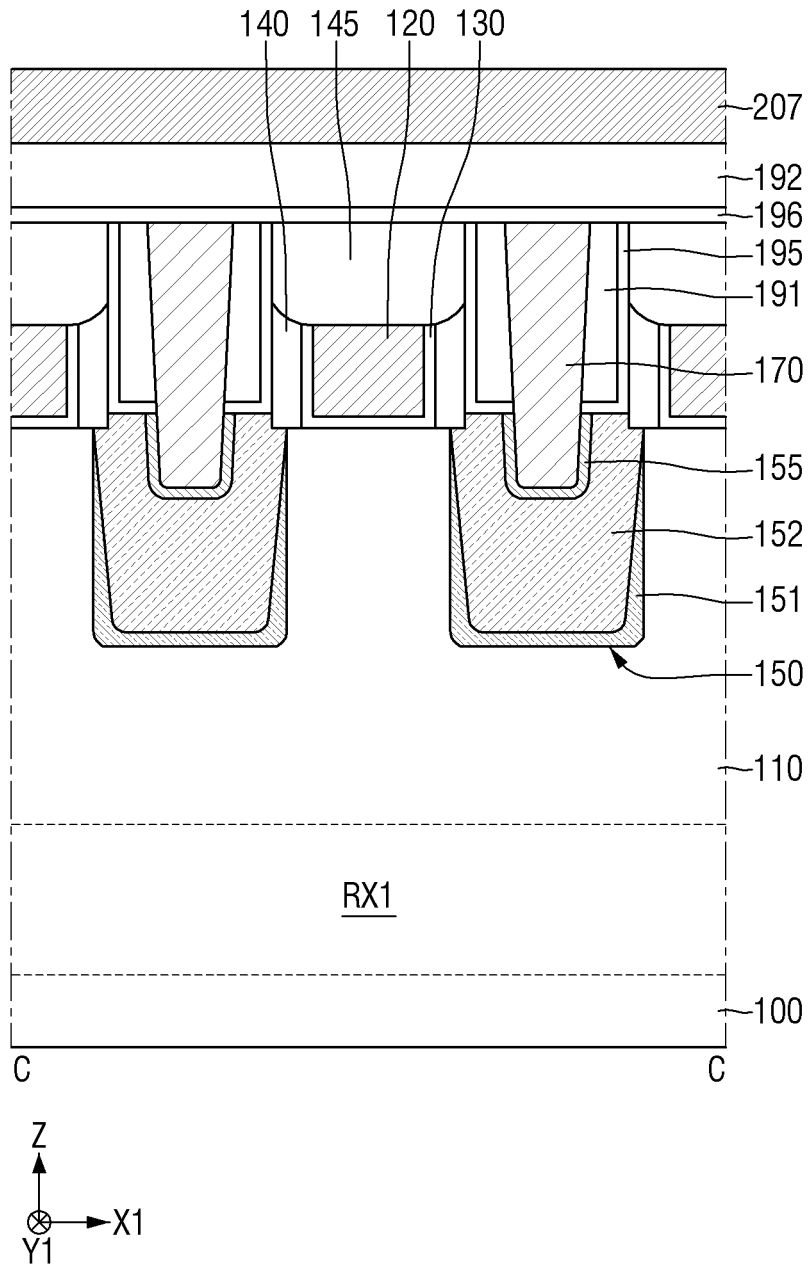


FIG. 5

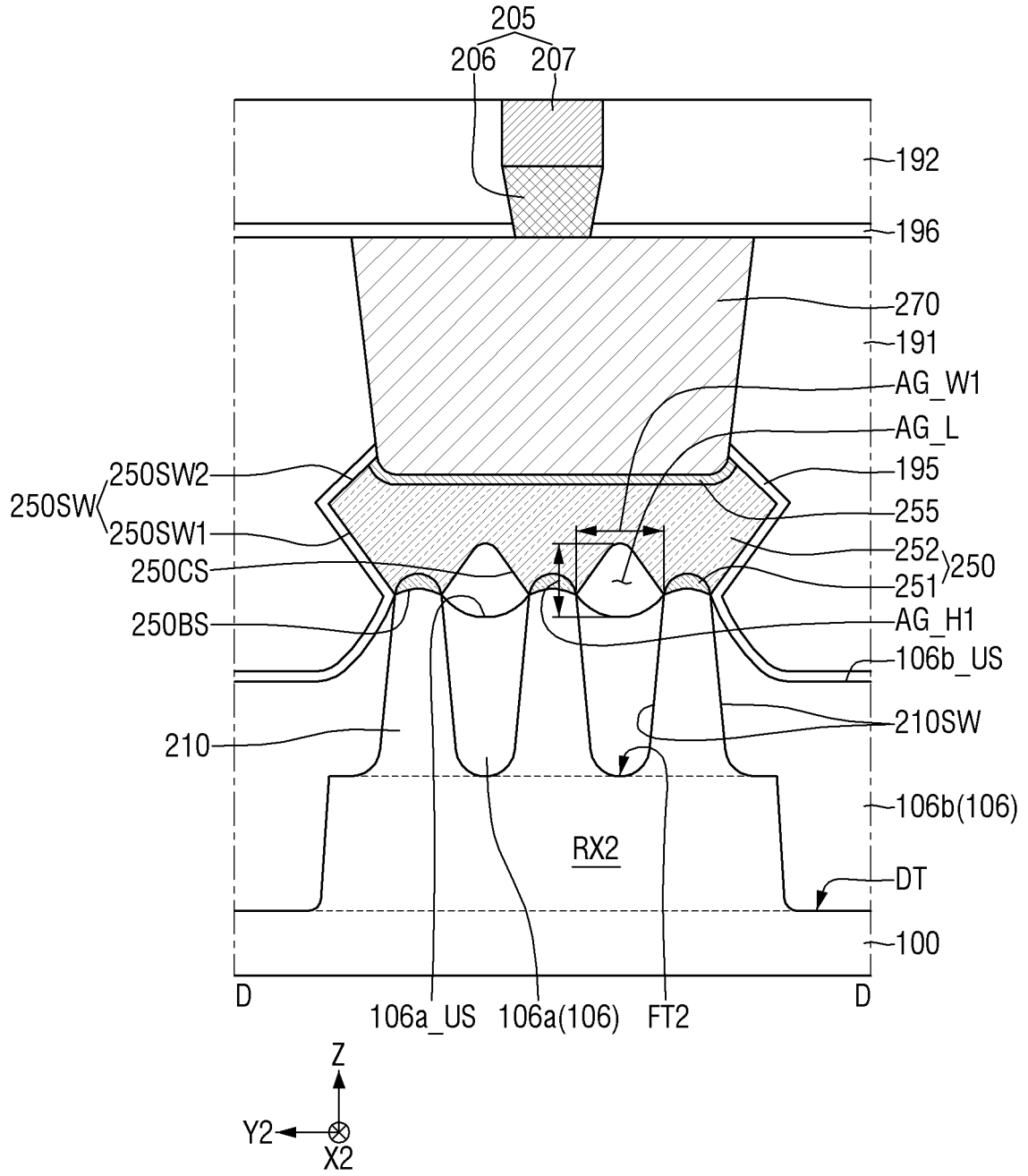


FIG. 6

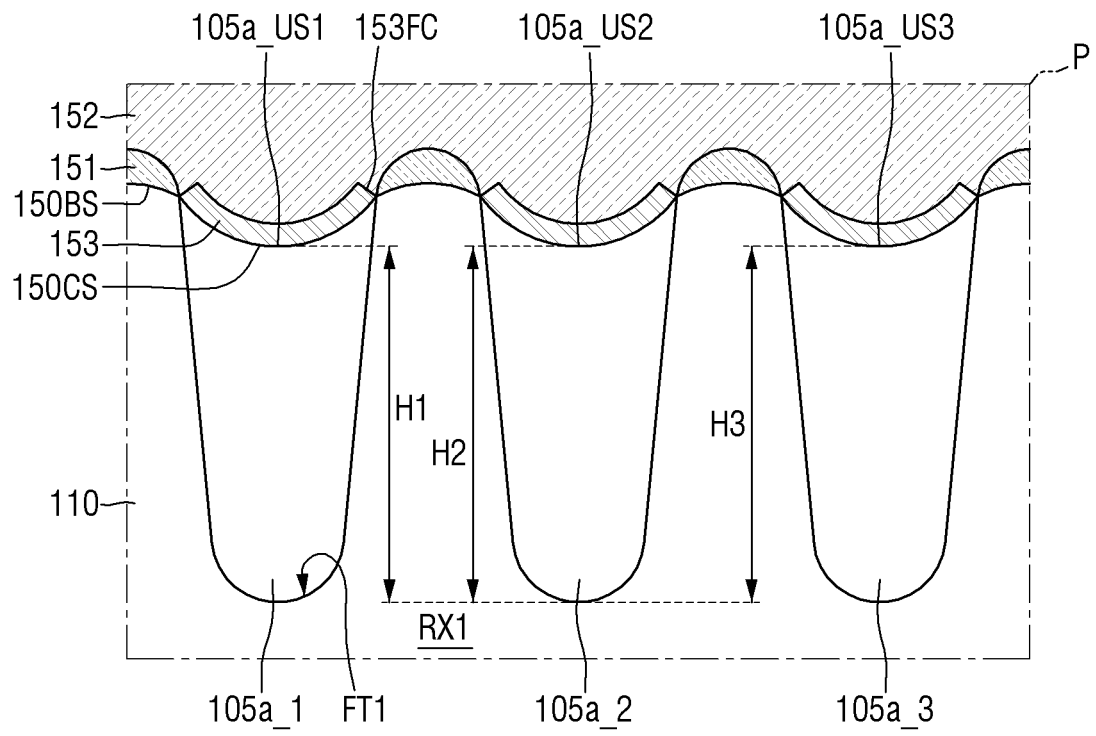


FIG. 7

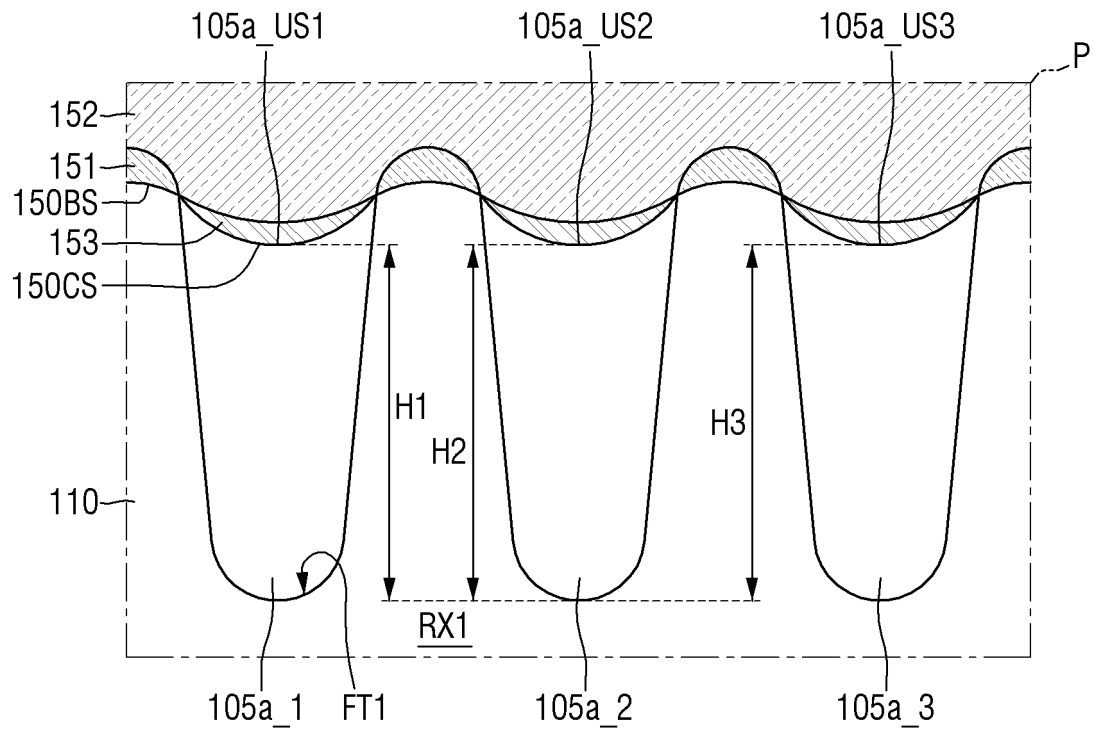


FIG. 8

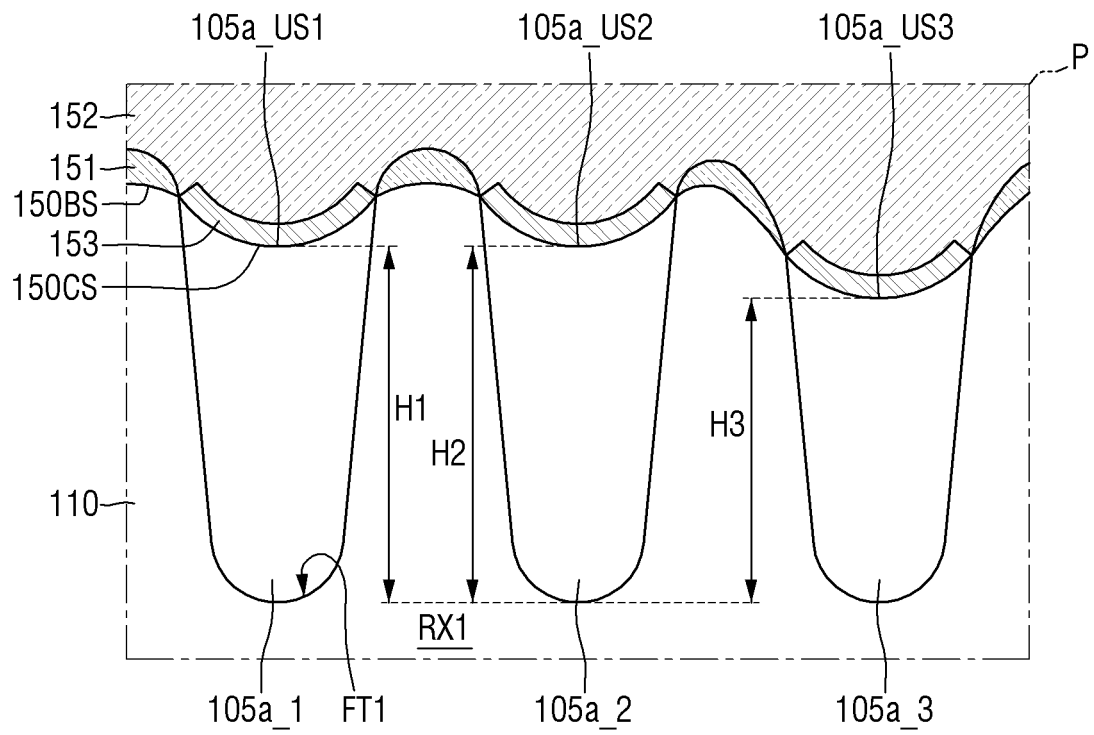


FIG. 9

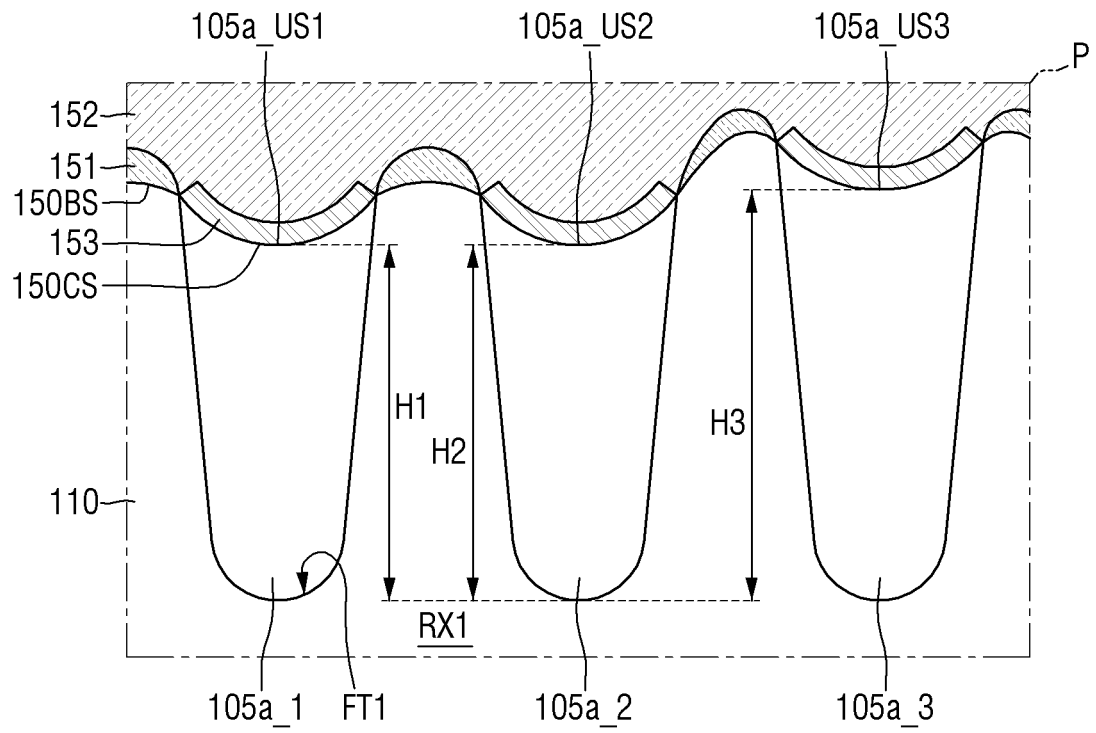


FIG. 10

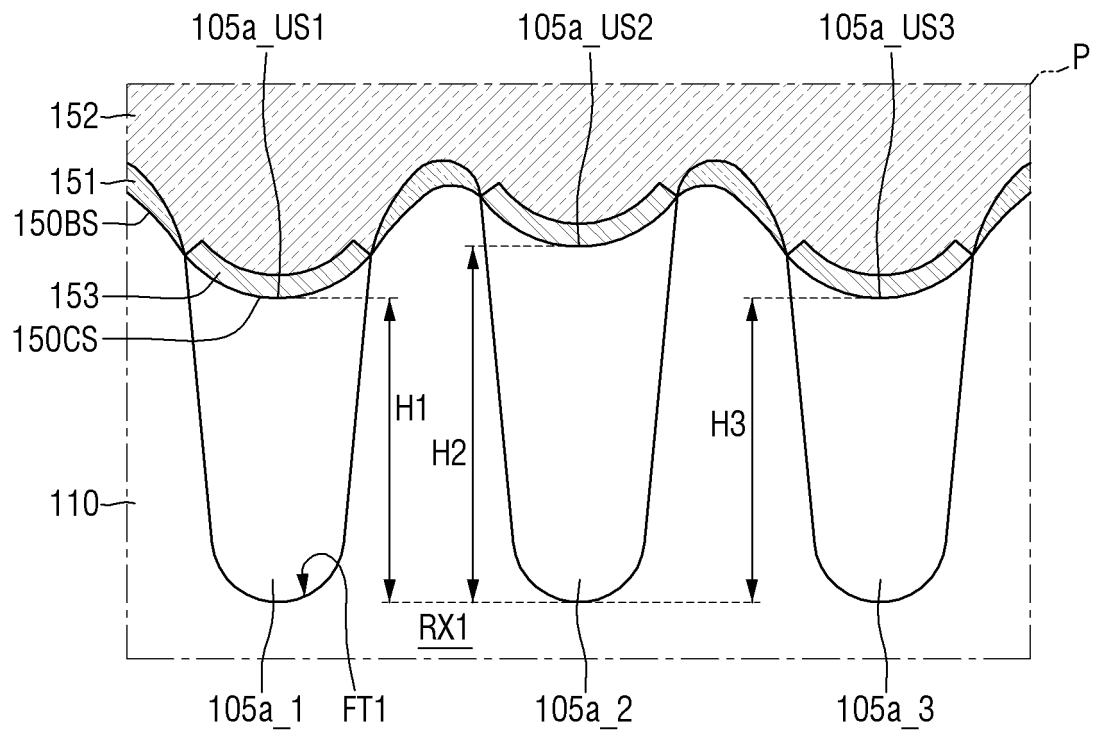


FIG. 11

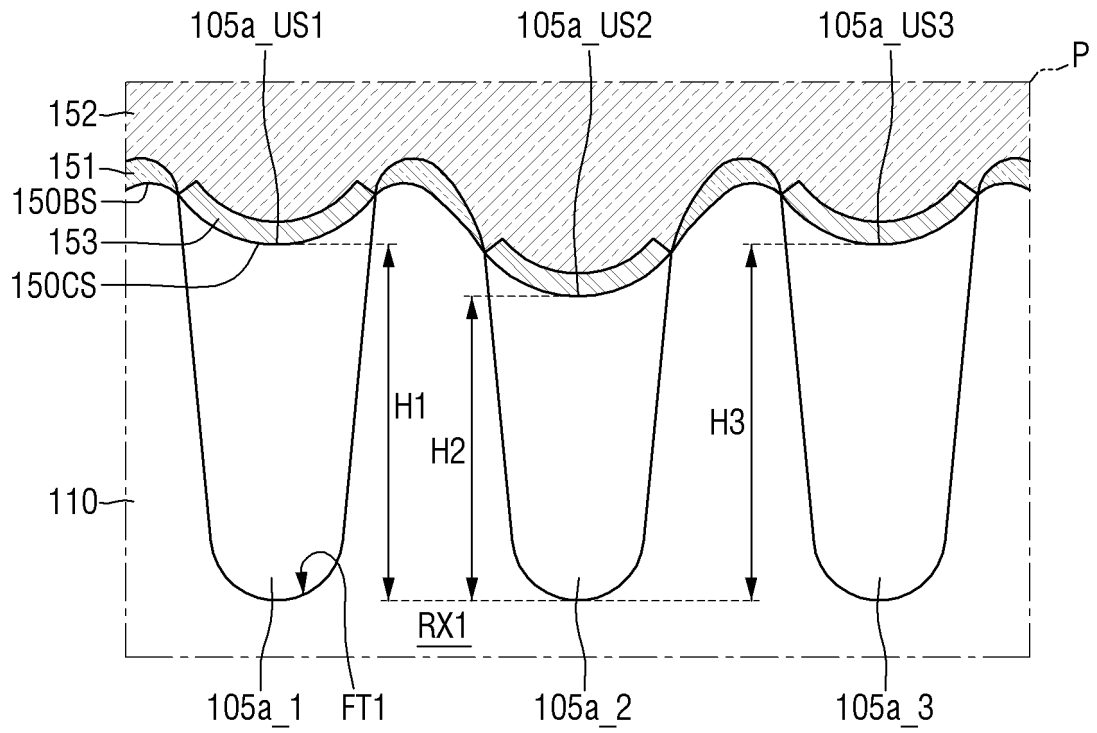


FIG. 12

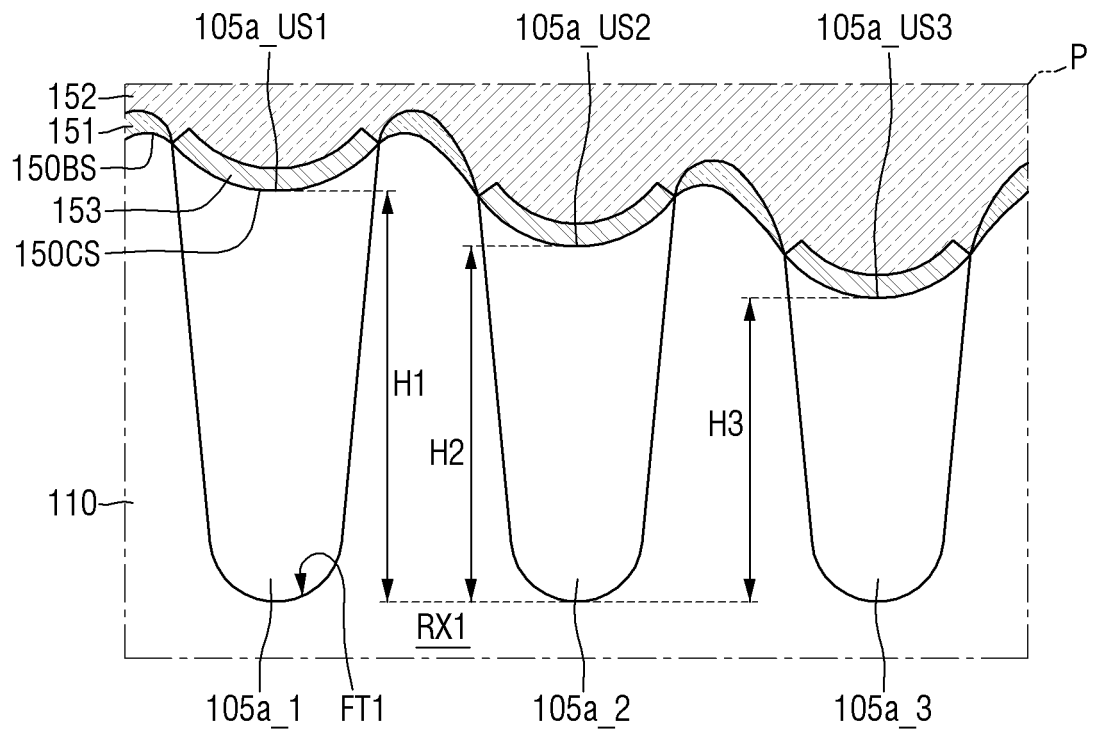
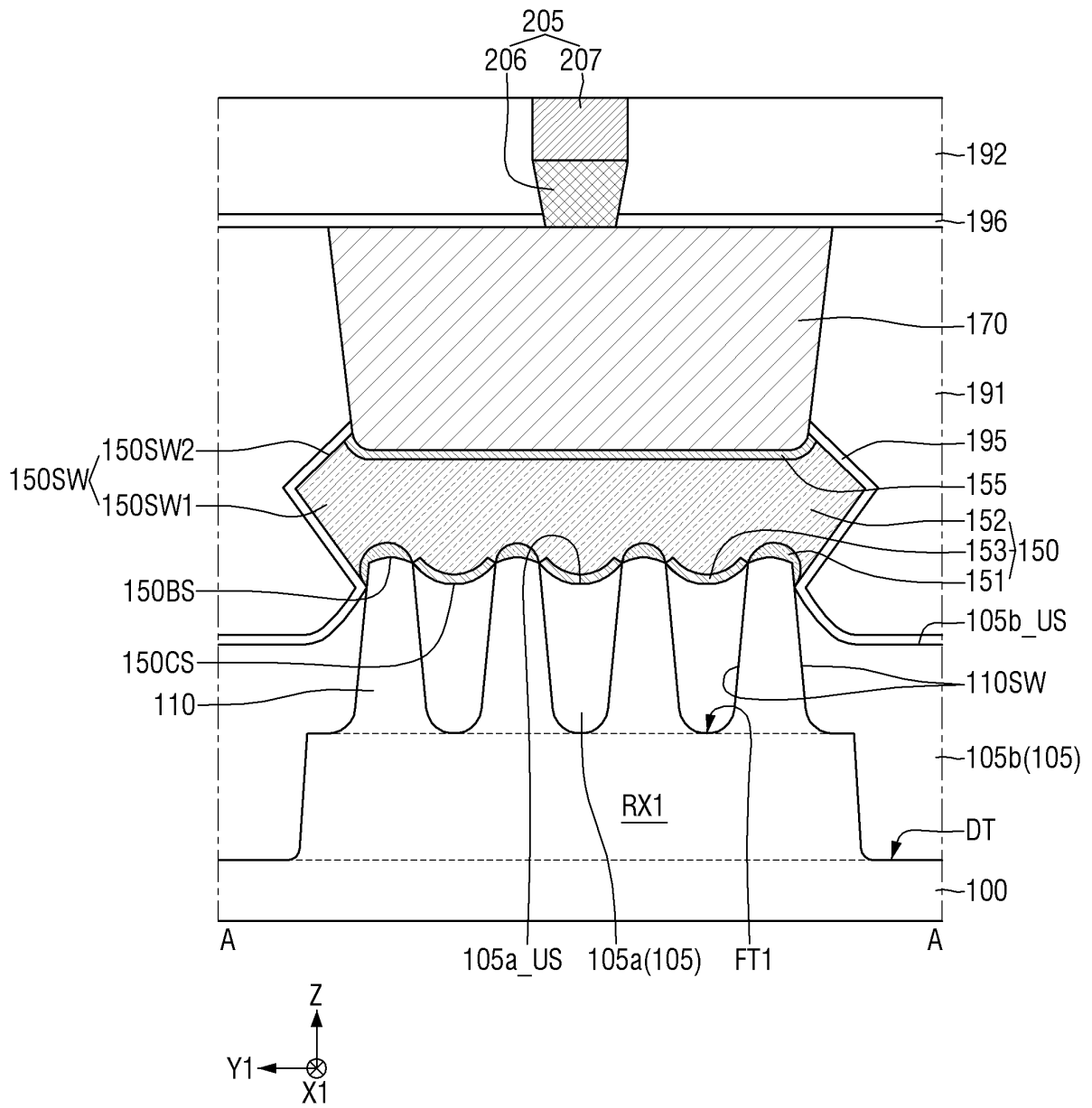


FIG. 13



$$\begin{array}{cc} & 205 \\ & \swarrow \quad \searrow \\ 206 & 207 \end{array}$$


FIG. 15

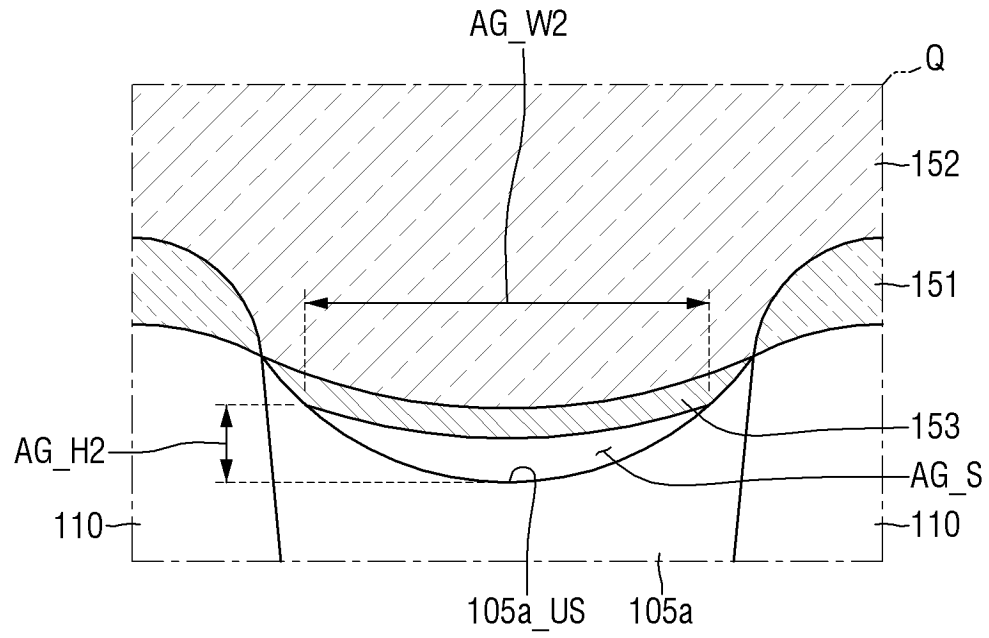


FIG. 16

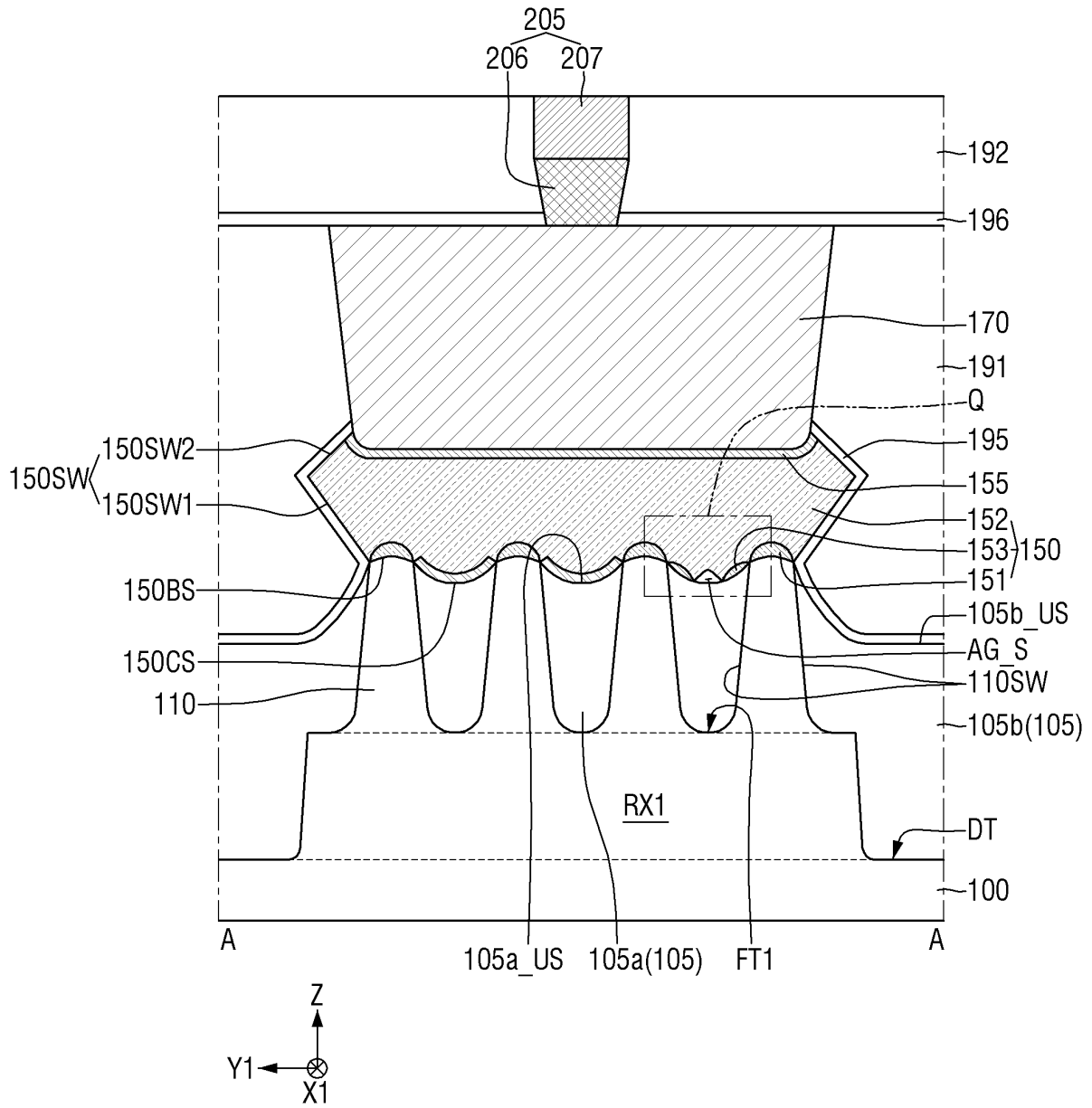
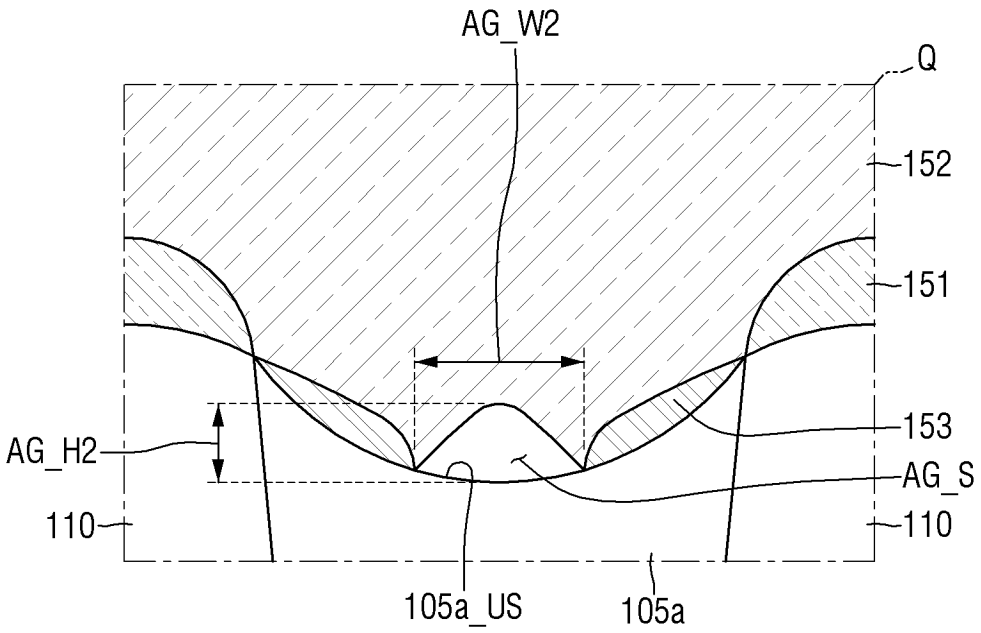


FIG. 17



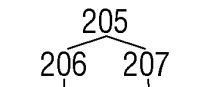
$$\begin{array}{cc} & 205 \\ & \swarrow \quad \searrow \\ 206 & 207 \end{array}$$


FIG. 19

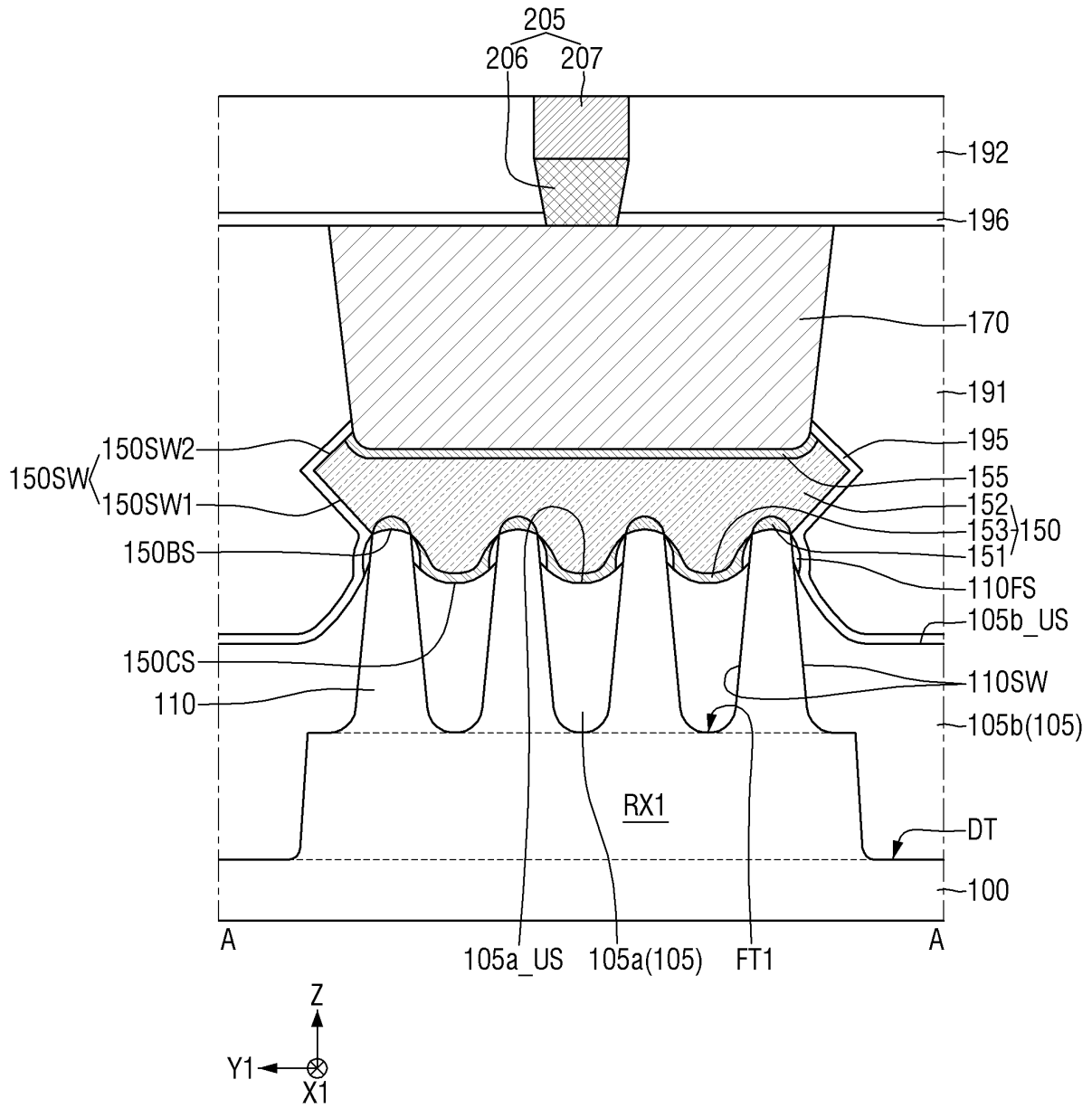


FIG. 20

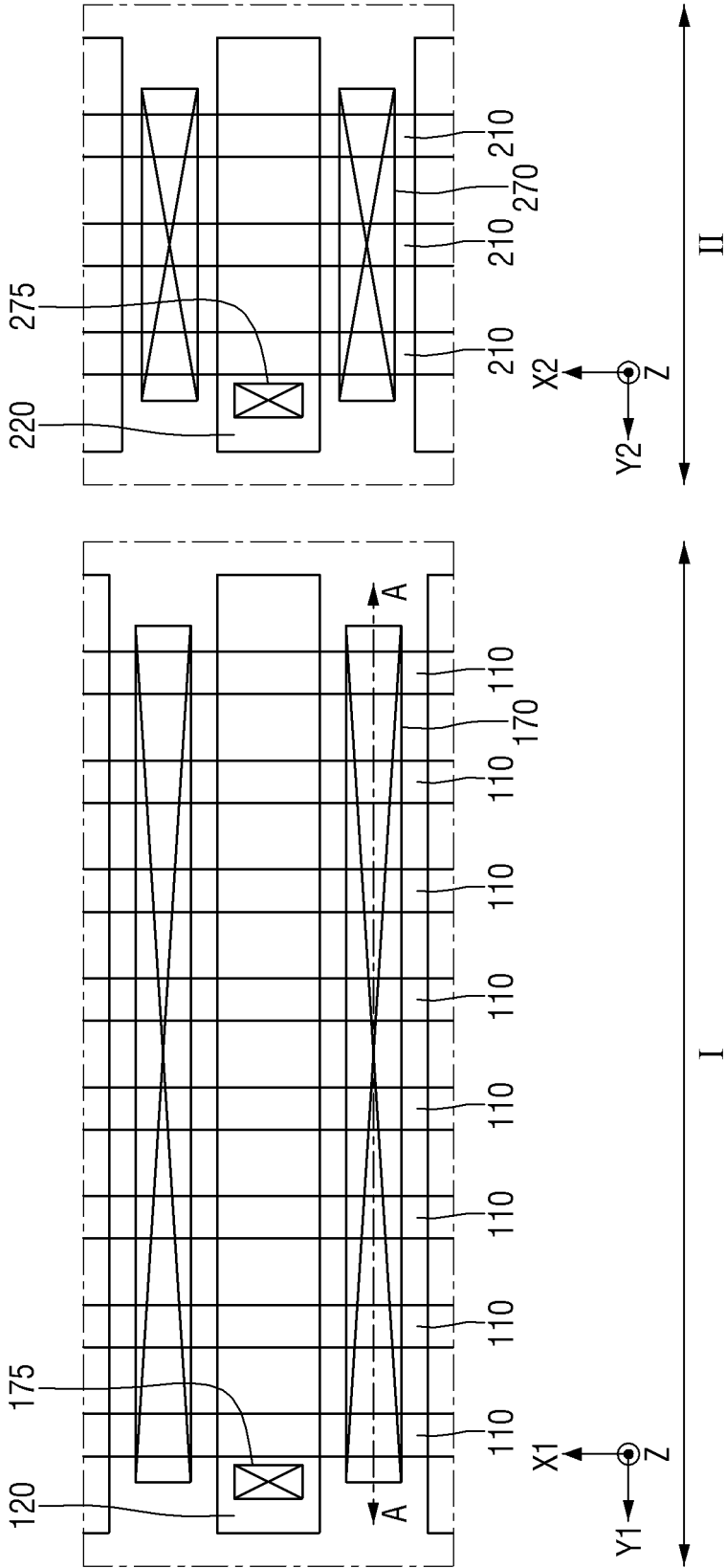


Figure 1 is a cross-sectional view of a semiconductor device 100. The device includes a substrate 110 with a top layer 192 and a bottom layer 196. A central region 170 is filled with a material 191. A series of vertical structures 105a(105) and 105b(105) are formed on the top layer 192. A dashed line 110 indicates a boundary. A coordinate system (X1, Y1, Z) is shown at the bottom right.

FIG. 22

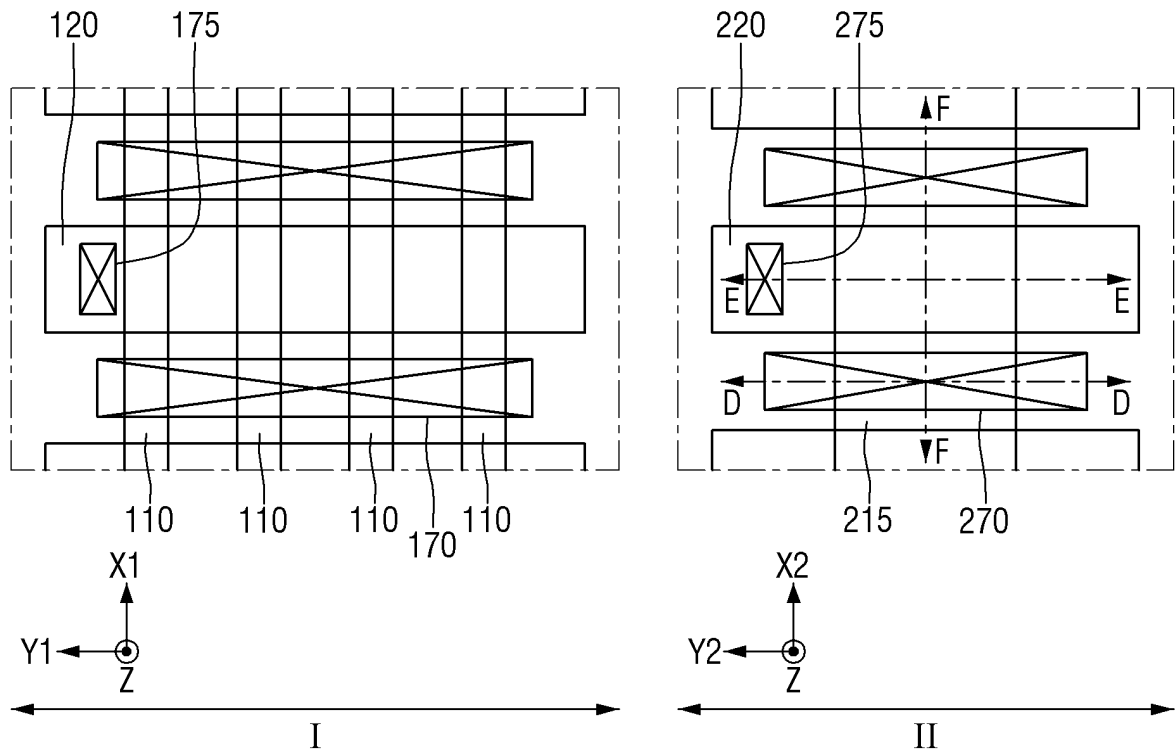


FIG. 23

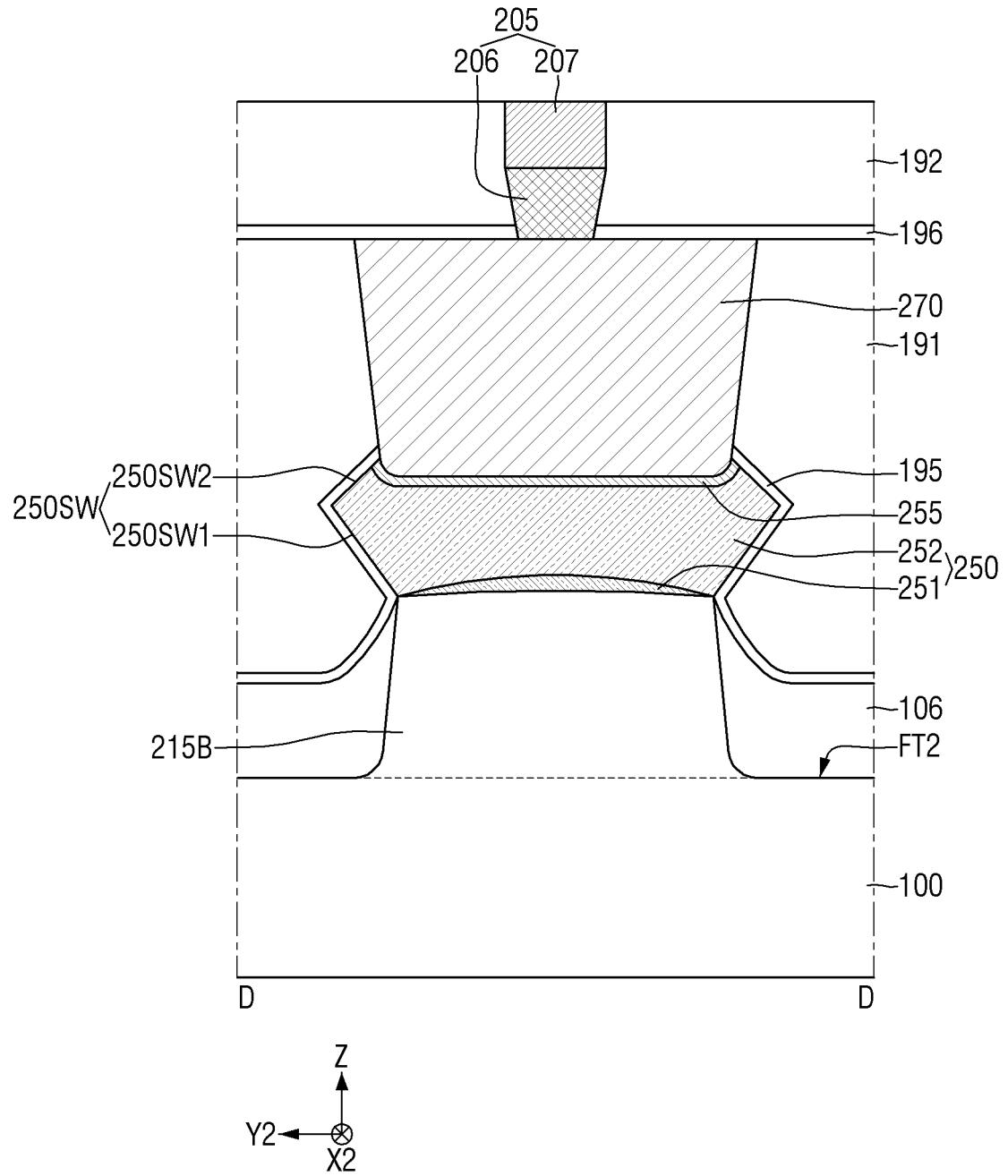


FIG. 24

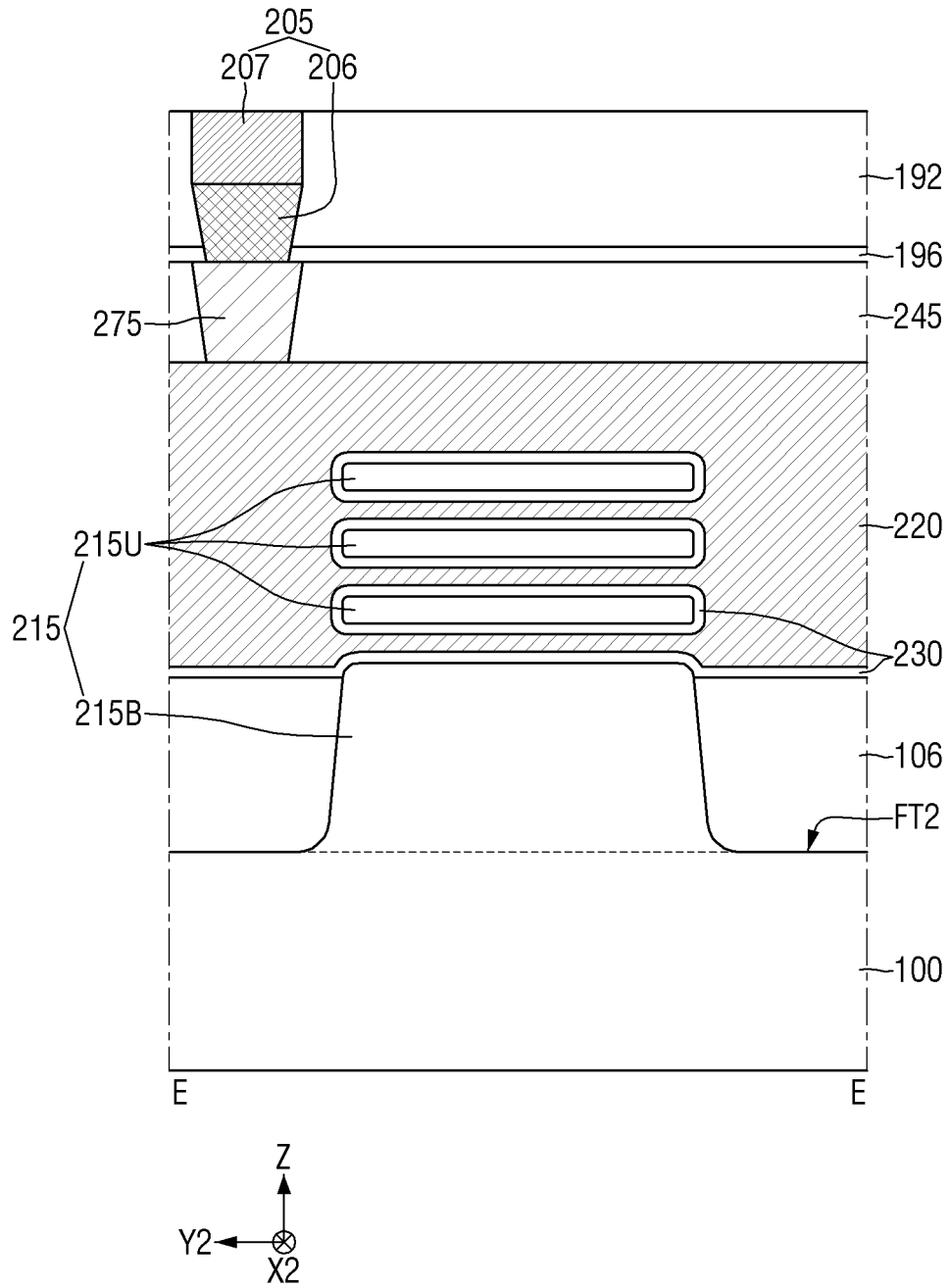


FIG. 25

