A NEW PROCESS OF DUAL DAMASCENE STRUCTURE

BACKGROUND OF THE INVENTION

(1) Field of the Invention.

The present invention relates to the field of semiconductor manufacturing, and more specifically to the formation of a dual damascene shaped metal interconnect.

(2) Description of the Prior Art.

The present invention relates specifically to the damascene process that is used for the formation of semiconductor surfaces. Damascene derives its name from the ancient art involving inlaying metal in ceramic or wood for decorative purposes. In Very Large-Scale Integrated circuit applications, the damascene process refers to a similar structure.

The damascene process has been demonstrated on a number of applications. The most commonly applied process is first metal or local interconnects. Some early Damascene structures have been achieved using Reactive Ion Etching (RIE) but Chemical Mechanical Planarization (CMP) is used exclusively today. Metal

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interconnects using damascene of copper and of aluminum is also being explored.

Fig. 7 gives an overview of the Damascene process, as follows:

Fig. 7a shows the metal plug formed after the surface planarization.

Fig. 7b shows the deposition of the Inter Level Dielectric.

Fig. 7c shows the formation of the trenches for metal lines.

Fig. 7d shows the deposition of metal to fill the trenches.

Fig. 7e shows the removal of the excess metal from the surface.

Referring now specifically to Fig. 7a, there is shown the formation of a metal via plug 10 within the semiconductor substrate 14. Any micro-scratch present on the surface 12 will fill with metal during subsequent metal deposition and can cause electrical shorts between adjacent via plugs 10 or between electrical lines deposited on top of surface 12. To remove the damascene residue and to reduce the scratch count on the surface 12, surface 12 is polished and buffed after the metal plugs 10 have been deposited.

Fig. 7b shows the deposition of the Inter Level Dielectric (ILD) 16 which can be deposited using Plasma Enhanced CVD (PECVD) techniques. Dielectric 16 can, for instance, be SiO_2.

Fig. 7c shows the formation of the trenches 18 for the metal lines, these trenches can be formed using Reactive Ion Etching (RIE) techniques.

Fig. 7d shows the deposition of metal 20 to fill the trenches 18; this process can use either the CVD or a metal flow process. The excess metal on the surface is removed using the CMP process, see Fig. 7e, and a planar structure 26 with metal inlays 22 in the dielectric 16 is achieved. The surface 26 created in this manner is planarized using CMP technology.

As device dimensions decrease, aluminum metalization used for the via plugs and/or for the metal conducting lines, encounters the problem of high resistivity and lower electromigration resistance. Copper thin films offer low resistivity and show good electromigration resistance. They would therefore appear to be attractive as Very Large Scale Integrated conductor materials, especially as device dimensions approach deep-submicron sizes. A dry-etching process for Cu films has not been successfully developed which is one chief

reason that Cu has not been widely considered for such applications. Also, wet-etch and sputter etch cannot pattern copper due to the non-volatile copper halides compounds. The present invention teaches a dual damascene structure that, combined with CMP, is required to pattern copper.

US 5,71,6 1 0 (Cleeves) shows a method of forming an opening for an inter-connect using a disposable post 221, see Figs. 2A - 2E. This patent shows the general idea of disposable posts, but does not show the exact steps to form the invention's dual damascene structure.

US 5,635,423(Huang), US 5,736,457(Zhao), US 5,741,626(Jain), US 5,677,244(Venkatraman), and US 5,705,430(Avanzino et al.) show a dual damascene process.

SUMMARY OF THE INVENTION

The principle objective of the present invention is to decrease the electrical resistivity and to increase the electromigration resistance of electrical interconnects.

Another objective of the present invention is to avoid the application of high-dielectric materials in forming electrical interconnects.

Yet another objective of the present invention is to avoid the use of time-etch in forming electrical interconnects.

Yet another objective of the present invention is to assure good interconnect metal profile in forming electrical interconnects.

Yet another objective of the present invention is to assure good interconnect metal thickness in forming electrical interconnects.

According to the present invention, a method is provided for forming a dual damascene "T" shaped interconnect by first forming a "T" shaped temporary post, than forming an insulating layer around the top part of the post, than removing the post to form a "T" shaped opening and refilling the opening with metal after which the metal surface is planarized using Chemical Mechanical Planarization.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1 through 6 show the processing steps of the present invention to form a dual damascene structure, as follows:

Fig. 1 shows a via pattern.

Fig. 2 shows a blanket deposition of a silicon layer.

Fig. 3 shows the pattern created in the silicon layer.

Fig. 4 shows the deposition of an Inter Level Dielectric.

Fig. 5 shows the removal of the silicon.

Fig. 6 shows the final creation of the dual shaped interconnect.

Figs. 7a through 7e present an overview of the Prior Art damascene process.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now specifically to Fig. 1, there is shown the deposition and etching of the via pattern 22, the via pattern 22 is created on the surface of a substrate 15. The via pattern 22 is etched into a layer 20, the material used for this layer can be a silicon dioxide (SiO_2) or any other suitable dielectric used within the art of semiconductor manufacturing. This oxide

layer 20 can be deposited using either Low Pressure CVD (LPCVD) or atmospheric CVD (APCVD) or ultrahigh vacuum CVD (UHCVD). All of these deposition techniques rely on the pyrolysis of source gases at high temperatures. At present, LPCVD is the preferred deposition technology for many films because of high deposition rates and excellent film-thickness uniformity. It is also possible, dependent on the semiconductor throughput requirements, to deposit the dielectric layer by using Rapid Thermal Processing (RTP) for the CVD process. For relatively thick layers of dielectric this requires deposition rates in excess of 1000 A^0 per minute in order to reach adequate wafer throughput. The deposition of layer 20 and the etching of openings 22 require semiconductor deposition and etching technology. Layer 20 can be deposited on top of a semiconductor substrate or on top of a base layer (not shown) first formed on top of the semiconductor substrate. This base layer is not limited to being formed on top of a semiconductor substrate but can be formed at any level within the structure of a semiconductor wafer wherein semiconductor devices are being fabricated.

The layer 20 is to be a thicker oxide layer and serves as an interlevel dielectric. This application requires that the oxide is several thousands of angstrom in thickness. An

important requirement also is that the oxide provides good step coverage. The physical parameter indicative of step coverage is the sticking coefficient in the CVD process. A CVD process with a small sticking coefficient provides better step coverage and conformity. This requirement favors the use of tetraethoxysilane (TEOS) or tetraethylorthosilicate and tetramethylcyclotrasiloxane (TMCTS) in the CVD process.

Fig. 2 shows the deposition of a layer 30 of polycrystalline silicon (poly-Si). This layer can also use other amorphous silicon. Poly-Si thin films have many applications in Integrated Circuit technology. The most widely used application of poly-Si is in metal-oxide-semiconductor (MOS) IC's. Heavily doped poly-Si films have been widely used as the gate electrodes and interconnections in MOS circuits. Poly-Si is used because of its compatibility with subsequent high temperature processing, its excellent interface with thermal oxide in that it exhibits low interface state density, its high stability, its ability to be deposited conformally over steep topography and its capability of reacting with the overlaying metal to form silicide structures. For all of these reasons, poly-Si or a semiconductor material of equal or similar characteristics, is an excellent material to use within the present invention.

Fig. 3 shows how the poly-Si is being prepared to serve as a mask. The "T" pattern 41 forms a temporary post that at a subsequent step within the present invention will be filled with a conducting material and form the dual shaped damascene interconnect. The patterning of poly is much easier than the patterning of any other material since poly to SiO_2 has excellent etch selectivity.

Fig. 4 shows the deposition of the inter level dielectric (ILD) 50. This layer 50 is deposited using semiconductor deposition technology, the layer 50 is planarized using CMP down to the level of the poly-Si 41.

Fig. 5 shows the removal of the poly-Si (41, Fig. 4) and the formation of the cavity 60. This "T" shaped cavity or post is the final shape of the interconnect.

Fig. 6 shows the deposition of a barrier 70 after which the "T" shaped cavity 60 (Fig. 5) is filled with copper 72 using Chemical Vapor Deposition techniques. The surface 74 of the structure is, as a final step in the process, planarized using CMP technology.

From the above it is apparent that a structure has been obtained that lends itself to accurate control of its profile due to the processing steps applied and the materials used in creating this profile. It is also clear that this structure lends itself to precise thickness control since its thickness is controlled by the amount and extend that planarization is applied to the top surface of the structure, a process that can be performed without affecting the bulk of the interconnect.

It will be apparent to those skilled in the art, that other embodiments, improvements, details and uses can be made consistent with the letter and spirit of the present invention and within the scope of the present invention, which is limited only by the following claims, construed in accordance with the patent law, including the doctrine of equivalents.

What is claimed is:

1. A method for forming a dual damascene structure within a semiconductor device, comprising the steps of:

securing a semiconductor substrate;

depositing a first layer of dielectric on top of said semiconductor substrate;

forming a via pattern in said first layer of dielectric;

depositing a second layer on top of said first layer of dielectric and said via pattern;

forming a pattern in said second layer;

depositing a layer of inter-level dielectric (ILD) over said pattern in said second layer and over said first layer of dielectric;

planarizing said layer of ILD;

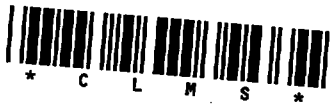
removing said second layer material from said pattern within said second layer and said pattern within said first layer of dielectric;

depositing a barrier within said opening;

depositing copper within said opening; and

planarizing said copper.

2. The method of claim 1 wherein said first layer of dielectric contains oxygen.



3. The method of claim 1 wherein said first layer of dielectric contains tetraethoxysilane (TEOS).

4. The method of claim 1 wherein said first layer of dielectric contains tetramethylcyclotrasiloxane (YMCTS).

5. The method of claim 1 wherein said first layer of dielectric contains tetraethylorthosilicate.

6. The method of claim 1 wherein said first layer of dielectric is deposited using the Rapid Thermal Chemical Vapor Deposition (RTCVD) process.

7. The method of claim 1 wherein said via pattern in said first layer of dielectric is formed using semiconductor exposure and etching technology.

8. The method of claim 1 wherein said second layer contains poly-silicon.

9. The method of claim 1 wherein said grain structure of the second layer is carefully controlled in order to maximize the etch sidewall profile.

10. The method of claim 1 wherein said pattern in said second layer overlays and mates with said via pattern and wherein the dimensions in the plane of deposition of each of the pattern elements or openings of said pattern in said second layer exceeds the dimensions in the plane of deposition of each of the elements or openings of said via pattern in said first layer of dielectric by a considerable margin.

11. The method of claim 1 wherein said pattern in said second layer is formed using semiconductor exposure and etching technology.

12. The method of claim 1 wherein said inter-level dielectric contains silicon dioxide.

13. The method of claim 1 wherein the deposition of said inter-level dielectric uses semiconductor deposition technology.

14. The method of claim 1 wherein patterning said second layer material is performed by plasma etching while adding HB_r/Cl_2 and oxygen-containing gasses to the etch process in order to enhance etch selectivity.

15. The method of claim 1 wherein said barrier within said opening contains Ta.

16. The method of claim 1 wherein said barrier within said opening contains Ta/TaN.

17. The method of claim 1 wherein said barrier within said opening contains TiN.

18. The method of claim 1 wherein said barrier deposition applies high temperature CVD technology.

19. The method of claim 1 wherein said barrier deposition applies high pressure CVD technology.

20. The method of claim 1 wherein a base layer has been formed on the top surface of said substrate.

21. A method for forming a dual damascene structure within a semiconductor device, comprising the steps of:

securing a semiconductor substrate;

forming a base layer on the top surface of said semiconductor substrate;

depositing a first layer of dielectric on top of said base layer thereby creating the plane for the formation of the lower portion of said dual damascene structure;

forming a via pattern in said first layer of dielectric thereby forming the lower portion of said dual damascene structure;

depositing a second layer on top of said first layer of dielectric and said via pattern thereby creating the plane for the formation of the upper portion of said dual damascene structure;

forming a pattern in said second layer wherein said pattern overlays and mates with said via pattern thereby forming the upper portion of said dual damascene structure;

depositing a layer of inter level dielectric over said pattern in said second layer and over said first layer of dielectric thereby forming an insulating layer around the upper portion of said dual damascene structure;

planarizing said layer of inter level dielectric down to the level of the top surface of said upper portion of said dual damascene structure;

removing said second layer material from said pattern within said second layer and said pattern within said first layer of dielectric thereby creating the dual damascene hole;

depositing a barrier within said dual damascene hole whereby said barrier penetrates said dual damascene hole and covers the

bottom and sidewalls of dual damascene hole thereby creating a region of insulation between the dual damascene structure and the surrounding dielectrics;

depositing copper within said dual damascene hole whereby said deposition fully fills said dual damascene hole thereby forming the dual damascene structure; and

planarizing said copper and said barrier.

22. The method of claim 21 wherein said dielectric material contains any of the non-metallic elements used within the manufacturing of semiconductor devices.

23. The method of claim 21 wherein said base layer is present at any level within the construct of a semiconductor device.

24. The method of claim 21 wherein said barrier deposition uses low pressure CVD technology.

25. The method of claim 21 wherein said barrier deposition uses high temperature CVD technology.

26. The method of claim 21 wherein said barrier contains tantalum or any of its derivatives.

27. The method of claim 21 wherein said barrier contains titanium or any of its derivatives.

28. The method of claim 21 wherein said pattern in said second layer overlays and mates with said via pattern and wherein the dimensions in the plane of deposition of each of the pattern elements or openings of said pattern in said second layer exceeds the dimensions in the plane of deposition of each of the elements or openings of said via pattern in said first layer of dielectric by a considerable margin.

29. The method of claim 21 wherein removing said second layer material is performed while adding HB_r/Cl_2 and oxygen containing gasses to the etch process in order to enhance etch selectivity.

30. The method of claim 21 wherein said second layer contains poly-silicon.

31. The method of claim 21 wherein said inter-level dielectric contains silicon dioxide.