ABSTRACT

TRANSISTORS WITH LOW OVERLAP CAPACITANCE

This invention relates to the fabrication of integrated circuit devices and more particularly to a method for reducing the gate to drain and gate to source overlap capacitance of deep sub-micron CMOS devices, as an improved means of reducing device switching times. This is accomplished by customizing the gate insulating layer, such that the dielectric constant, K, is lower in the gate to drain and gate to source overlap regions, relative to the more centrally located gate region between the source and drain. This invention avoids the process control problems associated with using conventional post polysilicon gate oxidation as a means of lowering such overlap capacitance, particularly for the deep sub-micron regime.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)