DESCRIPTION

LEAD FRAME SUBSTRATE AND METHOD OF MANUFACTURING THE SAME, AND SEMICONDUCTOR DEVICE

TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor package substrate suitable for mounting a semiconductor element, and a semiconductor device, and more particularly to a lead frame substrate and a method of manufacturing the same, and a semiconductor device using the lead frame substrate and the method of manufacturing the same.

This application claims priority to and the benefits of Japanese Patent Application No. 2008-254312 filed on September 30, 2008, the disclosure of which is incorporated herein by reference.

BACKGROUND ART

[0002]

In semiconductor packages using a lead frame represented by a quad flat package (QFP), outer leads for connection with a printed circuit board are disposed on side surfaces of the semiconductor package.

Such a lead frame is allowed to obtain a semiconductor element mounting section, inner leads acting as sections for connection with semiconductor element electrodes, outer leads, and an outer frame section fixing them by forming predetermined photoresist patterns on both surfaces of a metal plate and etching the both surfaces of the metal

plate. Further, these sections can be obtained by punching using a press in addition to the etching method.

In an assembly process of the semiconductor package, the semiconductor element is die-bonded onto the semiconductor element mounting section, and then the electrodes of the semiconductor element are electrically connected with the inner leads using, for instance, gold wires. Afterwards, the surroundings of the semiconductor element including the inner leads are encapsulated with a resin, and the outer frame section is cut off. If necessary, the outer leads are bent.

[0003]

In this way, the outer leads disposed on the side surfaces are limited to a range from 200 to 300 pins in a package size of about 30 mm^2 from the viewpoint of a processing ability of miniaturization.

In recent years, as the number of electrodes of the semiconductor element increases, a lead frame type semiconductor package having outer leads on side surfaces thereof cannot have a terminal number corresponding to the electrode number. Some external connection terminals of, for example, a ball grid array (BGA) type or a land grid array (LGA) type for connection with a printed circuit board are replaced by a semiconductor package disposed in an array shape on a bottom surface of a package substrate.

[0004]

The substrates used for these packages are generally configured to drill holes through a glass epoxy substrate having copper bonded on both surfaces thereof, bring a wall of each hole into conduction by means of plating, and form terminals for connection with the electrodes of the semiconductor element on one of the surfaces and external connection terminals arranged in an array shape on the other surface.

However, the manufacturing of the substrates requires a

complicated process as well as a high cost, and provides low reliability compared to the lead frame type package because the plating is used to connect interconnections within the substrate.

[0005]

For this reason, a BGA type semiconductor package structure using a lead frame, in which a process of etching the lead frame from both surfaces is used, is disclosed (e.g., Patent Document 1).

[0006]

In this structure, connection terminals for semiconductor element electrode are formed on one surface and external connection terminals are formed in an array form on the other surface by changing two photoresist patterns and etching the patterns at the same time or by etching one of the photoresist patterns, coating a pre-mold resin on the etched surface, and then etching the other photoresist pattern.

[0007]

Patent Document 1: Japanese Patent No. 3642911

DISCLOSURE OF INVENTION

Problem to be Solved by the Invention

[0008]

FIGS. 5A and 5B are cross-sectional views showing a conventional lead frame substrate.

In a BGA type lead frame, when the number of external connection terminals 111 increases, an interconnection 110 on the side of each semiconductor element electrode connection terminal 109 is lengthened. Since this interconnection is formed by half-etching a metal plate, it has a narrow width as well as a thin thickness. Thus, the interconnection is broken or bent in the processes following the etching, so that the yield is greatly reduced.

[0009]

In contrast, it is disclosed, for instance, in Patent Document 1 that, first, half-etching is performed only on the side of the external connection terminals 111, an electrodeposited polyimide layer 119 is formed on the etched surface, and the side of the semiconductor element electrode connection terminals 109 is etched so that the lead frame substrate is formed. Thereby, although the fine interconnections 110 are thin films, the fine interconnections 110 are supported by the polyimide layer 119, so that the interconnections are prevented from being broken or bent when the lead frame is manufactured.

However, according to Patent Document 1, when the semiconductor element is mounted on the lead frame substrate having this structure and then is connected with the semiconductor element electrode connection terminals 109 by wire bonding, a wire connecting force is not applied because each connection terminal 109 has a hollow lower portion, and connection failures take place. Thus, an assembly yield is remarkably reduced.

[0010]

Meanwhile, (although not disclosed in Patent Document 1), another countermeasure of thickening a resin layer by potting a pre-mold resin instead of the electrodeposited polyimide layer is also taken into consideration. This countermeasure is expected to prevent the problem with bonding failure to some extent. However, it is very difficult to adjust an amount of coating, and it is impossible to entirely avoid the hollow state.

For this reason, when the pre-mold resin is coated on a second surface at a constant amount using printing technology, the resin layer is formed to a relatively uniform thickness. Although the resin layer

is formed on the external connection terminals, it is also inferred that a removal process becomes easy due to a uniform film thickness.

[0011]

However, in the conventional structure of the external connection terminals (FIGS. 6A and 6B are a top view and a cross-sectional view after first etching is performed, respectively), the external connection terminal is considerably bulky as if its diameter ranges from about 200 μm to about 400 μm and its height ranges from about 100 μm to about 180 μm. Here, according to printing conditions, there is a risk of injecting air bubbles into the resin layer after printing is performed, and thus there is another risk of remarkably reducing the yield of production.

FIG. 6C shows a state of a thermally cured resin layer around an external connection terminal after printing is performed. As schematically shown in FIGS. 6A through 6C, there is a risk of air bubbles being formed over the external connection terminal in a printing direction (indicated by an arrow D1).

[0012]

The present invention has been made in view of the above-described circumstances, and an object of the invention is to provide a lead frame substrate and a method of manufacturing the same, and a related semiconductor element, capable of coping well with an increase in the number of electrodes of a semiconductor element, preventing air bubbles from being entrained, providing high reliability, and performing manufacture and assembly of a semiconductor package in a stable manner.

Means for Solving the Problem

[0013]

A first aspect of the present invention is a lead frame substrate, including: a metal plate having first and second surfaces; a semiconductor element mounting section, semiconductor element electrode connection terminals, and a first outer frame section formed on the first surface; external connection terminals formed on the second surface and electrically connected with the semiconductor element electrode connection terminals; a second outer frame section formed on the second surface; and a resin layer formed on a gap between the first outer frame and the second outer frame, wherein each external connection terminal buried in the resin layer has at least one projection formed on a side surface thereof throughout a side lower portion of the first surface.

[0014]

A second aspect of the present invention is a method of manufacturing a lead frame substrate, the method including: forming photoresist pattern to form a semiconductor element mounting section, semiconductor element electrode connection terminals, and an outer frame section on a first surface of a metal plate; forming external connection terminals connected with the semiconductor element electrode connection terminals and an outer frame section on a second surface of the metal plate; forming one or more protrusion-shaped patterns, the photoresist pattern to form the external connection terminals including the protrusion-shaped patterns; forming, through etching, non-through holes in a metal plate exposing section in which the metal plate of the second surface is exposed; coating a liquid pre-mold resin in the holes from the external connection terminals toward a direction of a projection, and heating and curing the pre-mold resin to form a resin layer; and etching the first surface to form the semiconductor element mounting section, the semiconductor element

electrode connection terminals electrically connected with the external connection terminals, and the outer frame section.

[0015]

A third aspect of the present invention is a semiconductor device including: a lead frame substrate including a metal plate having first and second surfaces, a semiconductor element mounting section, semiconductor element electrode connection terminals, and a first outer frame section which are formed on the first surface, external connection terminals formed on the second surface and electrically connected with the semiconductor element electrode connection terminals, a second outer frame section formed on the second surface, and a resin layer formed on a gap between the first outer frame and the second outer frame, wherein each external connection terminal buried in the resin layer has at least one projection formed on a side surface thereof throughout a side lower portion of the first surface, wherein a semiconductor element is mounted on the lead frame substrate and electrically connected with the lead frame substrate by wire bonding.

Effect of the Invention

[0016]

According to the present invention, external connection terminals for connection with a printed circuit board can be disposed on the entire rear surface of a lead frame substrate in an array form, and cope with an increase in the number of pins of a semiconductor element. Further, it is possible to ensure reliability against thermal stress because of a substrate based on a lead frame and use of no plating interconnections.

Meanwhile, when the lead frame substrate is manufactured, failures such as breaking or bending of the interconnection, as well as

the entrainment of air bubbles are not generated. When a wire bonding process, i.e. a semiconductor package assembly process, is performed, a lower portion of each wire-bonding connection terminal can be stabilized and connected because a pre-mold resin layer is present on the same plane as the surface of the external connection terminal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017]

FIG. 1A is a cross-sectional view showing an example of a method of manufacturing a lead frame substrate according to an embodiment of the present invention.

FIG. 1B is a cross-sectional view showing an example of a method of manufacturing a lead frame substrate according to the embodiment of the present invention in the process following that of FIG. 1A.

FIG. 1C is a cross-sectional view showing an example of a method of manufacturing a lead frame substrate according to the embodiment of the present invention in the process following that of FIG. 1B.

FIG. 1D is a cross-sectional view showing an example of a method of manufacturing a lead frame substrate according to the embodiment of the present invention in the process following that of FIG. 1C.

FIG. 1E is a cross-sectional view showing an example of a method of manufacturing a lead frame substrate according to the embodiment of the present invention in the process following that of FIG. 1D.

FIG. 1F is a cross-sectional view showing an example of a

method of manufacturing a lead frame substrate according to the embodiment of the present invention in the process following that of FIG. 1E.

FIG. 2A is a top view showing a photoresist pattern in a lead frame substrate according to the embodiment of the present invention.

FIG. 2B is a top view after the lead frame substrate is etched according to the embodiment of the present invention.

FIG. 2C is a cross-sectional view taken along line A2-A2 of FIG. 2B.

FIG. 2D is a top view after a lead frame substrate according to another embodiment of the present invention is etched.

FIG. 3 is a top view showing an example of a lead frame substrate according to the embodiment of the present invention, wherein the lead frame substrate is subjected to first etching.

FIG. 4A is a cross-sectional view showing an example of a lead frame substrate according to the embodiment of the present invention, wherein a semiconductor element is mounted and then wire-bonded.

FIG. 4B is a cross-sectional view showing an example of the lead frame substrate according to the embodiment of the present invention after transfer-molding encapsulation.

FIG. 5A is a cross-sectional view showing an example of a conventional lead frame substrate.

FIG. 5B is a cross-sectional view showing another example of the conventional lead frame substrate.

FIG. 6A is a top view showing an example of a conventional lead frame substrate after an external connection terminal is subjected to first etching.

FIG. 6B is a cross-sectional view showing an example of the conventional lead frame substrate after the external connection

terminal is subjected to first etching.

FIG. 6C is top view showing an example of the conventional lead frame substrate after the external connection terminal is subjected to first etching and then a resin layer is formed.

BEST MODE FOR CARRYING OUT THE INVENTION

[0018]

FIGS. 1A through 1F are schematic cross-sectional views showing a process of manufacturing a lead frame substrate.

Photoresist patterns 2 are formed on both surfaces of a metal plate 1 used for a lead frame (FIG. 1B). In FIGS. 1A through 1F, a pattern for a semiconductor element mounting section 8, connection terminals 9 for semiconductor element electrodes, interconnections 10, and an outer frame section 12 is formed on an upper surface of the metal plate 1, and a pattern for external connection terminals 11 and an outer frame section is formed on a lower surface of the metal plate 1.

[0019]

Thus, as shown in FIG. 2A, the embodiment of the present invention appropriately forms one or more protrusions 13 in addition to the external connection terminal forming pattern having a desired shape (in this case, a circular shape).

The pattern of this protrusion 13 formed of photoresist is designed so that a second metal surface is not left in subsequent etching.

The pattern of the protrusion 13 may be generally set to have a width of 30 μm or less and a length of 100 μm or less. However, because the protrusion is influenced by etching conditions of forming a hole 3 and an amount of etching, and a metal portion left behind after the etching is subjected to changes in size and shape, it is necessary to

take them into consideration to optimize the size of the protrusion 13 of the photoresist pattern.

[0020]

As the metal plate 1, any material may be used if it has etchability, mechanical strength, thermal conductivity, coefficient of expansion, and the like suitable for the lead frame. However, an iron-nickel alloy represented by Alloy42, a copper alloy in which a variety of metal elements are added to improve mechanical strength, or the like is often used as the metal plate 1.

The metal plate 1 is etched from the lower surface thereof using an etching solution, such as a ferric chloride solution, which dissolves the metal plate, and thus holes 3 are formed (FIG. 1C). The holes 3 may have a depth after the holes 3 are etched with a thickness of about 10 μm to about 50 μm left such that a fine interconnection can be formed when the metal plate is subjected to second etching from the upper surface thereof, in order to allow the remainder of the metal plate to be finally formed into the interconnection.

[0021]

The external connection terminal is formed with at least one projection 14, as shown in FIGS. 2B and 2C.

FIG. 2C shows a cross section taken along line A2-A2 of FIG. 2B, wherein the projection 14 is formed lower than a second surface. FIG. 2B shows that one projection 14 is formed, and FIG. 2D shows that two projections 14 are formed.

[0022]

Afterwards, the etched metal plate is turned upside down, and then a liquid pre-mold resin 5 is coated on an upper surface of the metal plate in a direction of an arrow D5 (FIG. 1D).

Such a coating may apply printing technology, which is

generally favorable from the viewpoint of productivity and quality. As the printing method, any method in which the coating can be done at a proper thickness may be used. However, screen printing is generally favorable. A printing direction is set to a direction of an arrow D2 of FIG. 2B, an arrow D3 of FIG. 2D, or an arrow D4 of FIG. 2D. Thereby, it is possible to give directionality to a flow of the pre-mold resin and to prevent air bubbles from being entrained. After the coating is performed, the pre-mold resin is heated and cured (FIG. 1E).

[0023]

After the printing coating is performed, a resin layer 6 of several microns or so is uniformly formed on the second surface (not shown). As such, it is necessary to remove this resin layer to expose the second surface. The removal method may be selected from dry etching, mechanical polishing, chemical polishing, and so on.

Furthermore, the opposite surface is etched to form the semiconductor element mounting section 8, the semiconductor element electrode connection terminals 9, and the interconnections 10. Thereby, a lead frame substrate 7 is obtained (FIG. 1F). FIG. 3 is a top view of the side of the external connection terminals. It is possible to dispose the external connection terminals in an array form, and to cope with a tendency to increase the number of pins of the semiconductor element.

[0024]

FIG. 4A is a cross-sectional view showing that a semiconductor element 15 is mounted and wire-bonded. The semiconductor element 15 is adhered by a die attach material 17, and is connected with the semiconductor element electrode connection terminals 9 by gold wires 16. If necessary, the semiconductor element electrode connection terminals may be properly subjected to any one of nickel-gold plating,

tin plating, silver plating, nickel-palladium-gold plating, and so on.

Further, when wire bonding is performed, the lead frame substrate is placed on a heat block, and is bonded while being heated. However, the pre-mold resin below the semiconductor element electrode connection terminals 9 is present on the same plane, and a hollow structure is not provided, so that it is possible to perform assembly without causing bonding failures.

[0025]

Finally, the side of the semiconductor element is encapsulated by transfer-molding or potting, and then the outer frame section is separated by, for instance, a diamond blade, so that the lead frame substrate is formed into a small piece (FIG. 4B).

In the case of the BGA type, solder balls are mounted on the external connection terminals, and thus the semiconductor package using the lead frame substrate is obtained.

[Example]

[0026]

As an example of applying an embodiment of the present invention, a ball grid array (BGA) type lead frame substrate will be described with reference to FIGS. 1A through 1F.

The manufactured BGA package has a size of 10 mm^2, and includes external connection terminals having an array form of 168 pins on a lower surface thereof.

[0027]

First, as shown in FIG. 1A, a metal plate 1 (available from Furukawa Electric Co., Ltd., EFTEC64T), which was formed of a copper alloy and had a width of 150 mm and a thickness of 200 μm in a long strip shape, was prepared.

Next, as shown in FIG. 1B, photoresist (available from Tokyo

Ohka Kogyo Co., Ltd., OFPR4000) was coated on both surfaces of the metal plate 1 by a roll coater so as to have a thickness of 5 μm, and then was pre-baked at a temperature of 90 °C.

Then, pattern exposure was performed from both surfaces via a photo mask having a desired pattern. Afterwards, development was performed using a 1% aqueous sodium carbonate solution, and then water-cleaning and post-baking were performed. Thereby, photoresist patterns 2 were obtained as shown FIG. 1B.

[0028]

As photoresist patterns, a pattern which forms a semiconductor element mounting section 8, semiconductor element electrode connection terminals 9, interconnections 10, and an outer frame section 12 was formed on a first surface of the metal plate, and a pattern which forms external connection terminals 11, each of which has the protrusion 13 (FIG. 2A), and an outer frame section 12 was formed on a second surface of the metal plate. Here, the protrusion 13 was shaped like an isosceles triangle which was in contact with the external connection terminal and had a width of 30 μm and a length of 80 μm.

[0029]

Next, the side of the first surface of the metal plate 1 was protected by covering a back sheet (not shown). Then, first etching was performed from the second surface of the metal plate using a ferric chloride solution, and parts of the metal plate exposed from the photoresist pattern of the side of the second surface were reduced in thickness up to 30 μm (FIG. 1C).

Further, the projection 14 having a length of about 40 μm could be formed on a side surface of the external connection terminal. The used ferric chloride solution was set to have a specific gravity of 1.38 and a temperature of 50 °C.

[0030]

Next, screen printing coating was performed on the second surface, in which holes were formed by the first etching, using a liquid thermosetting resin (available from Shin-Etsu Chemical Co., Ltd., SMC-376KF1). The printing was performed from a place where the projection 14 was not present toward the direction of the projection (FIG. 1D).

The resin was again cured at 180 °C for 3 hours, and thus a pre-mold layer 13 was formed. The thermosetting resin was excellent in fillability, and failures including air bubbles were not observed.

[0031]

Since a thermosetting resin layer of about 1 μm was left on the non-etched surfaces of the external connection terminals 11 and the outer frame section 12, the thermosetting resin layer was processed and removed for about 3 minutes using an aqueous alkaline solution of potassium permanganate at 60 °C (potassium permanganate of 40 g/L + sodium hydroxide of 20 g/L).

[0032]

Next, the back sheet was removed from the side of the first surface, and then the parts of the metal plate that were exposed from the photoresist pattern by performing second etching from the side of the first surface of the metal plate, were dissolved and removed by a ferric chloride solution. Thereby, the semiconductor element mounting section 8, the semiconductor element electrode connection terminals 9, the interconnections 10, and the outer frame section 12 were formed (FIG. 1E). The external connection terminals 11 extend from the semiconductor element electrode connection terminals 9.

Further, although not shown, a back sheet may be adhered to the side of the second surface when the second etching is performed so as

to prevent unnecessary etching from being performed on the side of the lower surface.

[0033]

Subsequently, the photoresist pattern 2 of the first surface was stripped, and thus a desired lead frame type BGA substrate 7 was obtained (FIG. 1F).

Next, the metal surface exposed after the stripping of the photoresist was subjected to electrolytic nickel-gold plating.

Thicknesses of the nickel and gold were 5 μm and 0.1 μm, respectively (not shown).

[0034]

Then, a semiconductor element 15 was mounted on the lead frame type BGA substrate 7 of the present invention using a die attach material 17, and then the die attach material was cured at 150 °C for 1 hour. Further, the electrodes of the semiconductor element and the semiconductor element electrode connection terminals 9 were connected by wire bonding using gold wires 16 having a diameter of 30 μm (FIG. 4A).

A heating temperature for the wire bonding was 200 °C. An entire strength of the wires on the side of the semiconductor element electrode connection terminals was measured to be 9 g or more, and good connection was obtained.

[0035]

Afterwards, as shown in FIG. 4B, an area including the semiconductor element and the semiconductor element electrode connection terminals was encapsulated by transfer-molding, and was cut into a small piece, so that the semiconductor package using the lead frame type BGA substrate was obtained.

Industrial Applicability

[0036]

A method of manufacturing a lead frame substrate of the present invention is used to be able to reduce failures in manufacture or assembly of semiconductor packages and to obtain a lead frame substrate with high reliability against thermal stress, and particularly, is applied to multi-pin package substrates that cannot be supported for a lead frame type semiconductor package.

Reference Symbols

[0037]

1: metal plate

2: photoresist pattern

3: hole

4: squeezer

5: liquid pre-mold resin

6: resin layer

7: lead frame substrate

8: semiconductor element mounting section

9: semiconductor element electrode connection terminal

10: interconnection

11: external connection terminal

12: outer frame section

13: photoresist protrusion pattern

14: projection

15: semiconductor element

16: gold wire

17: die attach material

18: transfer-molding resin

19: air bubble

CLAIMS

1. A lead frame substrate, comprising:

a metal plate having first and second surfaces;

a semiconductor element mounting section formed on the first surface;

at least one semiconductor element electrode connection terminal;

a first outer frame section formed on the first surface;

at least one external connection terminal formed on the second surface and electrically connected with the at least one semiconductor element electrode connection terminal;

a second outer frame section formed on the second surface; and

a resin layer formed on a gap between the first outer frame and the second outer frame,

wherein the at least one external connection terminal buried in the resin layer has at least one projection formed on a side surface thereof, the at least one projection being formed between a side lower portion of the at least one external connection terminal and a side upper portion of the at least one external connection terminal,

wherein first height between a first point of the at least one projection and a second point of the at least one projection is lower than a second height of the at least one external connection terminal, and

wherein the first point is the most near from the at least one external connection terminal, and the second point is the most far from the at least one external connection terminal.

2. The lead frame substrate according to claim 1,

wherein the more a third point is far from the side upper portion, the more the first height is low, and

the third point is between the first point and the second point.

3. The lead frame substrate according to claim 2,

wherein the height of the first point is the same height as that of the side upper portion, and the height of the second point is the same height as that of the side lower portion.

4. The lead frame substrate according to claim 3,

wherein a first percent of slope between the first point and a fourth point is different from a second percent of slope between the second point and the fourth point, and

wherein the fourth point is between the first point and the second point.

5. A method of manufacturing a lead frame substrate, the method comprising:

forming photoresist pattern to form a semiconductor element mounting section, at least one semiconductor element electrode connection terminal, and a first outer frame section on a first surface of a metal plate;

forming at least one external connection terminal connected with the at least one semiconductor element electrode connection terminal and a second outer frame section on a second surface of the metal plate;

forming at least one protrusion-shaped pattern, the photoresist pattern to form the at least one external connection terminal including the at least one protrusion-shaped pattern;

forming, through etching, at least one non-through hole in a metal plate exposing section in which the metal plate of the second surface is exposed;

coating a liquid pre-mold resin in the at least one non-through hole from the at least one external connection terminal toward a direction of at least one projection, and

heating and curing the liquid pre-mold resin to form a resin layer; and

etching the first surface to form the semiconductor element mounting section, the at least one semiconductor element electrode connection terminal electrically connected with the at least one external connection terminal, and the first and second outer frame sections,

wherein first height between a first point of the at least one projection and a second point of the at least one projection is lower than a second height of the at least one external connection terminal, and

wherein the first point is the most near from the at least one external connection terminal, and the second point is the most far from the at least one external connection terminal.

6. The method of manufacturing the lead frame substrate according to claim 5,

wherein the more a third point is far from the side upper portion, the more the first height is low, and

the third point is between the first point and the second point.

7. The method of manufacturing the lead frame substrate according to claim 6,

wherein the height of the first point is the same height as that of the side upper portion, and the height of the second point is the same height as that of the side lower portion.

8. The method of manufacturing the lead frame substrate according to claim 7,

wherein a first percent of slope between the first point and a fourth point is different from a second percent of slope between the second point and the fourth point, and

wherein the fourth point is between the first point and the second point.

9. A semiconductor device comprising:

a lead frame substrate including

a metal plate having first and second surfaces,

a semiconductor element mounting section formed on the first surface,

at least one semiconductor element electrode connection terminal, and

a first outer frame section formed on the first surface,

at least one external connection terminal formed on the second surface and electrically connected with the at least one semiconductor element electrode connection terminal,

a second outer frame section formed on the second surface, and

a resin layer formed on a gap between the first outer frame and the second outer frame,

wherein the at least one external connection terminal buried in the resin layer has at least one projection formed on a side surface thereof, the at least one projection being formed between a side lower portion of the at least one external connection terminal and a side upper portion of the at least one external connection terminal,

wherein a semiconductor element is mounted on the lead frame substrate and electrically connected with the lead frame substrate by wire bonding,

wherein first height between a first point of the at least one projection and a second point of the at least one projection is lower than a second height of the at least one external connection terminal, and

wherein the first point is the most near from the at least one external connection terminal, and the second point is the most far from the at least one external connection terminal.

10. The semiconductor device according to claim 9,

wherein the more a third point is far from the side upper portion, the more the first height is low, and

the third point is between the first point and the second point.

11. The semiconductor device according to claim 10,

wherein the height of the first point is the same height as that of the side upper portion, and the height of the second point is the same height as that of the side lower portion.

12. The semiconductor device according to claim 11,

wherein a first percent of slope between the first point and a fourth point is different from a second percent of slope between the second point and the fourth point, and

wherein the fourth point is between the first point and the second point.