The subject of the present invention is an interconnection device between an integrated circuit (denoted IC) and an electrical circuit (denoted EC), such as, for example, a printed circuit (denoted PC), the EC including one face substantially parallel to the active face of the IC. The device is capable of linking at least one land of the IC and one connection point of the EC which are offset with respect to one another in an abstract plane (known as "reference" plane) substantially parallel to the active face of the IC. Thus, whatever the desired correspondence between the lands of the IC and the connection points of the EC, the device makes it possible to achieve a significant reduction in the number or in the length of the tracks produced in or on the IC or the EC, by virtue of a judicious choice of displacements, in the reference plane, within the device itself, such a choice being capable of being programmed. The subject of the invention is also a method of fabricating a part of this device from a predefined number of modules of a single type.

The relative dimensions of the lands of an active face of an IC and of the connection points of an EC, such as, for example, a single-layer or multi-layer PC, exclude the possibility of connecting the IC directly to the EC: it is necessary to interconnect the IC and the EC by means of a device in which the connection fineness is intermediate between that of the IC and that of the EC. Such a device necessarily takes up space and complicates the interconnection operation.

Moreover, the desired correspondence between the lands of the IC and the connection points of the EC may entail production of supplementary tracks.

Devices are known for interconnection between an IC and an EC including a base fabricated from an insulating material, situated between the IC and the EC, the dimensions of which in the said reference plane are considerably greater than those of the IC, on which the IC is fixed on the side opposite its active face; the desired interconnection is produced by means of

electrically conducting wires (known as "die bonding" wires, and the fineness of which is of the same order of magnitude as that of the lands of the IC), linking the lands of the IC to electrically conducting tracks (the fineness of production of which is intermediate between that of the lands of the IC and that of the connection points of the EC) which are produced on and/or within the base, these tracks diverging around the IC towards leads for example, which are intended to be plugged into the holes of a PC. It is also known to equip such a base, not with leads, but with lands, placed at the periphery of the face of the base situated opposite the EC, linked to the said tracks, for example, by means of a partial metallization of the sides of the base, and intended to be welded to the connection points of the EC.

These known devices exhibit many drawbacks, however:

- because of their fineness, the bonding wires are fragile; in order to minimize this fragility, these wires are as short as possible and reach only to sites situated at the periphery of the active face of the IC (put another way, the lands of the IC are peripheral): this on the one hand limits the number of lands of an IC of given surface area, and, on the other hand, involves the production of tracks (in and/or on the IC) linking regions situated at the centre of the active face of the IC to the periphery of the latter;
- still because of their fineness, the bonding wires are tricky to connect, both to the lands of the IC and to the tracks of the base;
- the bonding wires are connected one by one, which takes time;
- the dimensions of the base in the reference plane being greater than those of the IC, the interconnection device is bulky;
- this interconnection device does not make it possible to compensate for a possible complexity in the desired correspondence between the lands of the IC and the points of the EC.

Moreover, devices are known for interconnection between an IC and an EC including layers of dielectric material however [sic] conducting tracks and conducting vias. Thus, the article which appeared in IBM Technical Disclosure Bulletin, vol. 28, No. 3, August 1985, pages 1184-1185 describes a multi-layer device for connection between a semiconductor chip and a base layer carrying pins, which corresponds to a device according to the pre-characterizing part of Claim 1. The device includes at least one intermediate dielectric layer traversed by conducting vias on the two faces of which are applied conducting track patterns according to a conventional technique of printed circuit production. These patterns are determined on the basis of the power supply and signal distributions to be formed, then the extremities of vias of one face of a layer are welded to appropriate tracks of the opposite face of the adjacent layer.

Another solution known from the European Patent Application EP-A-0 268 111 consists, for interconnecting semiconductor chips and a common interconnection substrate, in interposing several dielectric sheets each carrying parallel conducting tracks deposited by metallization and allowing the desired interconnections with the aid of conducting vias pierced or interrupted in some of the layers.

In both cases, it is necessary to produce either drawings of specific tracks or piercings and metallizations of specific vias which are characteristic of the interconnection to be produced. Thus the fabrication of each layer requires different operations according to relatively complex and costly production techniques.

The invention therefore proposes to remedy the drawbacks resulting from the use of bonding wires, by making use of a very much simplified device, which is easy to manufacture and inexpensive by virtue of very rigorous standardization of the interconnection elements provided.

These drawbacks are eliminated by an interconnection device between an integrated circuit and an

electrical circuit, and a method of fabrication as defined in Claims 1 and 7, respectively. Advantageous modifications are defined in the dependent Claims 2 to 6, 8 and 9.

Specifications, features and various embodiments of the invention will appear in the course of the description which follows, with the aid of the attached figures which represent:

- Figure 1, a sectional view of a known device for interconnection between an IC and an EC;
- Figure 2, a top view of the known device of Figure 1;
- Figure 3, an exploded diagram of an embodiment of the device according to the invention, situated between the two circuits (IC and EC) which it links;
- Figure 4, an exploded diagram of a preferred embodiment of the device according to the invention, situated between the two circuits (IC and EC) which it links;
- Figure 5, a detailed and perspective view of a first variant of the device of Figure 4 drawn in isolation, and represented in the course of fabrication;
- Figure 6, a part of the elements of Figure 5;
- Figure 7, a non-detailed view in exploded perspective of a second variant of the device of Figure 4, drawn in isolation;
- Figure 8, a flow chart of a first variant of a method of fabricating a wafer of the device according to the invention;
- Figure 9, a flow chart of a part of a second variant of a method of fabricating a wafer of the device according to the invention;
- Figure 10, a top view illustrating variants of the device of Figure 4, drawn in isolation.

On these various figures, on the one hand the real scale has not been respected, and on the other hand, the same references relate to the same elements.

A known and previously described device is illustrated, respectively in section and top view, in Figures 1 and 2. An IC 1 is fixed by the adhesive 2 to a base 3: this base 3 includes a support plate 31, carrying

the IC 1 on its upper face, covered over by an annular plate 32, arranged on the support plate 31 and around the IC 1; the active face of the IC 1 is placed opposite the base 3, and carries peripheral lands 11; these lands are linked, by means of bonding wires 34 (which are welded at each of their extremities) to electrically conducting tracks 33, which are produced by screen printing on the annular plate 32; these tracks 33 diverge (as Figure 2 shows) towards leads 35 (which are welded to the tracks 33); these leads 35 are, for example, plugged into the holes 42 of a printed circuit 41 and welded to the latter by means of welds 5 according to a method known in itself.

Figure 3 shows, diagrammatically in exploded view, an embodiment of the device 6 according to the invention. This device 6 provides the interconnection between an IC 1, including a number k of lands 11 situated on its active face 12 (this face 12 defining an abstract reference plane 7 as was explained in the foregoing) and an EC 4, including, for example, the same number k of connection points 41 which are on a surface substantially parallel to the said reference plane. The device 6 includes a wafer, a first face 601 of which is situated opposite the active face 12 of the IC 1, and a second face 602 of which is situated opposite the said surface area of the EC 4, these faces 601 and 602 being substantially parallel to the reference plane. The wafer is produced in an electrically insulating material, whose thermal expansion coefficient is advantageously substantially equal to that of the IC 1. The dimensions of the wafer in the reference plane are advantageously substantially the same as those of the IC 1 which is, for example, square. On the faces 601 and 602 are respectively lands 61 and 62, arranged respectively opposite the lands 11 of the IC 1 and the connection points 41 of the EC 4, and the fineness of which is intermediate between that of the lands 11 of the IC 1 and that of the connection points 41 of the EC 4. The lands 61 of the first face 601 are linked, in a one-to-one way,

for example, to those 62 of the second face 602 by fusible electrically conducting channels (not represented in this Figure 3), at least one of which links a given land 61 (of the first face 601) to a given land 62 (of the second face 602) offset in the reference plane 7 with respect to the land 61 in question. In this Figure 3, the IC 1, the device 6, and the EC 4 are represented spaced apart from one another, but these elements are in reality in contact with one another, as the discontinuous arrows 8 show. Such a contact is provided by assembly means, consisting, for example, of solder joints produced in the region of each pair of lands (11, 61) and of each land and connection point pair (62, 41): microvolumes of an electrically conducting material are either deposited or obtained by crystalline growth on one and/or the other lands and/or connection points which are to be in contact; these microvolumes are then welded to the lands and/or connection points which surround them. All the solder joints corresponding to putting the IC and the device 6 into contact, or respectively the device 6 and the EC, that is to say all the solder joints formed in the region of pairs of lands (11, 61), or in the region of land and connection point pairs (62, 41) respectively, are produced in a single operation.

Figure 4 shows diagrammatically in exploded view a preferred embodiment of the device 6 according to the invention for which the lands 11 of the IC, those 61 and 62 of the faces 601 and 602 of the device 6, and the connection points 41 of the EC 4, are arranged respectively at the vertices of four grids Q_{IC}, Q_1, Q_2 and Q_{EC}. These four grids Q_{IC}, Q_1, Q_2 and Q_{EC} are substantially:

- regular;
- identical;
- identically oriented;
- not offset with respect to one another, as the axis A indicates. According to this preferred embodiment, the IC 1 and the device 6 are preferably square. The rest of the description of Figure 4 is similar to that of Figure 3.

Figure 5 illustrates, in a detailed way, a first

variant of the device 6 of Figure 4, drawn in isolation and represented in the course of fabrication: before its use, this device is intended to undergo a treatment (set out in the following), which depends on the desired correspondence between the lands of the IC and the connection points of the EC. This device 6 includes a wafer 100, said to be for offset and called "offset matrix stratum" (and denoted SMDP) due to the fact that it includes less [sic] one electrically conducting channel linking a given land 61 (of the first face 601) to a given land 62 (of the second face 602) offset with respect to the land 61 in question, as was specified in the foregoing. More precisely, as illustrated in Figure 6, which represents a part of the elements of Figure 5, an electrically conducting channel is capable of linking:
- either a land 611 (or 612 respectively), situated on the first face 601, to a land 621 (622 respectively), situated on the second face 602 of the wafer, not offset (put another way, offset by a number p = 0 of pitches of the grid Q_1 of the first face 601) with respect to the land 611 (612 respectively) of the first face 601;
- or a land 611 (612 respectively), situated on the first face 601, to a land 622 (621 respectively), situated on the second face 602 of the wafer, offset by a number p = 1 of pitches of the grid Q_1 of the first face 601 in one of the two directions of this grid Q_1.

The four cardinal geographical points (north, east, south, west respectively denoted N, E, S, W) are attributed to the SMDP 100 so as to facilitate the description of the device 6 and of its various elements.

An electrically conducting channel without offset includes a transverse path 91, called "direct", (98 respectively), substantially straight-line and substantially perpendicular to the reference plane 7, passing through a vertex 611 (612 respectively) of the grid Q_1 of the first face 601.

An electrically conducting channel with an offset includes, in this order:
- a longitudinal track 94 (95 respectively),

substantially straight-line, produced on the first face 601, substantially parallel to a first diagonal D_1 of the grid Q_1 (parallel to the S/W - N/E direction), and the length of which is equal to half of the diagonal of an elementary square Ce of the grid Q_1;

- a transverse path 93 (92 respectively), called "indirect", substantially straight-line and substantially perpendicular to the reference plane 7, passing through a centre 631 (632 respectively) of the grid Q_1 of the first face 601;

- a longitudinal track 96 (97 respectively), substantially straight-line, produced on the second face 602, substantially parallel to the second diagonal D_2 of the grid Q_1 (parallel to the S/E - N/W direction), and of the same length as the longitudinal track 94 (95 respectively).

In the course of the description of Figures 5 and 6, the grid Q_1 of the first face 601 was arbitrarily taken as reference, but the grid Q_2 of the second face 602 could have played the same role.

At the stage of fabrication of the device 6 illustrated in Figures 5 and 6, each land 611 (612 respectively) of the first face 601 is linked, on the one hand, to a non-offset land 621 (622 respectively), and, on the other hand, to a land 622 (621 respectively) offset by a number p = 1 of pitches of the grid Q_1 in the E - W direction: the lands of the SMDP 100 are therefore grouped together in fours (two lands similar to the lands 611 and 612, and two lands similar to the lands 621 and 622).

According to the interconnection required between the IC and the EC, and with a view to minimizing the number or the length of the tracks produced in or on the IC or the EC, two routes are chosen for each of these groups of four lands. This choice is capable of being programmed. The fusible, electrically conducting channels corresponding to routes which are not chosen are burned out. According to the first variant illustrated by Figures 5 and 6 it is possible:

- either to link the land 621 to the land 611, and the land 622 to the land 612, which amounts to burning out the two electrically conducting channels constituted respectively by the longitudinal tracks 94, 96 and 95, 97 on the one hand, and the indirect transverse paths 93 and 92 on the other hand;
- or linking the land 622 to the land 611 and the land 621 to the land 612, which amounts to burning out the two channels constituted respectively by the direct transverse paths 91 and 98.

As was explained previously, the SMDP 100 includes at least one electrically conducting channel with an offset, that is to say at least one grouping of four lands 611, 612, 621, 622 linked according to the second choice.

Figure 7 gives a non-detailed view in perspective of a second variant of the device 6 of Figure 4, drawn in isolation. This device includes a number n of preferably square wafers of a first type 1000, 2000, 3000, 4000, etc., separated by a number n-1 of preferably square wafers of a second type 1002, 2003, 3004, etc. These wafers of a first type are substantially identical to the SMDP 100 of Figures 5 and 6 and are also called SMDP. The correspondence between the lands of a first face and the lands of the second face of each of the wafers of the first type, that is to say the choice of the routes within each of these SMDPs, is specific to each of these SMDPs. More exactly, each wafer of the first type is capable, for each grouping of four lands similar to those 611, 612, 621, 622 of Figures 5 and 6, of introducing an offset in the E-W direction of the four cardinal points N, E, S, W which are specific to it (in Figure 7 only the cardinal point N 21, 22, 23, 24 of each SMDP of the first type 1000, 2000, 3000, 4000 has been drawn). A combination of the choice of the routes within each SMDP, of the orientation of the SMDPs 1000, 2000, 3000, 4000, etc., with respect to one another, and of the number n of SMDPs, is therefore capable of providing any correspondence whatever between the lands of the first face of the

SMDP 1000 which is situated opposite the active face of the IC, and those of the second face of the SMDP which is situated opposite the EC: in the particular case illustrated by Figure 7, in a fixed reference system 29 corresponding to the four cardinal points N, E, S, W of the reference plane 7:

- the wafer 1000 provides at least one E-W shift;
- the wafer 2000 provides at least one N-S shift;
- the wafer 3000 provides at least one E-W shift;
- the wafer 4000 provides at least one N-S shift.

According to the configuration of SMDPs 1000, 2000, 3000, 4000, etc., it is vital, moreover, to interpose, between these SMDPs, wafers of a second type 1002, 2003, 3004, etc., which have the function of insulating the longitudinal tracks of the second (first respectively) face of a given SMDP, from those of the first face (second respectively) of an adjacent SMDP. The wafers of the second type are called "insulation strata" (and denoted IS); they are similar to the SMDP 100 of Figures 5 and 6, but include only direct transverse paths. The thickness of the ISs 1002, 2003, 3004, etc., is advantageously less than that of the SMDPs 1000, 2000, 3000, 4000, etc., so as to reduce the dimension of the device 6 perpendicularly to the reference plane 7: in fact, the ISs (in contrast to the SMDPs) show no risks of breakdown between the longitudinal tracks situated on either side of the same wafer.

A flow chart of a first variant of a method for fabricating a wafer of the device according to the invention is illustrated in Figure 8. This diagram represents the steps of fabrication of the SMDP similar to those 1000, 2000, 3000, 4000, etc., of Figure 7, or to that 100 of Figure 5.

These steps are interlinked in the following way:

- a wafer, the surface of which preferably has substantially the same dimensions as those of the active face of the IC, is fabricated according to a known method in an electrically insulating material, during a step 10;
- holes are pierced through the wafer, substantially

perpendicularly to its faces, at the vertices and at the centres of a substantially regular grid, during a step 20;

- the inner surface of these holes is covered with an electrically conducting layer: such as, for example, metal, which constitutes a step 30;

- electrically conducting tracks are produced, for example by screen printing, on each of the faces of the wafer, according to the drawing corresponding to Figures 5 and 6 during a step 40;

- a definition of the lands of each of the faces of the wafer which it is desired to link together constitutes a step 50 (this definition is a function of the desired correspondence between the lands of the IC and the connection points of the EC);

- routes are chosen according to this definition during a step 60; these routes include traverses of the wafer in holes and displacements on one or the other face of the wafer along the said screen-printed tracks;

- the electrically conducting tracks and holes which are not chosen during the preceding step 60 are treated in such a way as no longer to conduct electricity: they are "burned out"; this operation constitutes step 70.

Steps 10, 20 and 30, constituting a phase 80 of fabrication of a wafer including transverse paths, can be replaced by a phase 800, the flow chart for which is given by Figure 9, and which includes:

- a phase 81 of arranging, in a number b, equal to the number of vertices and of centres of a first grid, coils of an electrically conducting wire, forming a distribution of b wires at the vertices and at the centres of this first grid;

- a phase (82, 83) of fabricating a first wafer, called "mould-wafer", fabricated from a material not adhering to the insulating material, the surface area of which is at least equal to that of the wafer of the device, including b holes, distributed at the vertices and at the centres of the first grid, each of the holes preferably having a cross-section the shape and the dimensions of which are

substantially the same as that of the wires;
- a phase 84 of passing the b wires respectively into the b corresponding holes of the first mould-wafer;
- a phase (85, 86) of fabricating and piercing a second mould-wafer, having substantially the same characteristics as the first one, and additionally including means for fixing the said b wires;
- a phase 87 of passing the wires into the second mould-wafer and of positioning the latter;
- a phase 88 of fixing the b wires respectively in the b corresponding holes of the said second mould-wafer;
- a phase 89 of injecting a hardenable, electrically insulating material between the two mould-wafers;
- a phase 90 of sectioning the b wires, on either side of the hardenable material after it has hardened, the b wires constituting said transverse paths.

An IS similar to those 1002, 2003, 3004, etc., of Figure 7 is produced according to a method of fabrication including only steps similar to those constituting phase 80 of Figure 8, or that 800 of Figure 9, the holes moreover being produced only at the vertices of the grid.

Variants of the first and second embodiments of the device according to the invention are illustrated by Figure 10. The longitudinal tracks 94 and 96 (97 and 95 respectively) of Figure 6 form a right angle [lacuna] between them. The invention also covers two other configurations, illustrated in Figure 10, according to which the tracks 94 and 96 (97 and 95 respectively) are replaced by tracks 941 and 961 (971 and 951 respectively), forming an obtuse angle [lacuna] between them, or alternatively by tracks 942 and 962 (972 and 952 respectively), forming an acute angle [lacuna] between them. These two types of tracks are such that the indirect transverse paths respectively linking the tracks 94, 941 or 942 (95, 951 or 952 respectively) situated on the first face of the wafer to the tracks 96, 961 or 962 (97, 971 or 972 respectively) situated on the second face of the wafer pass through the mid-perpendicular D of the positions of the two lands 611 and 612 of the first face.

The invention also covers embodiments according to which the offset pitch p is an integer strictly greater than 1.

CLAIMS

1. Interconnection device (6) between an integrated circuit IC (1) including lands (11) arranged on an active face (12) and an electrical circuit EC (4) including a surface substantially parallel to the active face of the IC (1), at which connection points (41) are situated, the said device (6) linking lands of the IC (1) and connection points of the EC (4), and including:

- at least one wafer of a first type (100), fabricated in an electrically insulating material, placed between the active face (12) of the IC (1) and the EC (4), the faces of which each include lands (61, 62, 611, 612, 621, 622), the lands (61, 611, 621) of a first face (601), situated opposite the IC (1), being arranged facing those (11) of the IC (1), and the lands (62, 612, 622) of the second face (602), situated opposite the EC (4), being arranged facing connection points (41) of the EC (4), the said wafer (100) further including internal means (91; 98; 94, 93, 96; 95, 92, 97), providing an electrical contact between the lands (61, 611, 621) of the said first face (601) and those (62, 612, 622) of the said second face (602),

- means of assembly by welding or soldering, providing an electrical contact between the lands (11) of the IC (1) and the lands (61, 611, 621) of the said first face (601) on the one hand and between the lands (62, 612, 622) of the said second face and the connection points (41) of the EC (4) on the other hand, the said assembly means including microvolumes of an electrically conducting material formed on one and/or the other of the lands or connection points which have to be in electrical contact, each of the said microvolumes having been welded to the lands or connection points which surround it, the lands (11) of the IC (1), of the said first face (601), of the said second face (602), and the connection points (41) of the EC (4) being arranged respectively at the vertices of four regular grids (Q_{IC}, Q_1, Q_2 Q_{EC}), these four grids being identical, identically oriented and not offset with respect to one another in an abstract reference plane (7)

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parallel to the active face (12) of the IC (1), the device being characterized in that:

- the lands (61, 62, 611, 612, 621, 622) of the said wafer (100) are of a fineness intermediate between that of the lands (11) of the IC (1) and that of the connection points (41) of the EC (4),
- the said internal means (91; 98; 94, 93, 96; 95, 92, 97) providing an electrical contact include a predetermined number of fusible electrically conducting channels (91; 98) passing through the wafer (100) without offset at points corresponding to the said vertices along a transverse path perpendicular to the said reference plane (7), and a predetermined and non-zero number of fusible electrically conducting channels (94, 93, 96; 95, 92, 97) passing through the wafer (100) with a given offset in the said reference plane (7) being effected for the same wafer (100) along one of the two directions of one of the grids (Q_1, Q_2) of the faces of the wafer (100), the said offset corresponding to a predefined, strictly positive, integer number p of pitch of the said grid (Q_1, Q_2);
- and in that the said conducting channels (94, 93, 96; 95, 92, 97) with offset each include a first, straight-line longitudinal track (94; 95), produced on the said first face (601) parallel to a first track direction, a second straight-line longitudinal track (96; 97), produced on the said second face (602) parallel to a second track direction and a transverse path (93; 92) linking the extremities of the said two longitudinal tracks through the said wafer (100) perpendicularly to the said reference plane (7).

2. Device according to Claim 1, characterized in that the said first direction of the longitudinal tracks on the first face (601) and the said second direction of the longitudinal tracks on the second face (602) are symmetric with respect to the direction of offset for the wafer (100).

3. Device according to one of Claims 1 or 2, characterized in that the number p is equal to 1.

4. Device according to Claim 3, characterized in

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that the said first and second longitudinal track directions are respectively a first diagonal (D_1) and a second diagonal (D_2) of the said grid (Q_1, Q_2), and that the length of each of the longitudinal tracks is equal to half of a diagonal.

5. Device according to one of Claims 1 to 4, characterized in that the dimensions of the wafer (100) in the said reference plane (7) are substantially equal to those of the IC (1).

6. Device according to one of Claims 1 to 5, characterized in that it includes:

- a number n of wafers of the said first type (1000, 2000, 3000, 4000) stacked and placed between the active face (12) of the IC (1) and the EC (4), the respective directions of offset of the wafers of the first type (1000, 2000, 3000, 4000) being oriented or not oriented differently with respect to one another according to the overall offset sought,
- a number n-1 of wafers of the second type (1002, 2003, 3004), each being interposed between two successive wafers of the first type (1000, 2000, 3000, 4000), fabricated in an electrically insulating material, the faces of which each include lands which are of the same fineness as that of the lands of the wafers of the first type and are arranged at the said vertices, the lands of the faces of a given wafer of the second type being linked by electrically conducting channels passing through this wafer without offset,
- means of assembly by welding or soldering of the microvolumes of an electrically conducting material providing an electrical contact between, on the one hand, the lands of one face of a wafer of the first type (1000, 2000, 3000, 4000) and, on the other hand, the lands of a wafer of the second type (1002, 2003, 3004).

7. Method of fabricating a wafer of the first type for a device according to one of Claims 1 to 5, characterized in that it includes:

- a step (10; 89) of fabricating the wafer in an insulating material;

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- a step (20, 30; 81-88, 90) of producing fusible electrically conducting transverse paths, passing through the wafer perpendicularly to its faces at points corresponding to the said vertices and to the extremities of the longitudinal tracks;

- a step (40) of producing straight-line fusible, electrically conducting longitudinal tracks, on each of the faces of the wafer, linking the extremities of transverse paths;

- a step (50) of defining a correspondence between the said extremities situated on one of the said faces and those situated on the other of the said faces and having to be electrically linked;

- a step (60) of choice of routes providing the said correspondence, each of the said routes being produced either by means of one of the said transverse paths or by means of one of the said longitudinal tracks situated on the said first face, followed by one of the said transverse paths, followed by one of the said longitudinal tracks situated on the said second face;

- a step (70) of destruction of the transverse paths and of the longitudinal tracks which have not been chosen.

8. Method according to Claim 7, characterized in that the steps of fabricating the said wafer and of producing transverse paths include:

- a phase (82) of fabricating a first wafer mould, fabricated in a material which is not able to adhere to the said insulating material;

- a phase (83) of piercing the said first wafer mould perpendicularly to its faces at points corresponding to the vertices and to the extremities of the longitudinal tracks of the wafer to be fabricated;

- a phase (84) of passing electrically conducting wires into the holes of the said first wafer mould;

- a phase (85, 86) of fabricating a second wafer mould, fabricated in the same material as the first wafer mould and pierced in the same way;

- a phase (87) of passing the said wires into the second wafer mould and of positioning the latter parallel to the

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said first wafer mould;

- a phase (89) of injecting an electrically insulating hardenable material, between the two wafer moulds;

- a phase (90) of sectioning the wires, on either side of the said hardenable material after its hardening, the wires constituting the said transverse paths and the said hardenable material constituting the insulating material of the wafer.

9. Method according to one of Claims 7 or 8, characterized in that the longitudinal tracks are produced by screen printing on the faces of the wafer.