What is claimed is:

1. A memory device comprising:

a plurality of memory cells each storing 5-bit data including first bit data, second bit data, third bit data, fourth bit data, and fifth bit data based on a threshold voltage, the plurality of memory cells storing a first page, a second page, a third page, a fourth page, and a fifth page, and the first page, the second page, the third page, the fourth page, and the fifth page respectively including the first bit data, the second bit data, the third bit data, the fourth bit data, and the fifth bit data;

a word line coupled to the plurality of memory cells; and

a controller that executes a read operation for reading data from the plurality of memory cells by applying a read voltage to the word line,

wherein:

the controller performs control such that numbers of times the controller applies read voltages different from one another to the word line in read operations for the first page, the second page, the third page, the fourth page, and the fifth page are 7, 6, 6, 6, and 6, respectively

the 5-bit data is one of a plurality of data sets including a first data set to a 32nd data set different from one another, the threshold voltage of the memory cell

being included in one of a first state to a 32nd state different from one another, and the plurality of data sets being respectively allocated to the first state to the 32nd state, so that adjacent states are different only in respect of one bit,

a first read voltage to a 31st read voltage different from one another are set to correspond to adjacent states of the first state to the 32nd state, and

the controller performs control such that an interval between read voltages which the controller applies to the word line in a read operation for each of the first page to the fifth page corresponds to three states at minimum and eight states at maximum.

2. The memory device of claim 1, wherein one of a first condition and a second condition is satisfied,

the first condition being that a lowest read voltage for use in the read operation for the first page is set apart by one state from the first read voltage, which is the lowest of all the first read voltage to the 31st read voltage, and

the second condition being that a highest read voltage for use in the read operation for the first page is set apart by one state from the 31st read voltage, which is the highest of all the first read voltage to the 31st read voltage.

3. The memory device of claim 2, wherein none of the other one of the first condition and the second condition,

a third condition, a fourth condition, and a fifth condition are satisfied,

the third condition being that an interval between read voltages for use in the read operation for the first page corresponds to three states at minimum,

the fourth condition being that an interval between read voltages for use in a read operation for a page using the first read voltage or the 31st read voltage corresponds to three states at minimum, and

the fifth condition being that the first page to the fifth page include a page in which both the first read voltage and the 31st read voltage are used for a read operation.

4. The memory device of claim 1, wherein both of a second condition and a fourth condition are satisfied,

the second condition being that a highest read voltage for use in the read operation for the first page is set apart by one state from the 31st read voltage, which is the highest of all the first read voltage to the 31st read voltage, and

the fourth condition being that an interval between read voltages for use in a read operation for a page using the first read voltage or the 31st read voltage corresponds to three states at minimum.

5. The memory device of claim 4, wherein none of a first condition, a third condition, and a fifth condition are satisfied,

the first condition being that a lowest read voltage for use in the read operation for the first page is set apart by one state from the first read voltage, which is the lowest of all the first read voltage to the 31st read voltage,

the third condition being that an interval between read voltages for use in the read operation for the first page corresponds to three states at minimum, and

the fifth condition being that the first page to the fifth page include a page in which both the first read voltage and the 31st read voltage are used for a read operation.

6. The memory device of claim 1, wherein all of a first condition, a second condition, and a third condition are satisfied,

the first condition being that a lowest read voltage for use in the read operation for the first page is set apart by one state from the first read voltage, which is the lowest of all the first read voltage to the 31st read voltage,

the second condition being that a highest read voltage for use in the read operation for the first page is set apart by one state from the 31st read voltage, which is the highest of all the first read voltage to the 31st read voltage, and

the third condition being that an interval between read voltages for use in the read operation for the first

page corresponds to three states at minimum.

7. The memory device of claim 6, wherein neither of a fourth condition and a fifth condition is satisfied,

the fourth condition being that an interval between read voltages for use in a read operation for a page using the first read voltage or the 31st read voltage corresponds to three states at minimum, and

the fifth condition being that the first page to the fifth page include a page in which both the first read voltage and the 31st read voltage are used for a read operation.

8. The memory device of claim 1, wherein all of a second condition, a third condition, and a fourth condition are satisfied,

the second condition being that a highest read voltage for use in the read operation for the first page is set apart by one state from the 31st read voltage, which is the highest of all the first read voltage to the 31st read voltage,

the third condition being that an interval between read voltages for use in the read operation for the first page corresponds to three states at minimum, and

the fourth condition being that an interval between read voltages for use in a read operation for a page using the first read voltage or the 31st read voltage corresponds to three states at minimum.

9. The memory device of claim 1, wherein all of a first condition, a second condition, a third condition, and a fourth condition are satisfied,

the first condition being that a lowest read voltage for use in the read operation for the first page is set apart by one state from the first read voltage, which is the lowest of all the first read voltage to the 31st read voltage,

the second condition being that a highest read voltage for use in the read operation for the first page is set apart by one state from the 31st read voltage, which is the highest of all the first read voltage to the 31st read voltage,

the third condition being that an interval between read voltages for use in the read operation for the first page corresponds to three states at minimum, and

the fourth condition being that an interval between read voltages for use in a read operation for a page using the first read voltage or the 31st read voltage corresponds to three states at minimum.

10. The memory device of claim 9, wherein a fifth condition is not satisfied,

the fifth condition being that the first page to the fifth page include a page in which both the first read voltage and the 31st read voltage are used for a read operation.

11. The memory device of claim 1, wherein both of a

third condition and a fifth condition are satisfied,

the third condition being that an interval between read voltages for use in the read operation for the first page corresponds to three states at minimum, and

the fifth condition being that the first page to the fifth page include a page in which both the first read voltage and the 31st read voltage are used for a read operation.

12. The memory device of claim 11, wherein none of a first condition, a second condition, and a fourth condition are satisfied,

the first condition being that a lowest read voltage for use in the read operation for the first page is set apart by one state from the first read voltage, which is the lowest of all the first read voltage to the 31st read voltage,

the second condition being that a highest read voltage for use in the read operation for the first page is set apart by one state from the 31st read voltage, which is the highest of all the first read voltage to the 31st read voltage, and

the fourth condition being that an interval between read voltages for use in a read operation for a page using the first read voltage or the 31st read voltage corresponds to three states at minimum.

13. A memory device comprising:

a plurality of memory cells each storing 5-bit data

including first bit data, second bit data, third bit data, fourth bit data, and fifth bit data based on a threshold voltage, the plurality of memory cells storing a first page, a second page, a third page, a fourth page, and a fifth page, and the first page, the second page, the third page, the fourth page, and the fifth page respectively including the first bit data, the second bit data, the third bit data, the fourth bit data, and the fifth bit data;

a word line coupled to the plurality of memory cells; and

a controller that executes a read operation for reading data from the plurality of memory cells by applying a read voltage to the word line,

wherein:

the controller performs control such that numbers of times the controller applies read voltages different from one another to the word line in read operations for the first page, the second page, the third page, the fourth page, and the fifth page are 7, 6, 6, 6, and 6, respectively,

the 5-bit data is one of a plurality of data sets including a first data set to a 32nd data set different from one another, the threshold voltage of the memory cell being included in one of a first state to a 32nd state different from one another, and the plurality of data sets being respectively allocated to the first state to the 32nd state, so that adjacent states are different only in

respect of one bit,

a first read voltage to a 31st read voltage different from one another are set to correspond to adjacent states of the first state to the 32nd state, and

the controller performs control such that an interval between read voltages which the controller applies to the word line in a read operation for each of the first page to the fifth page corresponds to three states at minimum and nine states at maximum.

14. The memory device of claim 13, wherein an interval between read voltages in the read operation for the first page comprises only four states.

15. A memory device comprising:

a plurality of memory cells each storing 5-bit data including first bit data to fifth bit data based on a threshold voltage, the plurality of memory cells storing a first page to a fifth page respectively corresponding to the first bit data to the fifth bit data;

a word line coupled to the plurality of memory cells; and

a controller that executes a read operation,

wherein:

a threshold voltage of the memory cells is included in one of a first state to a 32nd state different from one another,

pieces of 5-bit data different from one another being allocated to each of the first state to the 32nd state, a

first read voltage to a 31st read voltage are set to adjacent states of the first state to the 32nd state in ascending order of read voltage, and

the controller is configured to perform control comprising:

in the read operation for the first page, executing seven reads of respectively applying the fourth read voltage, the eighth read voltage, the 12th read voltage, the 18th read voltage, the 22nd read voltage, the 26th read voltage, and the 30th voltage to the word line;

in the read operation for the second page, executing six reads of respectively applying the sixth read voltage, the 13th read voltage, the 16th read voltage, the 20th read voltage, the 23rd read voltage, and the 28th read voltage to the word line;

in the read operation for the third page, execute six reads of respectively applying the third read voltage, the ninth read voltage, the 15th read voltage, the 21st read voltage, the 27th read voltage, and the 31st read voltage to the word line;

in the read operation for the fourth page, executing six reads of respectively applying the second read voltage, the seventh read voltage, the 10th read voltage, the 14th read voltage, the 17th read voltage, and the 24th read voltage to the word line; and

in the read operation for the fifth page, executing six reads of respectively applying the first read

voltage, the fifth read voltage, the 11th read voltage, the 19th read voltage, the 25th read voltage, and the 29th read voltage to the word line.

16. The memory device of claim 15, wherein each of the first read voltage and the second read voltage is negative.

17. The memory device of claim 15, wherein, in the read operation for the first page, the controller applies the 30th read voltage, the 26th read voltage, the 22nd read voltage, the 18th read voltage, the 12th read voltage, the eighth read voltage, and the fourth voltage to the word line in this order.