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- (71) **Applicant:** ENTROPICA LABS [SG/SG]; 186b Telok Ayer Street, Singapore 068632 (SG).
- (72) **Inventors:** CHAI, Jing Hao; 186b Telok Ayer Street, Singapore 068632 (SG). DISILVESTRO, Leonardo; 186b Telok Ayer Street, Singapore 068632 (SG). MUNRO, Ewan Franek; 186b Telok Ayer Street, Singapore 068632 (SG). SOTIROPOULOS, Georgios; 186b Telok Ayer Street, Singapore 068632 (SG). BORNHEIMER, Ulrike; 186b Telok Ayer Street, Singapore 068632 (SG). SHARMA, Vishal; 186b Telok Ayer Street, Singapore 068632 (SG). NUR, Shahidee Bin Saharan; 186b Telok Ayer Street, Singapore 068632 (SG). POIRIER, Kilian; 186b Telok Ayer Street, Singapore 068632 (SG). VIGNAROLI, Luca; 186b Telok Ayer Street, Singapore 068632 (SG).
- (74) **Agent:** SPRUSON & FERGUSON (ASIA) PTE LTD; 152 Beach Road, #37-05/06 Gateway East, Singapore 189721 (SG).
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(54) **Title:** A SYSTEM AND METHOD FOR QUANTUM ERROR CORRECTION CIRCUIT VERIFICATION

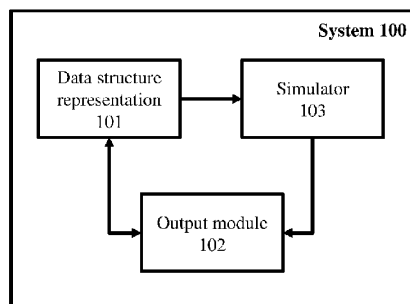


Figure 1A

(57) **Abstract:** Systems and methods disclosed herein relate to verification of quantum error correction circuits. A system for verification of quantum error correction circuits comprises a data structure representation configured to receive and/or store a quantum error correction code, an operation performed within the quantum error correction code, and an input circuit. The system further comprises an output module configured to prepare simulations of the input circuit, a simulator configured to simulate the input circuit, and wherein the output module is further configured to output at least one Boolean variable indicating whether the input circuit passes error correction circuit verification (ECCV) conditions, wherein the output module is further configured to provide debugging information when at least one Boolean variable indicates the input circuit fails at least one of the ECCV conditions.

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