

THIN FILM TRANSISTOR FABRICATION METHOD, ACTIVE
MATRIX SUBSTRATE FABRICATION METHOD, AND LIQUID CRYSTAL
DISPLAY DEVICE

Field of Invention

5 The present invention relates to technology for the formation of a gate insulation film for a thin film transistor (henceforth, TFT) used as the active element of a liquid crystal display, and to a liquid crystal display.

Related Art

10 Regarding methods of fabrication of thin film transistors (TFT) used as the active elements in liquid crystal displays, from the viewpoint of devising the increase of surface area and the reduction of cost, low-temperature processes and the use of inexpensive glass
15 substrates are desirable. In such a low-temperature process, in addition to the ability to form large-particle polysilicon films that rival those of high-temperature processes, and to activate the impurities sufficiently being necessary, it is important to be able to form high-
20 quality gate insulation films having a film quality equal to or greater than thermal oxide films.

 As technology for forming gate insulation films at low temperatures, there have been from the past film formation methods such as normal-pressure CVD, reduced-
25 pressure CVD, and the like. Normal-pressure CVD and reduced-pressure CVD are high in productivity, but the film quality as gate insulation films is inferior. For example, there are such problems as the increase of the space charge and interfacial charge in silicon oxide
30 films, the decrease of the on current properties, the decrease of the off-leakage current properties, and the shift of the threshold voltage of TFTs. Also, in the ECR-CVD method, the film quality is comparatively good, but there is a problem that the productivity is markedly low,
35 and all of the prior film formation methods do not satisfy the conditions for film formation of TFT gate insulation films used for the active elements of liquid crystal displays.

Also, as a low-temperature process for forming silicon oxide films, other than the above-mentioned film formation methods, there is also the plasma chemical vapor deposition method (plasma CVD method). The plasma CVD method is a film formation method whereby a film is formed by causing a discharge in a feed gas within a reaction chamber by applying a high frequency between electrodes, and causing a reaction to break down the feed gas with the plasma formed thereby. Because such a film formation method has the advantages of a high film formation speed, a low stress applied to the substrate, a good step coverage, and the like, it has been used up to the present for the formation of layer insulation films of semiconductor integrated circuits. Also, as published in *Sharp Giho* (Sharp Technical Journal) (No. 61, April 1995), it is coming to be seen as a film formation method for forming TFT gate insulation films as well. The conditions of the plasma CVD method examined here are that the interelectrode distance for generating the plasma is within the range of 35mm to 65mm, and the pressure inside the reaction chamber is in the range of 800mtorr to 1200mtorr, and conditions having exceeded such ranges are not suitable for forming TFT gate insulation films. Such is the gist of *Sharp Giho*, and others. The properties of film formation have been evaluated within the scope of such conditions because in addition to the space charge inside a silicon oxide film occurring more easily as the distance between the electrodes is made smaller, an interfacial layer is generated more easily on the surface of a semiconductor film in contact with the silicon oxide film. Furthermore, the on current properties and off-leakage current properties of the TFT are in a decreasing trend due to the presence of an interfacial charge originating in this interfacial layer. Further the properties have been evaluated within the scope of conditions mentioned above, because the on current properties and off-leakage current properties of the TFT

are in a decreasing trend as the pressure inside the reaction chamber is lowered.

However, the plasma CVD method has not arrived at the point where it genuinely can be applied to a TFT gate insulation film formation process as examined by changing various parameters within the above-mentioned scope of conditions. This is because when forming a TFT gate insulation film, which is different from depositing a silicon oxide film on a comparatively narrow substrate such as a silicon wafer and a layer insulation film, not only is the film formation speed high, the stress applied to the substrate low, and the step coverage satisfactory, but there are additional conditions inherent to this field. Namely since a TFT gate insulation film is being formed, the electrical properties related to the space charge and interfacial layer of the aforementioned silicon oxide film must be satisfactory. Moreover, it is desirable to be able to form evenly and at high speed a silicon oxide film on the entirety of a large-surface area substrate being 360mmx465mm, such as an active matrix of a liquid crystal display panel. However, by only applying the film formation conditions used in the formation of layer insulation films of semiconductor integrated circuits to the formation of TFT gate insulation films, the conditions mentioned above cannot be satisfied.

For example, following conditions are set when forming a silicon oxide film under the conventional technology in plasma CVD: the interelectrode distance is 35mm, the pressure in the reaction chamber is 1500mtorr, and the TEOS gas flow is 30SCCM or less. Setting the film formation conditions from the viewpoint of obtaining a silicon oxide film having satisfactory electrical properties related to the space charge and the interfacial layer, not only causes the film formation speed to drop markedly to about 250Angstrom/minute, if the value obtained from Equation (1) by the evaluation method explained below, which is expressed in terms of

irregularity of the film thickness, but also causes the result to be extremely high, being about 20% higher. Here, to be genuinely applicable to the formation process of a TFT gate insulation film, it is necessary to secure a film formation speed of 700Angstrom/minute or more, and to suppress irregularity of the film thickness to 7% or less.

In consideration of such problems, the object of the present invention is to provide a TFT fabrication method, being a low-temperature process, that can form at high film formation speed and have an even film thickness across a large-surface area substrate to produce a high-quality gate insulation film having satisfactory charge behavior.

DISCLOSURE OF THE INVENTION

In order to solve the above-mentioned problems, the inventors of the present invention have performed repeated examinations regarding the conditions up to now thought not to apply as conditions for forming films as gate insulation films in the plasma CVD method. As a result, it was discovered that a silicon oxide film suitable as a TFT gate insulation film can be formed within the scope of such conditions, and the use of a silicon oxide film formed under such film formation conditions as a TFT gate insulation film is proposed.

The invention as defined in Claim 1 of the present invention is a method of fabricating a thin film transistor having a gate electrode abutting against a channel region through a gate insulation film, wherein the gate insulation film formation process forms a silicon oxide film by using tetraethoxysilane, a.k.a. TEOS, as the gas to provide the silicon, and by using plasma chemical vapor deposition under the condition that the interelectrode distance for generating the plasma is about 15mm or less.

Given this condition, it is possible to improve the electrical film properties of charge behavior without

sacrificing the film formation speed and the uniformity of the film thickness. Therefore, it is possible to fabricate on a large substrate and at high productivity a TFT having stable on current properties and off-leakage current properties.

Also, the invention of Claim 3 is a method of fabricating a thin film transistor having a gate electrode abutting against a channel region through a gate insulation film, wherein the gate insulation film formation process forms a silicon oxide film by using tetraethoxysilane as the gas to provide the silicon, and by using plasma chemical vapor deposition under the condition that the reaction chamber is at a low pressure of 700mtorr or less.

Given this condition of the electrical film properties of film formation speed and charge behavior, it is possible to improve the latter without greatly sacrificing the former. Furthermore, in this case the uniformity of film thickness is not sacrificed. Therefore, it is possible to fabricate on a large substrate and at high productivity a TFT having stable on current properties and off-leakage current properties.

Also, the invention of Claim 5 is the thin film transistor fabrication method of Claim 1, wherein the gate insulation film formation process forms a silicon oxide film by using tetraethoxysilane as the gas to provide the silicon, and by using plasma chemical vapor deposition under the condition that the reaction chamber is at a low pressure of 700mtorr or less.

Given this condition, it is possible to improve the uniformity of film thickness as the electromagnetic power (power source output) printed between the electrodes is made smaller, and there is substantially no sacrificing of the electrical film properties of film formation speed and charge behavior.

Moreover, the invention of Claim 7 is the thin film transistor fabrication method of any of the claims 1

through 5, wherein the gate insulation film formation process forms a silicon oxide film by using oxygen gas as the feed gas to provide oxygen.

Moreover, the invention of Claim 10 is the active matrix substrate fabrication method as defined in Claim 9, including a capacitive-dividing type digital/analog converter.

Given this fabrication method, it becomes possible to digitize the signal generator that provides signals to the active matrix substrate, and it becomes possible to provide a liquid crystal device having low power consumption.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a process section modeling one example of a TFT fabrication process.

Fig. 2 is a summary plane drawing of the vicinity of the reaction chamber of a plasma chemical vapor deposition apparatus.

Fig. 3 is a section in the A-A' line of Fig. 2.

Fig. 4 is a graph showing the relationship between substrate temperature and film formation speed during film formation in a preferred embodiment (Examination 1) of the present invention.

Fig. 5 is a graph showing the relationship between substrate temperature and shift from the ideal flat band voltage during film formation in a preferred embodiment (Examination 1) of the present invention.

Fig. 6 is a graph showing the relationship between substrate temperature and irregularity of the film thickness during film formation in a preferred embodiment (Examination 1) of the present invention.

Fig. 7 is a graph showing the relationship between the flow of oxygen gas and film formation speed during film formation in a preferred embodiment (Examination 2) of the present invention.

Fig. 8 is a graph showing the relationship between the flow of oxygen gas and shift from the ideal flat band

voltage during film formation in a preferred embodiment (Examination 2) of the present invention.

Fig. 9 is a graph showing the relationship between the flow of oxygen gas and irregularity of the film thickness during film formation in a preferred embodiment (Examination 2) of the present invention.

Fig. 10 is a graph showing the relationship between the flow of TEOS gas and film formation speed during film formation in a preferred embodiment (Examination 3) of the present invention.

Fig. 11 is a graph showing the relationship between the flow of TEOS gas and shift from the ideal flat band voltage during film formation in a preferred embodiment (Examination 3) of the present invention.

Fig. 12 is a graph showing the relationship between the flow of TEOS gas and irregularity of the film thickness during film formation in a preferred embodiment (Examination 3) of the present invention.

Fig. 13 is a graph showing the relationship between the flow of RF source power (output) and film formation speed during film formation in a preferred embodiment (Examination 4) of the present invention.

Fig. 14 is a graph showing the relationship between the flow of RF source power (output) and shift from the ideal flat band voltage during film formation in a preferred embodiment (Examination 4) of the present invention.

Fig. 15 is a graph showing the relationship between the flow of RF source power (output) and irregularity of the film thickness during film formation in a preferred embodiment (Examination 4) of the present invention.

Fig. 16 is a graph showing the relationship between pressure of the reaction chamber and film formation speed during film formation in a preferred embodiment (Examination 5) of the present invention.

Fig. 17 is a graph showing the relationship between pressure of the reaction chamber and shift from the ideal flat band voltage during film formation in a preferred embodiment (Examination 5) of the present invention.

Fig. 18 is a graph showing the relationship between pressure of the reaction chamber and irregularity of the film thickness during film formation in a preferred embodiment (Examination 5) of the present invention.

Fig. 19 is a graph showing the relationship between interelectrode distance and film formation speed during film formation in a preferred embodiment (Examination 6) of the present invention.

Fig. 20 is a graph showing the relationship between interelectrode distance and shift from the ideal flat band voltage during film formation in a preferred embodiment (Examination 6) of the present invention.

Fig. 21 is a graph showing the relationship between interelectrode distance and irregularity of the film thickness during film formation in a preferred embodiment (Examination 6) of the present invention.

Fig. 22 is a graph showing the relationship between the flow of RF source power (output) and film formation speed when the pressure of the reaction chamber is 600mtorr and 650mtorr during film formation in a preferred embodiment (Examination 7) of the present invention.

Fig. 23 is a graph showing the relationship between the flow of RF source power (output) and shift from the ideal flat band voltage when the pressure of the reaction chamber is 600mtorr and 650mtorr during film formation in a preferred embodiment (Examination 7) of the present invention.

Fig. 24 is a graph showing the relationship between the flow of RF source power (output) and irregularity of the film thickness when the pressure of the reaction chamber is 600mtorr and 650mtorr during film

formation in a preferred embodiment (Examination 7) of the present invention.

Fig. 25 is a graph showing the relationship between the flow of RF source power (output) and film formation speed when the temperature of the reaction chamber is 300°C and 313°C during film formation in a preferred embodiment (Examination 8) of the present invention.

Fig. 26 is a graph showing the relationship between the flow of RF source power (output) and shift from the ideal flat band voltage when the temperature of the reaction chamber is 300°C and 313°C during film formation in a preferred embodiment (Examination 8) of the present invention.

Fig. 27 is a graph showing the relationship between the flow of RF source power (output) and irregularity of the film thickness when the temperature of the reaction chamber is 300°C and 313°C during film formation in a preferred embodiment (Examination 8) of the present invention.

Fig. 28 is a graph showing the relationship between pressure of the reaction chamber and film formation speed, explaining the scope of examination of the present invention.

Fig. 29 is a graph showing the relationship between on current and a gate insulation film of a TFT.

Fig. 30 is a graph showing the relationship between off current and a gate insulation film of a TFT.

Fig. 31 is a drawing showing a circuit equivalent to one pixel of a liquid crystal device using a TFT.

Fig. 32 is a graph showing the relationship between annealing temperature and shift from the ideal flat band voltage after film formation in a preferred embodiment (Examination 9) of the present invention.

Fig. 33 is a drawing showing a circuit equivalent to an active matrix substrate in a preferred embodiment (Examination 10) of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention is explained below, referring to the drawings.

[One Example of a TFT Fabrication Method]

5 The present invention has special features in the gate insulation film formation process within the TFT fabrication method. But before giving an explanation of these special features, a general TFT fabrication method is explained, referring to Fig. 1.

10 In Fig. 1(a), first, an undercoating protective layer 12 (silicon oxide film) of a film thickness of 1000-3000Angstrom, preferably 2000Angstrom, is formed by plasma CVD on the surface of a glass substrate 11. The feed gases at this time are TEOS gas and oxygen gas. The
15 undercoating protective layer 12 can be formed by other CVD methods. Also, an insulation film of silicon nitride film, and the like, or a multi-layer film of such can be used as well.

20 Next, an intrinsic silicon film 13 (amorphous silicon film) is deposited to the extent of 600Angstrom on the surface of the undercoating protective layer 12. For example, polycrystallization of the silicon film 13 is performed by solid phase growth for 24 hours at a processing temperature of 600°C. In such
25 polycrystallization can be used laser annealing and rapid thermal processing (RTA), and the like, at still lower processing temperatures. Thereafter, the silicon film 13 is processed to a specified shape using photolithography technology.

30 Next, on the silicon film 13 is formed a 300-3000Angstrom, preferably 1200Angstrom, gate insulation film 14 made of silicon oxide film. In this process, the silicon oxide film is formed by plasma CVD by a low-temperature process having a film formation temperature of
35 400°C or less. The feed gases at this time are tetraethoxysilane ($\text{Si}-(\text{O}-\text{CH}_2-\text{CH}_3)_4$), a.k.a. TEOS gas, and

oxygen gas, the tetraethoxysilane providing the silicon and the oxygen gas providing the oxygen.

Next, on the surface of the gate insulation film 14 is formed a tantalum thin film of 6000Angstrom film thickness by sputtering. Then it is patterned using photolithography technology, and a gate electrode 15 is formed as shown in Fig. 1(c). The tantalum thin film can be formed also by CVD, or the like.

Next, using a bucket-type non-quality-separating ion implantation apparatus (ion doping apparatus), impure ions are implanted in the silicon film 13 from the top of the gate insulation film as a mask of the gate electrode 15. As a result, source/drain regions 16 are formed self-aligning in relation to the gate electrode 15. At this time, the part within the silicon film 13 not having the impure ions implanted becomes the channel region 17. In this example, phosphine (PH_3) gas diluted with hydrogen gas to a density of 5% is used, and the accelerated voltage is 100keV. The total quantity of ions is $1 \times 10^{16} \text{ cm}^{-2}$. When forming a P-channel TFT, diborane (B_2H_6) diluted with hydrogen gas to a density of 5% is used. Also, it is possible also to implant the impurities at this time by etching a part or all of the gate insulation film on the source/drain part. Furthermore, it is possible also to perform the implantation of the impure ions by using a quality-separating ion implantation apparatus as commonly used in the fabrication of semiconductor integrated circuits.

Next, as shown in Fig. 1(d), a silicon oxide film of 5000Angstrom film thickness is formed by plasma CVD as an interfacial insulation film 18. The feed gas at this time is TEOS gas and oxygen gas.

Next, thermal processing is performed for one hour at 300°C , and activation of the implanted impure ions and reforming of the interfacial insulation film 18 are performed. A thermal processing temperature in the range

from 300°C to 450°C is desirable, and an atmosphere of N₂, O₂ or H₂ is desirable.

Next, a contact hole 19 is formed in the interfacial insulation film 18. Thereafter, source/drain electrodes 10 are electrically connected to the source/drain region 16, and the TFT is formed.

The above-mentioned fabrication method is still only an example, and low-density regions or offset regions may be provided in the regions abutting against the sides of the gate electrode 15. In either case, the gate insulation film (silicon oxide film) formation method explained below can be applied.

[Configuration of a Plasma Chemical Vapor Deposition Apparatus]

Of all the processes for fabricating TFTs, the present example uses a plasma CVD apparatus (plasma chemical vapor deposition apparatus) as shown in Fig. 2 and Fig. 3 in the gate insulation film formation process.

Fig. 2 is a summary plane drawing of the vicinity of the reaction chamber of a plasma CVD apparatus, and Fig. 3 is a section in the A-A' line of the apparatus.

In these drawings, the plasma CVD apparatus 200 of the present example is a capacitive-coupling type such that the plasma is generated using high-frequency power between parallel flat electrodes.

In the plasma CVD apparatus 200, a reaction chamber 201 is isolated from the outside air by a reaction vessel 202, and throughout film formation it is placed in a reduced pressure state from about 5mtorr to about 5torr. Inside the reaction vessel 202 are placed a lower flat electrode 203 and an upper flat electrode 204 in parallel to each other, and these two electrodes constitute the parallel flat electrodes. Between the parallel flat electrodes consisting of the lower flat electrode 203 and the upper flat electrode 204 is the reaction chamber 201. In this example, 410mmx510mm parallel flat electrodes are used, and the distance between the electrodes is variable.

The capacity of the reaction chamber 201 too is variable in the range from 2091cm^3 to 10455cm^3 according to variation of the distance between the electrodes. The variation of the distance between the electrodes can be performed by raising and lowering the position of the lower flat electrode 203, and any distance can be set. The change of the distance between the electrodes in the inner surfaces of the parallel flat electrodes is a mere 0.1mm when the distance between the electrodes is a given value. Consequently, the change of the field strength occurring between the electrodes is 1.0% or less in the inner surfaces of the parallel flat electrodes, and the plasma is generated evenly in the reaction chamber 201.

On top of the lower flat electrode 203 is placed a large-scale glass substrate 205 for deposition of the thin film, and 2mm of the insulated part of the substrate 205 is pressed against by a shadow frame 206. In Fig. 2, the shadow frame 206 is omitted so that the configuration of the apparatus would be easy to understand.

Inside the lower flat electrode 203 is provided a heater 207 for heating the substrate 205, and the temperature of the lower flat electrode 203 can be set arbitrarily between 25°C to 400°C . When the temperature of the electrode has been set to a given value, the temperature distribution within the inner surface of the lower flat electrode 203 excluding a 5mm perimeter is within $\pm 1^\circ\text{C}$ in relation to the set temperature, and the substrate temperature can be controlled to heat uniformly.

The shadow frame 206, for example, when using a general-purpose glass substrate (e.g., 7059 made by Corning Japan, OA-2 made by Nippon Electric Glass, or NA35 made by NH Techno Glass, etc.) as the substrate 205, prevents bowing deformation of the substrate 205 due to the heat from the heater 207, and in addition, it presses the substrate 205 such that useless thin film is not formed on the edges and underneath of the substrate.

The reaction gas consisting of the gas to be the feed gas and an additional gas according to need is introduced inside the upper flat electrode 204 through piping 208, and furthermore, it flows into the reaction chamber 201 at a substantially uniform pressure from the front of the upper flat electrode 204 by escaping through gas diffusion plates 209 provided inside the upper flat electrode 204. During film formation, a part of the reaction gas is separated at the point it has issued from the upper flat electrode 204, and a plasma is generated between the parallel flat electrodes. A part to all of the reaction gas contributes to the film formation. As opposed to this, the residual reaction gas not having contributed to the film formation and the gas caused as a result of the chemical reactions of the film formation are exhausted as exhaust gas from exhaust holes 210 provided on the upper perimeter of the reaction vessel 202.

The conductance of the exhaust holes 210 is desirably 100 times or more the conductance between the parallel flat electrodes. Furthermore, the conductance between the parallel flat electrodes is desirably much greater than the conductance of the gas diffusion plates 209, and still that value is desirably 100 times or more the conductance of the gas diffusion plates 209. By being configured in this manner, the reaction gas is introduced into the reaction chamber 201 at a substantially uniform pressure from the front of a large-scale, 410mmx510mm upper flat electrode 204, and simultaneously the exhaust gas is exhausted from the reaction chamber 201 at a uniform rate of flow in all directions.

The flow of the various types of reaction gases is adjusted to the specified values by a mass flow controller (not illustrated) before being introduced into the piping 208. Also, the pressure inside the reaction chamber 201 is adjusted to the specified value by a conductance valve 211 provided at the exit of the exhaust holes. On the exhaust side of the conductance valve 211 is provided a

vacuum exhaust apparatus (not illustrated) such as a turbo molecular pump. In the present example, an oil-free magnetic levitation type turbo molecular pump is provided as one part of the vacuum exhaust apparatus, and the degree of background vacuum inside the reaction chamber is at a level of 10^{-7} torr.

In Fig. 2 and Fig. 3, the gas flow is indicated by the arrows. The reaction vessel 202 and the lower flat electrode 203 are in grounded potential, and the electrically insulated state between these and the upper flat electrode 204 is maintained by an insulating ring 212. During plasma generation, after the RF waves output from the oscillating source 213 (power source) are amplified in an amplifier 214, they are printed on the upper flat electrode 204 via a matching circuit 215.

The plasma CVD apparatus 200 used in the present example is configured as a thin film formation apparatus applicable to large-scale, 400mm×500mm substrates by realizing extremely precise control of the distance between the electrodes and the flow of gas as described above. If these fundamental thoughts on design are followed, apparatuses can be easily configured to large-scale substrates such as 550mm×650mm.

In the present example, an RF power source was used, but power sources using microwaves and VHF waves also may be used. Also, the RF power source may be set to any wavelength being an integer multiple of the industrial RF wavelength (13.56MHz), such as 27.12MHz, 40.6MHz, 54.24MHz, 67.8MHz, etc. The modification of such wavelengths can be performed easily by exchanging the oscillation source 213, the amplifier 214, and the matching circuit 215. With the electromagnetic wave plasma, when the wavelength is increased, the electronic temperature within the plasma increases, and generation of radicals becomes easier.

[Results of Examination of Film Formation Conditions and Film Formation Properties]

In this example using such a plasma CVD apparatus, silicon oxide films were formed under the conditions shown in Table 1, and their film formation properties were evaluated. The results of each evaluation are shown in Fig. 4 through Fig. 27.

In these examinations, first, the amorphous silicon films are formed on 360mmx465mm substrates and made into polycrystalline silicon films by solid phase growth.

Next, the silicon oxide films were formed by plasma CVD on the surfaces of the polycrystalline silicon films while changing the film formation conditions as explained below. The film formation conditions in this plasma CVD method are: the silicon oxide films were formed by changing the flow of TEOS, the flow of oxygen, the distance between the electrodes of the parallel flat electrodes, the pressure (degree of vacuum) inside the reaction chamber, and the film formation time. In the following examinations, the frequency of the RF power source is fixed at 13.56MHz. During film formation, first a substrate is moved into the reaction chamber, and after momentarily drawing a vacuum, stabilization of the substrate temperature was performed for 5 minutes without providing the RF current under the gas flow and the reaction chamber pressure, which are the film formation conditions. After that, the RF source power is printed and film formation is performed. The stabilization time of the substrate temperature may be set to 10 minutes depending on the film formation conditions, and it is also possible to make the gas flow and the reaction chamber pressure different values with the film formation times. Also, it is possible to provide a preheating chamber separate from the reaction chamber, and to shorten the stabilization time of the substrate temperature to as few as 45 seconds to 1 minute by preheating the substrate temperature to as much as 300°C before moving the substrate into the film formation chamber.

Along with measuring the film formation speed (a film formation property), the film thickness after film formation was measured on a diagonal line in the region excluding 12mm from the ends. Irregularity of the film thickness (a film formation property) are also measured.

Among all the measurements pertaining to film thickness, those displayed with white circles in each graph (Fig. 4 through Fig. 27) showing the results are results measured by difference-in-levels measurement, and those displayed with black circles are results measured by ellipsometry.

As for the film formation speed, from the viewpoint of improving throughput, the higher the better, but a level of 700Angstrom/minute also is an allowable level. However, if the film formation speed is at this value or lower, industrial difficulties increase severely for the reasons below.

During film formation, the gases present inside the reaction chamber are tetraethoxysilane and oxygen supplied through the upper electrode and the gases generated by the reactions, but there are undesirable mixed gases in addition. The taking in of part of the mixed gases into the formed film, invites degradation of the film quality such as forming space charge, the loss of the film's insulating property, and the like. Such mixed gases are atmospheric leakage gases from the seams of the components constituting the reaction chamber, and back-flow gases of the vacuum exhaust apparatus, but if one attempts to avoid these completely, the plasma chemical vapor deposition apparatus becomes extremely costly, and the manufacturing cost of the thin film transistors is increased. Also, other mixed gases are detached gases having been attached to the walls of the reaction chamber. For said plasma chemical vapor deposition apparatus, in order to prevent the generation of particles caused by the peeling off of films formed on the walls, it is necessary to eliminate the films having attached to the walls of the

reaction chamber by etching them at high frequency. Because fluorine radicals generated by plasma decomposing such gases as nitrogen trifluoride, sulfur hexafluoride, and fluorine gas are used at that time, the fluorine and fluorine compounds produced at that time attach to the walls and become mixed gases. To avoid completely this phenomenon, after eliminating the films attached to the walls of the reaction chamber by etching, it is necessary to bake the walls of the reaction chamber for a long time, and this is not practical. Consequently, as a realistic method, it is necessary to supply a large quantity of feed gas compared with the mixed gases, and to perform film formation at a fast film formation speed. According to repeated film formation/film quality evaluation experiments, in order to prevent the degradation of film quality due to such mixed gases, a film formation speed of 300Angstrom/minute, preferably 700Angstrom/minute, was necessary.

Unevenness of the film thickness is evaluated by the value sought in the following equation.

$$\text{Unevenness of film thickness (\%)} = \frac{((\text{maximum value of film thickness} - \text{minimum value of film thickness}) / (\text{maximum value of film thickness} + \text{minimum value of film thickness})) \times 100 \dots \text{Equation (1)}}$$

It is desirable that the uniformity of the film thickness be 7% or less from the viewpoint of suppressing irregularities of the properties among TFTs.

Fig. 29 is a drawing showing the relationship between the film thickness of a TFT gate insulation film and the on current (drain current when gate voltage is 10V and drain voltage is 4V), and Fig. 30 is a drawing showing the relationship with the off current (drain current when gate voltage is 0V and drain voltage is 8V). The formation of the source/drain regions of the TFT at this time uses the aforementioned ion doping, and it was a method of implanting phosphorus at 100keV. If the gate

insulation film becomes 1320Angstrom or more, the on current decreases suddenly. This is because the density of the phosphorus implanted in the source/drain regions decreases by the gate insulation film becoming thicker.

5 Also, if the gate insulation film becomes 1080Angstrom or less, in addition to the on current decreasing, a severe increase in off current is seen. This is because a gap layer has occurred concomitant with the ion implantation on the semiconductor layer of the interface contacting the
10 channel region of the source/drain regions and contacting the silicon oxide film. It is well-known that, when performing doping of impurities by performing ion implantation, a gap layer occurs having a greatest gap density as much as 2/3 the depth of the depth showing the
15 maximum value of the ion density. When the gate insulation film is thin, this gap layer occurs inside the semiconductor layer and invites decreasing of the on current due to it working as an unnecessary resistance layer, and at the same time it invites the increase of off
20 current due to the leakage current generated across the gap. Consequently, it is necessary that the in-surface uniformity of the gate insulation film be at least $\pm 10\%$, also, when considering that the iterative precision of the average film thickness of the gate insulation films for
25 each film formation is 2-3%, it is desirable to be $\pm 7\%$ or less.

The application of pixel switching element of a liquid crystal display device can be mentioned as the most important application of thin film transistors. Fig. 31
30 shows an equivalent circuit corresponding to one pixel when assembling thin film transistors and liquid crystal elements. 311 is a thin film transistor, 312 is a liquid crystal element, 313 is a data signal wire supplying image signals, and 314 is a gate signal wire providing signals
35 to control the switching of the thin film transistor 311. For each field, when a new image signal is supplied from the data wire 313, and a signal from the gate signal wire

314 is supplied to the thin film transistor, the thin film transistor 311 becomes low resistance, and the voltage printed to the liquid crystal element 312 rewrites it to a new image signal. After that, an off signal from the signal wire 314 is supplied to the thin film transistor, the thin film transistor becomes high resistance, and the voltage of the liquid crystal element 312 is maintained until being rewritten by the next field. Not only does a thin film transistor have a resistance component, but it also has a capacitance component between each terminal, that is, between the gate electrode and the source electrode, and between the gate electrode and the drain electrode. Consequently, when a thin film transistor goes on/off, the voltage caused by the switching of the thin film transistor is also printed overlaid on the image signal of the liquid crystal element. When the capacitance component of each thin film transistor is not uniform for each pixel unit, a fixed pattern corresponding to the irregularity of the capacitance appears in the images, and the image quality is degraded significantly. A human can recognize a difference in brightness to as little as 1%, but in order that such a fixed pattern be at or below the perceptual limit, the irregularity of the gate insulation film that determines the irregularity of the capacitance component had to be at least $\pm 10\%$ or less, desirably $\pm 7\%$ or less. In short it is because, when selecting the size of the thin film transistor in the relationship of the liquid crystal element and the thin film transistor shown in Fig. 32 such that the writing operations and the maintenance operations of the thin film transistor are satisfactory, the capacitance ratio of the liquid crystal and the thin film transistor and the liquid crystal becomes as much as 10:1. Furthermore, the voltage ratio caused by the image signals written to the liquid crystal element and the switching of the thin film transistor becomes as much as 10:1.

In the thin film transistor fabrication process, and in all cases of the application of thin film transistors, the internal irregularity of the film thickness of the gate insulation film must be $\pm 10\%$ or less, preferably $\pm 7\%$ or less.

Also, of the electrical properties of the silicon oxide film used as the gate insulation film of the thin film transistor, regarding the space potential within the film and the interfacial charge of the film interface, the method of evaluation is easy by forming the insulation film on a silicon wafer in the manner as below, creating an MOS capacitor, measuring the relationship between its capacitance and the printed voltage, and evaluating it as the shift from the ideal flat band voltage (ΔV_{FB}).

This value can be obtained by the method below. First, after a silicon oxide film has been formed by plasma CVD on a silicon wafer, an aluminum electrode is created in a dot shape on this silicon oxide film. Next, a MOS capacitor is configured by connecting electrodes to the aluminum electrode and the silicon wafer, respectively, and after such, the shift from the ideal flat band voltage (ΔV_{FB}) is obtained from its capacitance-printed voltage properties. That is, ideally, it becomes flat band when the bias voltage (gate voltage) corresponds to the difference of the potentials of the aluminum and silicon connections. However, in actual elements there is a shift from the ideal flat band due to the existence of a space charge within the oxide film, and the existence of an interfacial charge caused by the interfacial level of the semiconductor surface in contact with the oxide film. Consequently, if the extent of such a shift is measured, it is possible to estimate with high correlation the internal quality of the element when the TFT has been configured.

Here, if a silicon oxide film having a small absolute value of the shift from the ideal flat band voltage (ΔV_{FB}) is used for a gate insulation film, the

electrical properties of the TFT element are satisfactory. If a silicon oxide film having a great absolute value of the shift from the ideal flat band voltage ($\Delta V_F.B$) is used, the on current properties and off leakage properties decrease.

Regarding these evaluation results, in a thermal oxide film formed in a comparatively high-temperature process, the shift from the ideal flat band voltage ($\Delta V_F.B$) is more or less $-0.6V$. In a low-temperature process, the shift from the ideal flat band voltage ($\Delta V_F.B$) should be a value of $-1.0V$ or higher on the minus side and a value of $1.0V$ or lower on the plus side, in short, the absolute value of $\Delta V_F.B$ should be $1V$ or less. The reason is because, as the shift from the ideal flat band voltage ($\Delta V_F.B$) shifts greater on the plus side, the on current of a type-N TFT decreases, and the off current of a type-P TFT increases. On the other hand, as the shift from the ideal flat band voltage ($\Delta V_F.B$) shifts greater on the minus side, the on current of a type-P TFT decreases, and the off current of a type-N TFT increases. Consequently, it is because a shift in either direction causes harm when configured as a CMOS circuit, such as the decrease of circuit operations and the increase of power consumption. Because the voltage required for switching on/off of a TFT is as little as $2-3V$, it is necessary to make the shift less than or equal to $\pm 1V$ due to the existence of a space charge inside the gate oxide film and an interfacial charge caused by the interfacial level of the semiconductor surface in contact with the oxide film. Also, if the interfacial level of the semiconductor surface in contact with the TFT gate oxide film becomes greater, a decrease in the sharpness of the rise in the on current of both a type-N TFT and a type-P TFT, an increase in off leakage, a rise in threshold voltage, and an increase in power consumption when configured as a CMOS circuit will be caused. However, examining the interfacial charge caused by the interfacial level of the

semiconductor surface in contact with the oxide film, using a silicon wafer, such degradation due to interfacial lecel is little enough to be ignored, if an oxide film TFT gate insulation film is used having an AVF.B of absolute value 1V or less.

Table 1

Conditions Division	[SCCM] Flow of TEOS	[SCCM] Flow of oxygen	POWER [W]	[mm]	[mToor]	[°C]
Examination 1 (Figs. 4~8)	120 Fixed to	3000 Fixed to	900 Fixed to	12.7 Fixed to	650 Fixed to	284~334
Examination 2 (Figs. 7~9)	120 Fixed to	1000~4000	900 Fixed to	12.7 Fixed to	650 Fixed to	300 Fixed to
Examination 3 (Figs. 10~12)	80~120	3000 Fixed to	900 Fixed to	12.7 Fixed to	650 Fixed to	300 Fixed to
Examination 4 (Figs. 13~15)	120 Fixed to	3000 Fixed to	900~1200	12.7 Fixed to	650 Fixed to	300 Fixed to
Examination 5 (Figs. 16~18)	120 Fixed to	3000 Fixed to	900 Fixed to	12.7 Fixed to	500~650	300 Fixed to
Examination 6 (Figs. 19~21)	120 Fixed to	3000 Fixed to	900 Fixed to	5.0~15.0	650 Fixed to	300 Fixed to
Examination 7 (Figs. 22~24)	120 Fixed to	3000 Fixed to	900~1200	12.7 Fixed to	600 650	300 Fixed to
Examination 8 (Figs. 25~27)	120 Fixed to	3000 Fixed to	900~1200	12.7 Fixed to	650 Fixed to	300 313

(Scope of Examination)

Fig. 28 makes clear the differences between the scope of examination of the film formation conditions and the prior art. The same figure is shown in a research report of a special interest group on applied electronic properties (Oyo Denshi Bussei Bunkakai), JSAP: AP922203 p. 7. In a plasma CVD method having TEOS and oxygen as the feed gases, a consequence of increasing the pressure of the reaction chamber is that the film formation speed increases. Once the maximum film formation speed is obtained the film formation speed decreases again. Such a change in film formation speed is thought to show an immediate change of scale of the film growth reaction around the same point having the maximum film formation speed. Consequently, around this point, the various parameters of the film formation speed and the film quality, namely, the pressure dependency, the substrate temperature dependency, the oxygen gas flow dependency,

the TEOS gas flow dependency, the RF power source dependency, and the interelectrode gap dependency can provide entirely different results. In the prior art, mainly a range of pressures greater than this pressure having the maximum film formation speed has been examined. In the present invention, a range of pressures less than this pressure having the maximum film formation speed has been examined. This pressure having the maximum film formation speed is dependent on the interelectrode gap. That is, when the interelectrode gap is small, the pressure at which the film formation speed is maximum moves to the high-pressure side. Fig. 28 is a graph showing the relationship between the film formation chamber pressure and the film formation speed when the interelectrode gap was 11.4mm, and it is possible to realize conditions whereby the film formation speed becomes greater when the pressure becomes greater within a wide pressure range. The flow of TEOS at this time was 120SCCM, the flow of oxygen was 3000SCCM, the RF source power was 900W, and the substrate temperature was 300°C. The present inventors have achieved good results by investigating in detail a scope of conditions different from the prior art, namely, a scope of film formation conditions with a small interelectrode gap and a low reaction chamber pressure, whereby the film formation speed becomes greater as the reaction chamber pressure becomes greater.

(Examination 1)

As shown in Table 1, in Examination 1, the flow of TEOS was set to 120SCCM, the flow of oxygen to 3000SCCM, and the RF source power was set to 900W, and differing from the prior art, the interelectrode distance of the parallel flat electrodes was set to the small value of 12.7 and the pressure of the reaction chamber to the low value of 650mtorr. The relationships between the substrate temperature during film formation and the film formation properties (film formation speed, shift from

ideal flat band voltage, irregularity of film thickness) were evaluated by changing the substrate temperature during film formation within the range of 284°C to 334°C. The results are shown in Fig. 4-Fig. 6.

As shown in Fig. 4-Fig. 6, when the substrate temperature during film formation was changed, the film formation speed and irregularity of film thickness were improved as the substrate temperature was lowered, but differing from the prior art, the shift from the ideal flat band voltage increased steadily as the substrate temperature was lowered.

(Examination 2)

As shown in Table 1, in Examination 2, the flow of TEOS was set to 120SCCM, the RF source power was set to 900W, and the substrate temperature during film formation was set to 300°C, and differing from the prior art, the interelectrode distance of the parallel flat electrodes was set to the small value of 12.7 and the pressure of the reaction chamber to the low value of 650mtorr. The relationships between the flow of oxygen and the film formation properties (film formation speed, shift from ideal flat band voltage, irregularity of film thickness) were evaluated by changing the flow of oxygen within the range of 1000SCCM-3000SCCM. The results are shown in Fig. 7-Fig. 9.

As shown in Fig. 7-Fig. 9, when the flow of oxygen was changed, the film formation speed improved as the flow of oxygen was made smaller, but the uniformity of the film thickness decreased.

The shift from the flat band voltage does not receive much influence from the flow of oxygen, but extremely high values appear.

(Examination 3)

As shown in Table 1, in Examination 3, the flow of oxygen was set to 3000SCCM, the RF source power was set to 900W, and the substrate temperature during film formation was set to 300°C, and differing from the prior art, the

interelectrode distance of the parallel flat electrodes was set to the small value of 12.7 and the pressure of the reaction chamber to the low value of 650mtorr. The relationships between the flow of oxygen [sic: TEOS] and the film formation properties (film formation speed, shift from ideal flat band voltage, irregularity of film thickness) were evaluated by changing the flow of TEOS within the range of 80SCCM-120SCCM. The results are shown in Fig. 10-Fig. 12.

As shown in Fig. 10-Fig. 12, when the flow of TEOS was changed, the film formation speed and the uniformity of the film thickness improved as the flow of TEOS was made greater, but the shift from the flat band increased. Regarding film quality, it was similar to the prior art.

(Examination 4)

As shown in Table 1, in Examination 4, the flow of TEOS was set to 120SCCM, the flow of oxygen was set to 3000SCCM, the interelectrode distance of the parallel flat electrodes was set to 12.7mm, the pressure of the reaction chamber was set to 650mtorr, and the substrate temperature during film formation was set to 300°C. The relationships between the RF source power and the film formation properties (film formation speed, shift from ideal flat band voltage, irregularity of film thickness) were evaluated by changing the RF source power within the range of 900W to 1200W. The results are shown in Fig. 13-Fig. 15.

As shown in Fig. 13-Fig. 15, even when changing the RF source power within the range of 900W to 1200W, the film formation speed does not change. Also, differing from the prior art, the shift from the flat band voltage does not change. Furthermore, the uniformity of the film thickness is improved as the power is made less. Under the conditions that the interelectrode distance of the parallel flat electrodes is 12.7 or less, and the pressure of the reaction chamber is 650mtorr, and the power is low, it is possible to improve the uniformity of the film

thickness without sacrificing the film formation speed, and without increasing the shift from the flat band voltage.

(Examination 5)

5 As shown in Table 1, in Examination 5, the flow of TEOS was set to 120SCCM, the flow of oxygen was set to 3000SCCM, the RF source power was set to 900W, the interelectrode distance of the parallel flat electrodes was set to 12.7mm, and the substrate temperature during
10 film formation was set to 300°C. The relationships between the pressure of the reaction chamber and the film formation properties (film formation speed, shift from ideal flat band voltage, irregularity of film thickness) were evaluated by changing the pressure of the reaction
15 chamber within the range of 500mtorr to 650mtorr. The results are shown in Fig. 16-Fig. 18.

 As shown in Fig. 16-Fig. 18, if the pressure of the reaction chamber is set within the range of 500mtorr to 650mtorr, the uniformity of the film thickness does not
20 change greatly, but the film formation speed is in a slightly improving trend as the pressure of the reaction chamber is made higher. At this time as well, the shift from the flat band voltage only becomes somewhat greater.

 Conversely, if the pressure of the reaction
25 chamber is set within the range of 500mtorr to 650mtorr, the uniformity of the film thickness does not change much, but the shift from the flat band is in a slightly decreasing trend as the pressure of the reaction chamber is lowered. At this time as well, the film formation
30 speed only becomes somewhat lower. If the pressure of the reaction chamber was further lessened to 400mtorr, the uniformity of the film thickness is in a somewhat worsening trend of $\pm 8\%$. This is because pursuant to the decreasing of the pressure in the reaction chamber, the
35 thermal contact with the lower flat electrode becomes less, and the temperature distribution inside the substrate is worsened. However, even in this case, if the

time of a raised temperature is made a little longer, up to 10 minutes, or if the pressure in the reaction chamber during stabilization of the substrate temperature is set to as little as 1torr, or if the substrate temperature is first heated to as much as 300°C in a preheating chamber, the uniformity of the film thickness could become $\pm 5\%$ or less. Furthermore, film formation at further lower pressures could not be achieved without changing the flow of the above-mentioned gases. When reducing the flow of gases and forming films in the same manner, the things that sacrifice the film formation speed are the uniformity of the film thickness and the small change in the shift from the flat band voltage. Also, when considering the stability of the plasma, a reaction chamber pressure of 100mtorr or more was preferable.

(Examination 6)

As shown in Table 1, in Examination 6, the flow of TEOS was set to 120SCCM, the flow of oxygen was set to 3000SCCM, the RF source power was set to 900W, the pressure in the reaction chamber was set to 650mtorr, and the substrate temperature during film formation was set to 300°C. The relationships between the interelectrode distance of the parallel flat electrodes and the film formation properties (film formation speed, shift from ideal flat band voltage, irregularity of film thickness) were evaluated by changing the interelectrode distance of the parallel flat electrodes within the range of 5.0mm to 15.00mm. The results are shown in Fig. 19-Fig. 21.

As shown in Fig. 19-Fig. 21, when the interelectrode distance of the parallel flat electrodes was changed, the film formation speed and the uniformity of the film thickness did not change much, but as the interelectrode distance of the parallel flat electrodes was made smaller, the shift from the flat band became markedly smaller, differing greatly from the prior art. That is, if the interelectrode distance of the parallel flat electrodes is within the range of 5.0mm to 12.7mm, it is possible to improve significantly the shift from the flat band without sacrificing the film formation speed and the uniformity of the film thickness. When the interelectrode distance is less than 5mm, the plasma state during ignition of the plasma becomes unstable and undesirable. However, this phenomenon can be avoided by correcting the ranges of operating settings of the matching circuit, and the like.

(Examination 7)

As shown in Table 1, in Examination 7, the flow of TEOS is set to 120SCCM, the flow of oxygen is set to 3000SCCM, the interelectrode distance of the parallel flat electrodes is set to 12.7mm, the pressure of the reaction chamber is set to 600mtorr or 650mtorr, and the substrate temperature during film formation is set to 300°C. The

relationships between the RF source power and the film formation properties (film formation speed, shift from ideal flat band voltage, irregularity of film thickness) were evaluated by changing the RF source power within the range of 900W to 1200W when the pressure of the reaction chamber was 600mtorr and 650mtorr, respectively. The results are shown in Fig. 22-Fig. 24.

As shown in Fig. 22-Fig. 24, if the power is reduced under the conditions whereby the interelectrode distance of the parallel flat electrodes is 12.7mm and the pressure of the reaction chamber is 650mtorr, whether the pressure of the reaction chamber is 600mtorr or 650mtorr, the uniformity of the film thickness can be improved. At this time, the film formation speed does not decrease. Also, the shift from the flat band voltage substantially does not increase when the pressure of the reaction chamber is 650mtorr, and even at 600mtorr, there is only a slight increase, and it can be checked to +1.0V or less. (Examination 8)

As shown in Table 1, in Examination 8, the flow of TEOS is set to 120SCCM, the flow of oxygen is set to 3000SCCM, the interelectrode distance of the parallel flat electrodes is set to 12.7mm, the pressure of the reaction chamber is set to 650mtorr, and the substrate temperature during film formation is set to 300°C or 313°C. The relationships between the RF source power and the film formation properties (film formation speed, shift from ideal flat band voltage, irregularity of film thickness) were evaluated by changing the RF source power within the range of 900W to 1200W when the substrate temperature during film formation was 300°C and 313°C, respectively. The results are shown in Fig. 25-Fig. 27.

As shown in Fig. 25-Fig. 27, if the power is lowered under the conditions whereby the interelectrode distance of the parallel flat electrodes is 12.7mm and the pressure of the reaction chamber is 650mtorr, whether the substrate temperature during film formation is 300°C or

313°C, it is possible to improve the uniformity of the film thickness, and even in this case, the film formation speed does not decrease. Also, when the substrate temperature during film formation is 300°C, there is no increase of the shift from the flat band voltage even when the power is reduced, and when the substrate temperature during film formation is 313°C, the shift from the flat band voltage becomes smaller as the power is reduced.

(Examination 9)

In Examination 9 as shown in Fig. 32, the flow of TEOS is set to 120SCCM, the flow of oxygen is set to 3000SCCM, the interelectrode distance of the parallel flat electrodes is set to 15mm, the pressure of the reaction chamber is set to 650mtorr, the substrate temperature during film formation is set to 300°C, and the RF source power is set to 900W. The annealing temperature and the shift from the flat band voltage were evaluated when having annealed for one hour after film formation. The film formation speed is 1230Angstrom/minute, and the irregularity of the film thickness is as low as 5%. The shift from the flat band voltage became smaller as the annealing temperature is raised. The annealing atmosphere is examined with nitrogen, oxygen, and hydrogen atmospheres, but there was no great difference. The effects of annealing similarly for various film formation conditions are examined, but when having formed the film under conditions indicating a small shift from the flat band voltage before annealing had the shift from the flat band voltage become even smaller, and there is no change in the size relationships before and after annealing.

(Examination 10)

In Examination 10, following the aforementioned examination results, an actual active matrix substrate for a liquid crystal display was created and its display capabilities were confirmed. The film formation conditions of the gate insulation film had the flow of TEOS set to 120SCCM, the flow of oxygen set to 3000SCCM,

the RF source power set to 900W, the interelectrode distance of the parallel flat electrodes set to 11.4mm, the pressure of the reaction chamber set to 650mtorr, and the substrate temperature during film formation set to 300°C. The film formation speed at this time was 1250Angstrom/minute and the irregularity of the film thickness was $\pm 5\%$.

The fundamental fabrication method of the TFT was as mentioned before, but in Examination 10, a 360mmx465mm sheet of OA-2 manufactured by Nippon Electrical Glass Corporation was used as the glass substrate, and the undercoating protective layer was made 2000Angstrom under the same film formation conditions as the gate insulation film. For the formation of the polycrystalline silicon film a laser annealing method is used, and for the formation of the source/drain regions an ion doping method is used. In addition, a pixel electrode made of indium tin oxide (ITO) was connected to one side of the source/drain electrode of each pixel TFT. In Examination 10, an active matrix substrate was manufactured having type N thin film transistors as the pixel switching elements of a 200 (rows) x 320 (columns) x 3 (colors) = 192,000 (pixels) color LCD, and having a 6-bit digital data driver (vertical driver) and a scanning driver (horizontal driver) installed in a CMOS thin film semiconductor device composed of type N and type P thin film transistors. In Fig. 33 is shown a circuit diagram of the 6-bit digital data driver. The digital data driver of the present preferred embodiment comprises a clock generator circuit, a shift register circuit, a NOR gate, a digital video signal wire, a latch circuit 1, a latch pulse wire, a latch circuit 2, a reset wire 1, an AND gate, a base potential wire, a reset wire 2, a capacitive-dividing 6-bit D/A converter, a CMOS analog switch, a common potential wire, and a source wire reset transistor, and the output from the CMOS analog switch is connected to the source wire of the pixel section. The capacitance of

the D/A converter is formed using the gate insulation film, which satisfies the relationship of $C_0=C_1/2=C_2/4=C_3/8=C_4/16=C_5/32$, and the intermediate tones are represented by combinations of this capacitance. Into the digital video signal wire the digital video signals are inputted from the video random access memory (VRAM) of a computer. A liquid crystal panel is manufactured using an active matrix substrate obtained in this manner on one side of a pair of substrates. For the liquid crystals sandwiched between the pair of substrates TN type liquid crystals are used, and are made as a normally-white (white display when voltage is not printed to the liquid crystals) liquid crystal panel. Since the present invention is characterized by the gate oxide film having a high uniformity, proof is conducted of the uniformity in such a liquid crystal panel being sensitive to the irregularity of the gate insulation film.

A liquid crystal display device was manufactured by connecting the obtained liquid crystal panel to external wiring. As a result, because the on resistance and transistor capacitance of the type N TFTs and the type P TFTs are variously equivalent. Furthermore, because the TFTs are high-performance, the parasitic capacitance of the transistors is extremely small, and the properties throughout the surface of the substrate are uniform, a liquid crystal display device was produced, with both the 6-bit digital driver and the scanning driver operating normally over a wide operating region, and having a high display quality. In particular, the spottiness of the intermediate tones concomitant with irregularity of the film thickness of the gate insulation film of concern was at or below the perceptual limit. Also, because the fabrication process of the active matrix substrate also was stable, it became possible to manufacture the liquid crystal display device with stability and at low cost.

Thus, in the TFT fabrication method of the present invention, it was confirmed that, when forming a gate

insulation film, when plasma chemical vapor deposition is used, when TEOS is used as the gas to provide the silicon, when the interelectrode distance for generating the plasma is made 12.7mm or less, and if the results of the evaluations conducted in the past are followed, it is possible to suppress the influence of the space charge in the film and the interfacial charge of the film interface without sacrificing the film formation speed and the uniformity of the film thickness, regardless of the scope of conditions that had been considered involved in the decrease of film properties. Also, it was confirmed that, according to the results of repeatedly performed additional annealing experiments, if the interelectrode distance for generating the plasma is made about 15mm, it is possible to reduce the influence of the charge inside the film and in the film interface without sacrificing the film formation speed and the uniformity of the film thickness. Consequently, following such film formation conditions, it is possible to form a silicon oxide film having film properties equal to or better than thermal oxide films while being a low-temperature process. Furthermore, it is possible to fabricate on large substrates at high productivity TFTs having stable on current properties and off leakage current properties. Therefore, according to the present example, it is possible to realize increased surface area and reduced cost of liquid crystal display panels, and the like.

In forming a gate insulation film when plasma chemical vapor deposition is used, TOES is used as the gas for providing the silicon, the pressure inside the reaction chamber is made 650mtorr or less, while being a low-temperature process, among the electrical film properties, it is possible to improve the charge behavior substantially without sacrificing the film formation speed. In this case as well, the uniformity of the film thickness was not sacrificed. Also, according to the results of repeatedly performed other experiments, it was

confirmed that, if the pressure inside the reaction chamber is made 700mtorr or less, it is possible to obtain the same results.

Furthermore, if the interelectrode distance of the parallel flat electrodes is made about 15mm or less, and if the pressure of the reaction chamber is under a condition of being about 700mtorr or less, although being a low-temperature process, the uniformity of the film thickness is improved as the power is made less. In this case as well, there was no decrease in film formation speed, and no increase in the shift from the flat band voltage.

It is desirable that the interelectrode distance of the parallel flat electrodes be 5mm or more, and that the pressure of the reaction chamber be 100mtorr or more.

As explained above, the TFT fabrication method pertaining to the present invention is a gate insulation film formation process, wherein plasma chemical vapor deposition is used, in addition, tetraethoxysilane is used as the gas to provide the silicon, and moreover, the interelectrode distance for generating the plasma is made about 15mm or less. According to such a process, if the results of the evaluations conducted in the past are followed, because it is possible to suppress the influence of the space charge in the film and the interfacial charge of the film interface without sacrificing the film formation speed and the uniformity of the film thickness, regardless of the scope of conditions that had been considered [involved in] the decrease of film properties, it is possible to form a silicon oxide film having film properties equal to or better than thermal oxide films while being a low-temperature process. Therefore, it is possible to fabricate on large substrates at high productivity TFTs having stable on current properties and off leakage current properties.

Also, in the gate insulation film formation process, when plasma chemical vapor deposition is used, in

addition, in this process, when TEOS is used as the gas for providing the silicon, and moreover, when the pressure inside the reaction chamber is made 650mtorr or less, while being a low-temperature process, of the electrical film properties of film formation speed and charge behavior, it is possible to improve the latter without greatly sacrificing the former. In this case as well, because the uniformity of the film thickness was not sacrificed, it is possible to fabricate on large substrates at high productivity TFTs having stable on current properties and off leakage current properties while being a low-temperature process.

Also, if the interelectrode distance of the parallel flat electrodes is made about 15mm or less, moreover, if the pressure of the reaction chamber is under a condition of being about 700mtorr or less, it is possible to improve the uniformity of the film thickness as the power is made less. Therefore, it is possible to fabricate on large substrates at high productivity TFTs having stable on current properties and off leakage current properties while being a low-temperature process.

Also, when fabricating an active matrix substrate by the said fabrication method, because the on resistance and transistor capacitance of the type N TFTs and the type P TFTs are variously equivalent, furthermore, because the TFTs are high-performance, moreover, because the parasitic capacitance of the transistors is extremely small, and in addition, because the properties throughout the surface of the substrate are uniform, a liquid crystal display device was produced, with both the 6-bit digital driver and the scanning driver operating normally over a wide operating region, and having a high display quality. In particular, the capacitive dividing 6-bit digital driver as well, whereby the spottiness of the intermediate tones concomitant with irregularity of the film thickness of the gate insulation film is a concern, operated normally while maintaining the spottiness of the intermediate tones at or

below the perceptual limit. Consequently, it became possible to digitize all the signals provided to the active matrix substrate, and a liquid crystal display device having little power consumption became possible. Also, because the active matrix substrate fabrication process also is stable, it became possible to fabricate liquid crystal display devices with stability and at low cost.

Utility in the Industry

The present invention is applicable to active matrix substrate and liquid crystal display fabrication processes, and in particular, to a gate insulation film fabrication process.



WHAT IS CLAIMED IS:

1. A thin film transistor fabrication method having a channel region connected to a source region and a drain region, and a gate electrode abutting against the channel region through a gate insulation film, wherein

the formation process of said gate insulation film forms a silicon oxide film by using tetraethoxysilane as the feed gas to provide the silicon, and by using plasma chemical vapor deposition under the condition that the interelectrode distance for generating the plasma is about 15mm or less.

2. The thin film transistor fabrication method as defined in Claim 1, wherein the formation process of said gate insulation film forms a silicon oxide film by using tetraethoxysilane as the feed gas to provide the silicon, and by using plasma chemical vapor deposition under the condition that the interelectrode distance for generating the plasma is about 5mm or more.

3. A thin film transistor fabrication method having a channel region connected to a source region and a drain region, and a gate electrode abutting against the channel region through a gate insulation film, wherein

the formation process of said gate insulation film forms a silicon oxide film by using tetraethoxysilane as the feed gas to provide the silicon, and by using plasma chemical vapor deposition under the condition that the inside of the reaction chamber is pressurized to less than 700mtorr.

4. The thin film transistor fabrication method as defined in Claim 3, wherein the formation process of said gate insulation film forms a silicon oxide film by using tetraethoxysilane as the feed gas to provide the silicon, and by using plasma chemical vapor deposition under the condition that the inside of the reaction chamber is pressurized to more than 100mtorr.

5. The thin film transistor fabrication method as defined in either Claim 1 or 2, wherein the formation

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process of said gate insulation film forms a silicon oxide film by using tetraethoxysilane as the feed gas to provide the silicon, and by using plasma chemical vapor deposition under the condition that the inside of the reaction chamber is pressurized to less than 700mtorr.

6. The thin film transistor fabrication method as defined in Claim 5, wherein the formation process of said gate insulation film forms a silicon oxide film by using tetraethoxysilane as the feed gas to provide the silicon, and by using plasma chemical vapor deposition under the condition that the inside of the reaction chamber is pressurized to more than 100mtorr.

7. The thin film transistor fabrication method as defined in any of Claims 1 through 6, wherein the formation process of said gate insulation film forms a silicon oxide film by using oxygen gas as the feed gas to provide the oxygen.

8. The thin film transistor fabrication method as defined in any of Claims 1 through 7 wherein the film thickness of said gate insulation film is 200-3000Angstrom.

9. An active matrix substrate fabrication method, whereby the active matrix substrate is fabricated by the thin film transistor fabrication method as defined in any of Claims 1 through 7.

10. An active matrix substrate fabrication method including a capacitive-dividing type digital/analog converter, whereby the active matrix substrate is fabricated by the active matrix substrate fabrication method as defined in Claim 9.

11. A liquid crystal display device, comprising an active matrix substrate fabricated by the active matrix substrate fabrication method as defined in either Claim 9 or 10, a corresponding substrate, liquid crystals, and drive signals for said active matrix substrate.

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