SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This patent application claims benefit of priority to Korean Patent Application No. 10-2022-0073469 filed on 16 June 2022 in the Korean Intellectual Property Office, the disclosure of which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] Example embodiments relate to a semiconductor device and a method of manufacturing the semiconductor device.

BACKGROUND

[0003] Research has been conducted to reduce the size of elements of a semiconductor device and to improve performance of the semiconductor device. For example, in memory devices such as Dynamic Random Access Memories (DRAMs), research has been conducted to reliably and stably form elements having reduced sizes.

SUMMARY

[0004] Example embodiments provide a semiconductor device having a high degree of integration.

[0005] Example embodiments provide a method of manufacturing the semiconductor device.

[0006] According to example embodiments, a semiconductor device may include a lower structure, first electrodes spaced apart from each other on the lower structure, a second electrode on the first electrodes, and a dielectric layer between the first

electrodes and the second electrode. Each of the first electrodes may include a first element, a second element, and nitrogen (N). A degree of stiffness of a first nitride material including the first element may be higher than a degree of stiffness of a second nitride material including the second element. Each of the first electrodes may include a region in which a ratio of a concentration of the first element in the region to a concentration of the second element in the region decreases in a horizontal direction, away from a side surface of each of the first electrodes. The horizontal direction may be parallel to an upper surface of the lower structure.

[0007] According to example embodiments, a semiconductor device may include a lower structure, a first electrode on the lower structure, a second electrode on the first electrode, and a dielectric layer between the first electrode and the second electrode. The first electrode may include a first region including at least a titanium (Ti) element, a niobium (Nb) element, and a nitrogen (N) element. In the first region of the first electrode, a concentration of the Nb element may increase in a horizontal direction, away from a side surface of the first electrode.

[0008] According to example embodiments, a semiconductor device may include a lower structure, a first electrode on the lower structure, a second electrode on the first electrode, and a dielectric layer between the first electrode and the second electrode. The first electrode may include a first region including at least three elements. The first region of the first electrode may include a first sub-region, and a second sub-region, wherein the first sub-region is between, in a horizontal direction, the second sub-region and a side surface of the first electrode. The first sub-region may include first layers and second layers alternately stacked in the horizontal direction. The second sub-region may include third layers and fourth layers alternately stacked in the horizontal direction. The first layers and the third layers may include a same first

material. The second layers and the fourth layers may include a same second material. A horizontal thickness of each of the second layers may be smaller than a horizontal thickness of each of the fourth layers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The above and other aspects, features, and advantages of the present inventive concept will be more clearly understood from the following detailed description, taken in conjunction with the accompanying drawings, in which:

[0010] FIGS. 1, 2, 3A, and 3B are schematic diagrams illustrating a semiconductor device according to an example embodiment;

[0011] FIG. 4A is a graph illustrating an example of a change in concentration of a second element in a semiconductor device according to an example embodiment;

[0012] FIG. 4B is a graph illustrating another example of a change in concentration of a second element in a semiconductor device according to an example embodiment;

[0013] FIG. 4C is a graph illustrating another example of a change in concentration of a second element in a semiconductor device according to an example embodiment;

[0014] FIG. 4D is a graph illustrating another example of a change in concentration of a second element in a semiconductor device according to an example embodiment;

[0015] FIG. 5A is a schematic partially enlarged view illustrating an example of a first electrode of a semiconductor device according to an example embodiment;

[0016] FIG. 5B is a schematic partially enlarged view illustrating a modification of a first electrode of a semiconductor device according to an example embodiment;

[0017] FIG. 6A is a schematic partially enlarged view illustrating a modification of a first electrode of a semiconductor device according to an example embodiment;

[0018] FIG. 6B is a schematic partially enlarged view illustrating a modification of a

first electrode of a semiconductor device according to an example embodiment;

[0019] FIG. 7A is a schematic partially enlarged view illustrating a modification of a first electrode of a semiconductor device according to an example embodiment;

[0020] FIG. 7B is a schematic partially enlarged view illustrating a modification of a first electrode of a semiconductor device according to an example embodiment;

[0021] FIGS. 8A and 8B are schematic partially enlarged views illustrating a modification of a first electrode of a semiconductor device according to an example embodiment;

[0022] FIG. 9 is a schematic partially enlarged view illustrating a modification of a first electrode of a semiconductor device according to an example embodiment;

[0023] FIGS. 10 and 11 are schematic diagrams illustrating a modification of a semiconductor device according to an example embodiment;

[0024] FIG. 12 is a schematic top view illustrating a modification of a semiconductor device according to an example embodiment; and

[0025] FIGS. 13, 14 and 15 are cross-sectional views illustrating an example of a method of forming a semiconductor device according to an example embodiment.

DETAILED DESCRIPTION

[0026] Hereinafter, terms such as "upper portion," "middle portion," and "lower portion" may be replaced with other terms, for example, "first," "second," and "third" to describe components of the specification. Terms such as "first," "second," and "third" may be used to describe different components, but the components are not limited by the terms, and a "first component" may be referred to as a "second component."

[0027] An example of a semiconductor device according to an example embodiment will be described with reference to FIGS. 1 and 2. FIGS. 1 and 2 are schematic

diagrams illustrating a semiconductor device according to an example embodiment. In FIGS. 1 and 2, FIG. 1 is a schematic top view illustrating a semiconductor device according to an example embodiment, and FIG. 2 is a schematic cross-sectional view illustrating regions taken along lines I-I' and II-II' of FIG. 1.

[0028] Referring to FIGS. 1 and 2, the semiconductor device 1 according to an example embodiment may include a lower structure LS and an upper structure US on the lower structure LS.

[0029] The lower structure LS may include a substrate 5, active regions 7a1 disposed on the substrate 5, and an isolation region 7s1 defining the active regions 7a1.

[0030] The substrate 5 may be a semiconductor substrate. For example, the substrate 5 may include a group IV semiconductor, a group III-V compound semiconductor, or a group II-VI compound semiconductor. For example, the group IV semiconductor may include silicon, germanium, or silicon-germanium. For example, the substrate 5 may include a silicon material, for example, a single crystal silicon material. The substrate 5 may be a substrate including a silicon substrate, a silicon on insulator (SOI) substrate, a germanium substrate, a germanium on insulator (GOI) substrate, a silicon-germanium substrate, or an epitaxial layer.

[0031] The isolation region 7s1 may be a trench isolation layer. The isolation region 7s1 may be disposed on the substrate 5 and may define side surfaces of the active regions 7a1. The isolation region 7s1 may include an insulating material such as silicon oxide and/or silicon nitride. The active regions 7a1 may have a shape in which the active regions 7a1 protrude from the substrate 5 in a vertical direction Z.

[0032] The lower structure LS may further include gate trenches 12 intersecting the active regions 7a1 and extending to the isolation region 7s1, gate structures 15 disposed in the gate trenches 12, and first impurity regions 9a and second impurity regions 9b

disposed in the active regions 7a1 adjacent to side surfaces of the gate structures 15.

[0033] Each of the gate structures 15 may have a linear shape extending in a first direction D1. Each of the active regions 7a1 may have a bar shape extending in an oblique direction with respect to the first direction D1. One active region among the active regions 7a1 may intersect a pair of gate structures adjacent to each other among the gate structures 15.

[0034] In one active region 7a1 of the active regions 7a1, a pair of second impurity regions 9b, and one first impurity region 9a between the pair of second impurity regions 9b may be disposed. In one active region 7a1 of the active regions 7a1, the first and second impurity regions 9a and 9b may be spaced apart from each other by a pair of gate structures 15 (e.g., a pair of gate structures).

[0035] In example embodiments, the first impurity region 9a may be referred to as a first source/drain region, and the second impurity region 9b may be referred to as a second source/drain region.

[0036] Each of the gate structures 15 may include a gate dielectric layer 17a conformally covering an inner wall of the gate trench 12, a gate electrode 17b disposed on the gate dielectric layer 17a and filing a portion of the gate trench 12, and a gate capping layer 17c disposed on the gate electrode 17b and filling a remaining portion of the gate trench 12.

[0037] The gate dielectric layer 17a, the gate electrode 17b, the first impurity region 9a, and the second impurity region 9b may be included in a cell transistor.

[0038] The gate dielectric layer 17a may include at least one of silicon oxide and a high-κ dielectric. The high-κ dielectric may include a metal oxide or a metal oxynitride. The gate electrode 17b may be a word line of a memory semiconductor device such as DRAM or the like. The gate electrode 17b may include doped

polysilicon, a metal, a conductive metal nitride, a metal-semiconductor compound, a conductive metal oxide, conductive graphene, carbon nanotubes and/or a combination thereof. The gate capping layer 17c may include an insulating material, for example, silicon nitride.

[0039] The lower structure LS may further include a buffer insulating layer 20 disposed on the active regions 7a1, the isolation region 7s1, and the gate structures 15.

[0040] The lower structure LS may further include bit line structures 23 and contact structures 42. Each of the bit line structures 23 may include a bit line 25 and a bit line capping pattern 27 sequentially stacked. The bit line 25 may have a linear shape extending in a second direction D2, perpendicular to the first direction D1. The bit line 25 may be formed of a conductive material. The bit line 25 may include a first bit line layer 25a, a second bit line layer 25b, and a third bit line layer 25c sequentially stacked. For example, the first bit line layer 25a may include doped silicon, for example, polysilicon having an N-type conductivity, and the second and third bit line layers 25b and 25c may include different conductive materials among Al, Cu, Ti, Ta, Ru, W, Mo, Pt, Ni, Co, TiN, TaN, WN, NbN, TiAl, TiAlN, TiSi, TiSiN, TaSi, TaSiN, RuTiN, NiSi, CoSi, IrO_x, RuO_x, graphene, and/or carbon nanotubes.

[0041] The bit line capping pattern 27 may include a first bit line capping layer 27a, a second bit line capping layer 27b, and a third bit line capping layer 27c sequentially stacked. The bit line capping pattern 27 may be formed of an insulating material. Each of the first to third bit line capping layers 27a, 27b, and 27c may be formed of silicon nitride or a silicon nitride-based insulating material.

[0042] Each of the bit lines 25 may further include a bit line contact portion 25d extending downward from the first bit line layer 25a and electrically connected to the first impurity region 9a. The bit line 25 may be formed on the buffer insulating layer

20, and the bit line contact portion 25d of the bit line 25 may pass through the buffer insulating layer 20 and may be in contact with the first impurity region 9a.

[0043] Each of the contact structures 42 includes a lower contact plug 43 passing through the buffer insulating layer 20 and electrically connecting to the second impurity region 9b (e.g., the lower contact plug 43 may contact the second impurity region 9b), an upper contact plug 49 on the lower contact plug 43, and a metal-semiconductor compound layer 46 between the lower contact plug 43 and the upper contact plug 49. The lower contact plug 43 may include doped silicon, for example, polysilicon having an N-type conductivity. The upper contact plug 49 may include a plug portion 49P and a pad portion 49L disposed on the plug portion 49P and vertically overlapping a portion of the adjacent bit line capping pattern 27.

[0044] The lower structure LS may further include a bit line spacer 29 that is in contact with side surfaces of the bit line structure 23 and may be formed of an insulating material.

[0045] The lower structure LS may further include an insulating fence 40 in contact with the contact structures 42 between a pair of the bit line structures 23 adjacent and parallel to each other. For example, a plurality of contact structures 42 may be disposed between the pair of bit line structures 23 adjacent and parallel to each other, and the insulating fence 40 may be disposed between the contact structures 42. The insulating fence 40 may be formed of an insulating material such as silicon nitride.

[0046] The lower structure LS may further include an insulating pattern 63 passing through a space between the pad portions 49L of the contact structures 42, extending downwardly, and spaced apart from the bit lines 25. The insulating pattern 63 may be formed of an insulating material such as silicon nitride.

[0047] The lower structure LS may include an etch-stop layer 67 covering the contact

structures 42 and the insulating patterns 63. For example, the etch stop layer 67 may cover an entirety of each respective upper surface of the insulating patterns 63 and at least a portion of each respective upper surface of the contact structures 42. The etch-stop layer 67 may be formed of an insulating material. For example, the etch-stop layer 67 may include at least one of a SiBN material and a SiCN material.

[0048] The upper structure US may further include a capacitor CAP and at least one supporter layer 72 having an opening 72o.

[0049] The capacitor CAP may be a capacitor of a memory cell storing data in a DRAM device. The capacitor CAP may be referred to as a data storage structure.

[0050] The capacitor CAP may include first electrodes 80, a second electrode 90 on the first electrodes 80, and a dielectric layer 85 between the first electrodes 80 and the second electrode 90. The second electrode 90 may cover an upper surface and a side surface of each of the first electrodes 80.

[0051] Each of the first electrodes 80 may include a conductive material including at least three different elements. The dielectric layer 85 may include a high-κ dielectric, silicon oxide, silicon nitride, silicon oxynitride, or a combination thereof. The second electrode 90 may include a conductive material. The conductive material of the second electrode 90 may include a doped silicon-germanium, a metal, a conductive metal nitride, a metal-semiconductor compound, a conductive metal oxide, or a combination thereof, but example embodiments are not limited to the above-described materials. The second electrode 90 may include another conductive material.

[0052] The first electrodes 80 may be in contact with and electrically connected to the pad portions 49L, may pass through the etch-stop layer 67, and may extend upward.

[0053] Each of the first electrodes 80 may have a column shape or a pillar shape, but example embodiments are not limited thereto. For example, each of the first

electrodes 80 may have a cylindrical shape.

[0054] The at least one supporter layer 72 may include a lower supporter layer 72a and an upper supporter layer 72b disposed on different levels. The upper supporter layer 72b may be in contact with upper regions of the first electrodes 80, and may prevent the first electrodes 80 from collapsing. The lower supporter layer 72a may be in contact with the first electrodes 80 on a level lower than that of the upper supporter layer 72b, and may prevent deformation such as bending of the first electrodes 80. The at least one supporter layer 72 may include an insulating material such as silicon nitride.

[0055] In the capacitor CAP, the dielectric layer 85 may be disposed along the first electrodes 80 and surfaces of the at least one supporter layer 72 in contact with the first electrodes 80.

[0056] According to an example embodiment, the first electrode 80 may include a first element, a second element, and a third element. A degree of stiffness of a first nitride material including the first element may be higher than a degree of stiffness of a second nitride material including the second element. The first electrode 80 may include a region in which a concentration of the first element decreases and/or a concentration of the second element increases in a horizontal direction, away from side surfaces S1 and S2 of the first electrode 80. The first electrode 80 may include a region in which a ratio of a concentration of the first element in the region to a concentration of the second element in the region decreases in a horizontal direction, away from side surfaces S1 and S2 of the first electrode 80. For example, a concentration of the first element in the region may remain the same or may decrease in the horizontal direction, away from the side surfaces S1 and S2 of the first electrode 80, and a concentration of the second element in the region may increase in the horizontal direction, away from the side surfaces S1 and S2 of the first electrode 80. Here, the first nitride material including

the first element may be a material having stiffness capable of minimizing deformation of the first electrode 80, and the second nitride material including the second element may be a material capable of increasing capacitance of a capacitor CAP. For example, the first element may be Ti, the second element may be Nb, the third element may be N, the first nitride material including the first element may be TiN, and the second nitride material including the second element may be NbN. Accordingly, it is possible to provide the capacitor CAP including the first electrode 80 capable of increasing capacitance while minimizing deformation, thereby increasing a degree of integration of the semiconductor device 1.

[0057] Hereinafter, an example of a semiconductor device according to an example embodiment will be described with reference to FIGS. 3A and 3B, based on one first electrode 80 of the first electrodes 80. FIG. 3A is a partially enlarged view of a region indicated by "A" of FIG. 2, and FIG. 3B is a partially enlarged view of a region indicated by "B" of FIG. 3A.

[0058] Referring to FIGS. 3A and 3B together with FIGS. 1 and 2, the first electrode 80 may include a first material region 80a and a second material region 80b.

[0059] The second material region 80b may include a lower portion 80b_L and an upper portion 80b_U surrounding the first material region 80a and extending upward from an edge region of the lower portion 80b_L. In a top view, the upper portion 80b_U of the second material region 80b may have a ring shape surrounding the first material region 80a. In the second material region 80b, the lower portion 80b_L may be in contact with the pad portion 49L.

[0060] The first electrode 80 may include a region including at least three elements. For example, the first electrode 80 may include at least a first element, a second element, and a third element.

[0061] The stiffness of the first nitride material including the first element may be higher than that of the second nitride material including the second element. For example, the first element may be a titanium (Ti) element, the second element may be a niobium (Nb) element, and the third element may be a nitrogen (N) element. The first nitride material including the first element may be a TiN material, and the second nitride material including the second element may be a NbN material.

[0062] The first material region 80a may include at least three elements. In the first electrode 80, the first material region 80a may be defined as a region including the first element, the second element, and the third element, and the second material region 80b may be defined as a region including the first element and the third element, and not including the second element. The first element may be Ti, the second element may be Nb, and the third element may be N. The first material region 80a may be referred to as a first region, and the second material region 80b may be referred to as a second region.

[0063] The first material region 80a may be a region including a material capable of increasing the capacitance of the capacitor CAP, for example, a region including Nb. In order to prevent or minimize collapse or deformation of the first electrodes 80, the second material region 80b may be a region including a material having a stiffness higher than that of the first material region 80a, for example, a region including a TiN material.

[0064] In the first material region 80a of the first electrode 80, the second element, for example, a Nb element, may have a concentration increasing toward a vertical central axis Cz of the first electrode 80 from a portion close to a side surface of the first electrode 80. For example, in the first material region 80a of the first electrode 80, the second element, for example, a Nb element, may have a concentration that increases when moving in a horizontal direction X away from side surfaces S1 and S2 of the first

electrode 80 toward the vertical central axis Cz of the first electrode 80. Conversely, in the first material region 80a, the first element, for example, a Ti element, may have a concentration decreasing toward the vertical central axis Cz of the first electrode 80 from the portion close to the side surface of the first electrode 80. For example, in the first material region 80a of the first electrode 80, the first element, for example, a Ti element, may have a concentration that decreases when moving in a horizontal direction X away from side surfaces S1 and S2 of the first electrode 80 toward the vertical central axis Cz of the first electrode 80. However, example embodiments are not limited thereto. In the first material region 80a, the first element, for example, a Ti element, may have a concentration remaining the same toward the vertical central axis Cz of the first electrode 80 from the portion close to the side surface of the first electrode 80. For example, in the first material region 80a of the first electrode 80, the first element, for example, a Ti element, may have a concentration that remains substantially the same when moving in a horizontal direction X away from side surfaces S1 and S2 of the first electrode 80 toward the vertical central axis Cz of the first electrode 80.

[0065] In example embodiments, the side surface of the first electrode 80 may have a first side surface S1 and a second side surface S2 opposing each other in a horizontal direction, parallel to an upper surface of the lower structure LS. The first side surface S1 may be referred to as a first side S1, and the second side surface S2 may be referred to as a second side S2.

[0066] In example embodiments, a direction, parallel to the upper surface of the lower structure LS and toward the vertical central axis Cz of the first electrode 80 from the side surface of the first electrode 80 may be defined as a horizontal direction X. For example, the horizontal direction X may be a direction, toward the vertical central axis Cz of the first electrode 80 from the first side surface S1 of the first electrode 80, and a

direction, toward the vertical central axis Cz of the first electrode 80 from the second side surface S2 of the first electrode 80.

[0067] Hereinafter, various examples of a change in concentration of the second element in the first material region 80a will be described with reference to FIGS. 4A to 4D, respectively.

[0068] In an example, referring to FIG. 4A, in the first material region 80a, the second element, for example, a Nb element, may have a concentration increasing in a horizontal direction, away from the first side surface S1 and the second side surface S2. That is, in the first material region 80a of the first electrode 80, the concentration of the second element may increase in a direction, away from a side surface of the first electrode 80.

[0069] In the first material region 80a, the concentration of the second element may be highest in a central region between the first side surface S1 and the second side surface S2. In the first material region 80a, the concentration of the second element may gradually increase in a direction, away from the first side surface S1 and the second side surface S2.

[0070] In another example, referring to FIG. 4B, in the first material region 80a, the second element, for example, a Nb element, may have a concentration increasing in a stepwise manner in a direction, away from the first side surface S1 and the second side surface S2. In the first material region 80a, the concentration of the second element may be highest in a central region between the first side surface S1 and the second side surface S2.

[0071] In another example, referring to FIG. 4C, in the first material region 80a, the second element, for example, a Nb element, may have a concentration gradually increasing in a direction, away from the first side surface S1 and the second side surface S2, and may have a decreasing concentration in a central region between the first side

surface S1 and the second side surface S2.

[0072] In another example, referring to FIG. 4D, in the first material region 80a, the second element, for example, a Nb element, may have a concentration increasing in a stepwise manner in a direction, away from the first side surface S1 and the second side surface S2, and may have a decreasing concentration in a central region between the first side surface S1 and the second side surface S2.

[0073] Hereinafter, various modifications of components of the above-described example embodiment will be described. The various modifications of the components of the above-described example embodiment described below will mainly be described with respect to components to be modified or components to be replaced. In addition, the components that are modifiable or replaceable to be described below are described with reference to drawings below, but the components that are modifiable or replaceable are combined with each other, or are combined with the components described above to configure a semiconductor device according to example embodiments.

[0074] FIGS. 5A and 5B are diagrams illustrating various examples of the first material region 80a in FIGS. 3A and 3B, and may be partially enlarged views corresponding to the partially enlarged view of FIG. 3B.

[0075] In an example, referring to FIG. 5A, the first material region 80a of the first electrode 80 may include a first sub-region 80a_Sa and a second sub-region 80a_Sb that are sequentially disposed in the horizontal direction X, toward the vertical central axis Cz of the first electrode 80 from the side surfaces S1 and S2 of the first electrode 80. The first material region 80a may further include a third sub-region 80a_Sc. The third sub-region 80a_Sc may be disposed at a position farther than that of the second sub-region 80a_Sb and the first sub-region 80a_Sa from the side surfaces S1 and S2 of the first electrode 80. The third sub-region 80a_Sc may be disposed in a central region

of the first electrode 80. The second sub-region 80a_Sb may be disposed between the first sub-region 80a_Sa and the third sub-region 80a_Sc.

[0076] The first sub-region 80a_Sa may include first layers 78a1 and second layers 78b1 alternately stacked in the horizontal direction X. The second sub-region 80a_Sb may include third layers 78a2 and fourth layers 78b2 alternately stacked in the horizontal direction X. The third sub-region 80a_Sc may include fifth layers 78a3 and sixth layers 78b3 alternately stacked in the horizontal direction X.

[0077] The first layers 78a1 may be first NbN layers. The second layers 78b1 may be first TiN layers. The third layers 78a2 may be second NbN layers. The fourth layers 78b2 may be second TiN layers. The fifth layers 78a3 may be third NbN layers. The sixth layers 78b3 may be third TiN layers. Hereinafter, for easier understanding, example embodiments will be described by directly citing TiN and NbN. Accordingly, the first sub-region 80a_Sa may include the first NbN layers 78a1 and the first TiN layers 78b1 alternately stacked in the horizontal direction X. The second sub-region 80a_Sb may include the second NbN layers 78a2 and the second TiN layers 78b2 alternately stacked in the horizontal direction X. The third sub-region 80a_Sc may include the third NbN layers 78a3 and the third TiN layers 78b3 alternately stacked in the horizontal direction X.

[0078] The first NbN layers 78a1 may have the same thickness. The first TiN layers 78b1 may have the same thickness. The second NbN layers 78a2 may have the same thickness. The second TiN layers 78b2 may have the same thickness. The third NbN layers 78a3 may have the same thickness. The third TiN layers 78b3 may have the same thickness.

[0079] A thickness of each of the first TiN layers 78b1 may be greater than a thickness of each of the first NbN layers 78a1. A thickness of each of the third TiN layers 78b3

may be smaller than a thickness of each of the third NbN layers 78a3.

[0080] A thickness of each of the second NbN layers 78a2 may be greater than the thickness of each of the first NbN layers 78a1. The thickness of each of the third NbN layers 78a3 may be greater than the thickness of each of the second NbN layers 78a2.

[0081] In an example embodiment, the first to third TiN layers 78b1, 78b2, and 78b3 may have the same thickness (e.g., the same horizontal thickness). Accordingly, a concentration of a Ti element in the second sub-region 80a_Sb may be the same as a concentration of a Ti element in the first sub-region 80a_Sa, and a concentration of a Ti element in the third sub-region 80a_Sc may be the same as the concentration of the Ti element in the second sub-region 80a_Sb. However, example embodiments are not limited thereto. For example, a concentration of the Ti element may decrease in a horizontal direction, away from side surfaces S1 and S2 of the first electrode 80. The first NbN layers 78a1 may have a first thickness. The second NbN layers 78a2 may have a second thickness greater than the first thickness. The third NbN layers 78a3 may have a third thickness greater than the second thickness. Accordingly, a content ratio of a Nb element in the second sub-region 80a_Sb may be higher than a content ratio of a Nb element in the first sub-region 80a_Sa, and a content ratio of a Nb element in the third sub-region 80a_Sc may be higher than the content ratio of the Nb element in the second sub-region 80a_Sb. A concentration of the Nb element in the second sub-region 80a_Sb may be higher than a concentration of the Nb element in the first sub-region 80a_Sa, and a concentration of the Nb element in the third sub-region 80a_Sc may be higher than the concentration of the Nb element in the second sub-region 80a_Sb. Accordingly, a content ratio of the Ti element to the Nb element may decrease in a horizontal direction, away from side surfaces S1 and S2 of the first electrode 80.

[0082] In another example, referring to FIG. 5B, the first material region 80a of the first electrode 80 may include a first sub-region 80a_Sa, a second sub-region 80a_Sb, a third sub-region 80a_Sc, a fourth sub-region 80a_Sd, and a fifth sub-region 80a_Se that are sequentially stacked in a direction (e.g., the horizontal direction X), toward the vertical central axis Cz of the first electrode 80 from the side surfaces S1 and S2 of the first electrode 80. The fifth sub-region 80a_Se may be disposed in a central region of the first electrode 80.

[0083] The first to third sub-regions 80a_Sa, 80a_Sb, and 80a_Sc may be substantially the same as the first to third sub-regions 80a_Sa, 80a_Sb, and 80a_Sc described with reference to FIG. 5A.

[0084] The fourth sub-region 80a_Sd may include fourth TiN layers 78b4 and fourth NbN layers 78a4 alternately stacked in the horizontal direction X. The fifth sub-region 80a_Se may include fifth TiN layers 78b5 and fifth NbN layers 78a5 alternately stacked in the horizontal direction X. The fourth TiN layers 78b4 may have the same thickness. The fourth NbN layers 78a4 may have the same thickness. The fifth TiN layers 78b5 may have the same thickness. The fifth NbN layers 78a5 may have the same thickness.

[0085] A thickness of each of the fourth NbN layers 78a4 may be smaller than a thickness of each of the third NbN layers 78a3. A thickness of each of the fifth NbN layers 78a5 may be smaller than a thickness of each of the fourth NbN layers 78a4. Accordingly, a content ratio of a Nb element in the second sub-region 80a_Sb may be higher than a content ratio of a Nb element in the first sub-region 80a_Sa. A content ratio of a Nb element in the third sub-region 80a_Sc may be higher than the content ratio of the Nb element in the second sub-region 80a_Sb. A content ratio of a Nb element in the fourth sub-region 80a_Sd may be lower than the content ratio of the Nb

element in the third sub-region 80a_Sc. A content ratio of a Nb element in the fifth sub region 80a_Se may be lower than the content ratio of the Nb element in the fourth sub-region 80a_Sd. A concentration of the Nb element in the second sub-region 80a_Sb may be higher than a concentration of the Nb element in the first sub-region 80a_Sa. A concentration of the Nb element in the third sub-region 80a_Sc may be higher than a concentration of the Nb element in the second sub-region 80a_Sb. A concentration of the Nb element in the fourth sub-region 80a_Sd may be lower than the concentration of the Nb element in the third sub-region 80a_Sc. A concentration of the Nb element in the fifth sub-region 80a_Se may be lower than the concentration of the Nb element in the fourth sub-region 80a_Sd.

[0086] In the example embodiments described above with reference to FIGS. 3A to 5B, a width of the first material region 80a may be same as a width of the second material region 80b positioned on either side of the first material region 80a. However, embodiments are not limited thereto. For example, the width of the first material region 80a may be different from the width of the second material region 80b positioned on either side of the first material region 80a. Examples in which the width of the first material region 80a is different from the width of the second material region 80b will be described with reference to FIGS. 6A and 6B. FIGS. 6A and 6B are conceptual diagrams illustrating the widths of the first material region 80a and the second material region 80b in the example embodiments described above with reference to FIGS. 3A to 5B, and may be partially enlarged views corresponding to the partially enlarged view of FIG. 3B.

[0087] In an example, referring to FIG. 6A, the width of the first material region 80a may be greater than the width of the second material region 80b positioned on either side of the first material region 80a. For example, the width of the first material region

80a may be greater than the width of the second material region 80b positioned on each respective side of the first material region 80a.

[0088] In another example, referring to FIG. 6B, the width of the first material region 80a may be smaller than the width of the second material region 80b positioned on either side of the first material region 80a. For example, the width of the first material region 80a may be smaller than the width of the second material region 80b positioned on each respective side of the first material region 80a.

[0089] In the example embodiments described above with reference to FIGS. 1 to 6B, the first electrode 80 may include the first material region 80a and the second material region 80b. However, example embodiments are not limited thereto. For example, in the first electrode 80, the second material region 80b may be omitted. Various examples in which the second material region 80b is omitted in the first electrode 80 as described above and the first electrode 80 includes the first material region 80a will be described with reference to FIGS. 7A and 7B, respectively.

[0090] Referring to FIG. 7A, the first electrode 80 may include the first material region 80a as described with reference to FIG. 5A or the first material region 80a as described with reference to FIG. 5B. For example, the first material region 80a may include the first sub-region 80a_Sa, the second sub-region 80a_Sb, and the third sub-region 80a_Sc sequentially disposed in the horizontal direction X as described with reference to FIG. 5A. Referring to FIG. 5A, the first sub-region 80a_Sa may include the first NbN layers 78a1 and the first TiN layers 78b1 alternately stacked in the horizontal direction X.

[0091] Among the first NbN layers 78a1 and the first TiN layers 78b1 in the first sub-region 80a_Sa, one of the first NbN layers 78a1 may be in contact with the dielectric layer 85. However, example embodiments are not limited thereto. For

example, as illustrated in FIG. 7B, among the first NbN layers 78a1 and the first TiN layers 78b1 in the first sub-region 80a_Sa, one of the first TiN layers 78b1 may be in contact with the dielectric layer 85.

[0092] A modification of the first electrode 80 including the first material region 80a and the second material region 80b described in the example embodiments with reference to FIGS. 1 to 6B will be described with reference to FIGS. 8A and 8B. FIG. 8A is a partially enlarged view illustrating a modification of a region indicated by "A" of FIG. 2, and FIG. 8B is a partially enlarged view of a region indicated by "Ba" of FIG. 8A.

[0093] Referring to FIGS. 8A and 8B, the first electrode 80 described with reference to FIGS. 3A and 3B may be modified into a first electrode 180 including a first material region 180a and a second material region 180b as described with reference to FIGS. 8A and 8B.

[0094] In the first electrode 180, the first material region 180a may include a lower portion 180a_L below the second material region 180b, and an upper portion 180a_U extending upward from an edge region of the lower portion 180a_L and covering a side surface of the second material region 180b. The first electrode 180 may include a first element, a second element, and a third element. The first element may be a titanium (Ti) element, the second element may be a niobium (Nb) element, and the third element may be a nitrogen (N) element.

[0095] The second material region 180b may be formed of a material the same as that of the second material region described above (80b in FIGS. 3A and 3B). For example, the second material region 180b may include a material including the first element and the third element, for example, TiN.

[0096] The first material region 180a may include the first element, the second element,

and the third element. The first material region 180a may include a material having a concentration of the second element that varies according to a distance from a side surface of the first electrode 180. For example, in the first material region 180a, the concentration of the second element may increase as the distance from the side surface of the first electrode 180 increases.

[0097] The first material region 180a of the first electrode 180 may include a first sub-region 180a_Sa, a second sub-region 180a_Sb, and a third sub-region 180a_Sc that are sequentially disposed in a horizontal direction (e.g., the horizontal direction X) toward a vertical central axis Cz of the first electrode 180 from side surfaces S1 and S2 of the first electrode 180.

[0098] The first sub-region 180a_Sa may include first NbN layers 178a1 and first TiN layers 178b1 alternately stacked in the horizontal direction X. The second sub-region 180a_Sb may include second NbN layers 178a2 and second TiN layers 178b2 alternately stacked in the horizontal direction X. The third sub-region 180a_Sc may include third NbN layers 178a3 and third TiN layers 178b3 alternately stacked in the horizontal direction X.

[0099] The first NbN layers 178a1 may have the same thickness. The first TiN layers 178b1 may have the same thickness. The second NbN layers 178a2 may have the same thickness. The second TiN layers 178b2 may have the same thickness. The third NbN layers 178a3 may have the same thickness. The third TiN layers 178b3 may have the same thickness.

[00100] A thickness of each of the first TiN layers 178b1 may be greater than a thickness of each of the first NbN layers 178a1. A thickness of each of the third TiN layers 178b3 may be smaller than a thickness of each of the third NbN layers 178a3. A thickness of each of the second NbN layers 178a2 may be greater than a thickness of

each of the first NbN layers 178a1, and a thickness of each of the third NbN layers 178a3 may be greater than a thickness of each of the second NbN layers 178a2.

[00101] In an example, among the first NbN layers 178a1 and the first TiN layers 178b1, one of the first TiN layers 178b1 may be in contact with the dielectric layer 85.

[00102] In another example, among the first NbN layers 178a1 and the first TiN layers 178b1, one of the first NbN layers 178a1 may be in contact with the dielectric layer 85.

[00103] A modification of the first electrode 80 including the first material region 80a and the second material region 80b described in the example embodiments with reference to FIGS. 1 to 6B will be described with reference to FIG. 9. FIG. 9 is a partially enlarged view illustrating a modification of a region indicated by "A" of FIG. 2.

[00104] Referring to FIG. 9, the first electrode 80 described with reference to FIGS. 3A and 3B may be modified into a first electrode 280 including a first material region 280a, a second material region 280b, and a third material region 280c.

[00105] In the first electrode 280, the first material region 280a may include a lower portion 280a_L below the third material region 280c, and an upper portion 280a_U extending upward from an edge region of the lower portion 280a_L and covering a side surface of the third material region 280c. The second material region 280b may include a lower portion 280b_L below the first material region 280a, and an upper portion 280b_U extending upward from an edge region of the lower portion 280b_L and covering an outer surface of the first material region 280a.

[00106] The first electrode 280 may include at least three elements. For example, the first electrode 280 may include a first element, a second element, and a third element. The first element may be a titanium (Ti) element, the second element may be a niobium

(Nb) element, and the third element may be a nitrogen (N) element.

[00107] The second material region 280b may be formed of a material the same as that of the second material region 80b described above (80b in FIGS. 3A and 3B). For example, the second material region 280b may include a material including the first element and the third element, for example, TiN.

[00108] The third material region 280c may be formed of a material the same as that of the second material region 80b described above (80b in FIGS. 3A and 3B). For example, the third material region 280c may include a material including the first element and the third element, for example, TiN. The second material region 280b and the third material region 280c may include the same material.

[00109] The first material region 280a may be substantially the same as one of the first material regions 80a described with reference to FIGS. 1 to 6B. For example, the first material region 280a may include at least three elements. For example, the first material region 280a may include the first element, the second element, and the third element, and a concentration of the second element in the first material region 280a may increase as a distance from a side surface of the first electrode 280 increases.

[00110] Next, a modification of the lower structure LS described with reference to FIGS. 1 and 2 will be described with reference to FIGS. 10 and 11. In FIGS. 10 and 11, FIG. 10 is a schematic plan view illustrating a semiconductor device 300 in a modification, and FIG. 11 is a cross-sectional view illustrating a region taken along lines IV-IV' and V-V' of FIG. 10.

[00111] Referring to FIGS. 10 and 11, a semiconductor device 300 according to an example embodiment may include a lower structure LS' obtained by modifying the lower structure LS described with reference to FIGS. 1 and 2.

[00112] The lower structure LS' may include a substrate 305, a plurality of first

conductive lines 320 disposed on the substrate 305, channel regions 330c, lower source/drain regions 330s, upper source/drain regions 330d, cell gate electrodes 340, and cell gate dielectrics 350. The substrate 305 may be a semiconductor substrate.

[00113] The channel regions 330c, the lower source/drain regions 330s, the upper source/drain regions 330d, and the cell gate electrodes 340 may be included in vertical channel transistors. Here, the vertical channel transistors may be referred to as cell transistors. The vertical channel transistor may refer to a structure in which a channel length of each of the channel regions 330c extends from the substrate 305 in a vertical direction.

[00114] The lower structure LS' may further include a lower insulating layer 312 disposed on the substrate 305. On the lower insulating layer 312, the plurality of first conductive lines 320 may be spaced apart from each other in a second horizontal direction, and may extend in a first horizontal direction.

[00115] The lower structure LS' may further include a plurality of first lower insulating patterns 322 filling a space between the plurality of first conductive lines 320 on the lower insulating layer 312. The plurality of first lower insulating patterns 322 may extend in a first horizontal direction. Upper surfaces of the plurality of first lower insulating patterns 322 may be disposed on a level the same as those of upper surfaces of the plurality of first conductive lines 320. The plurality of first conductive lines 320 may function as bit lines of the semiconductor device 300.

[00116] In an example, the plurality of first conductive lines 320 may include doped polysilicon, a metal, a conductive metal nitride, a conductive metal silicide, a conductive metal oxide, or a combination thereof. For example, the plurality of first conductive lines 320 may include doped polysilicon, Al, Cu, Ti, Ta, Ru, W, Mo, Pt, Ni, Co, TiN, TaN, WN, NbN, TiAl, TiAlN, TiSi, TiSiN, TaSi, TaSiN, RuTiN, NiSi, CoSi,

IrO_x, RuO_x, or a combination thereof, but are not limited thereto. The plurality of first conductive lines 320 may include a single layer or multiple layers including the above-described materials. In an example, the plurality of first conductive lines 320 may include a two-dimensional semiconductor material. For example, the two-dimensional semiconductor material may include graphene, carbon nanotubes, or a combination thereof.

[00117] The channel regions 330c may be arranged in a matrix form in which the channel regions 330c are spaced apart from each other in a second horizontal direction and a first horizontal direction on the plurality of first conductive lines 320.

[00118] The lower source/drain regions 330s, the channel regions 330c, and the upper source/drain regions 330d may be sequentially stacked (e.g., in a vertical direction).

[00119] In an example, one channel region 330c and the lower and upper source/drain regions 330s and 330d disposed below/on the one channel region 330c may have a first width in a horizontal direction and a first height in a vertical direction, and the first height may be greater than the first width. For example, the first height may be about 2 to 10 times the first width, but is not limited thereto.

[00120] In an example, the channel regions 330c may include an oxide semiconductor. For example, the oxide semiconductor may include $In_xGa_yZn_zO$, $In_xGa_ySi_zO$, $In_xSn_yZn_zO$, In_xZn_yO, Zn_xO, Zn_xSn_yO, Zn_xO_yN, $Zr_xZn_ySn_zO$, Sn_xO, $Hf_xIn_yZn_zO$, $Ga_xZn_ySn_zO$, $Al_xZn_ySn_zO$, $Yb_xGa_yZn_zO$, In_xGa_yO, or a combination thereof. The channel regions 330c may include a single layer or multiple layers of the oxide semiconductor. In some examples, the channel regions 330c may have a bandgap energy greater than that of silicon. For example, the channel regions 330c may have a bandgap energy of about 1.5 eV to about 5.6 eV. For example, the channel

regions 330c may have optimal channel performance when the channel regions 330c have a bandgap energy of about 2.0 eV to 4.0 eV. For example, the channel regions 330c may be polycrystalline or amorphous, but are not limited thereto.

[00121] In an example, the channel regions 330c may include a two-dimensional semiconductor material. For example, the two-dimensional semiconductor material may include graphene, carbon nanotubes, or a combination thereof.

[00122] In an example, the channel regions 330c may include a semiconductor material such as silicon.

[00123] Hereinafter, one channel region 330c and one cell gate electrode 340 will mainly be described, but the channel region 330c and the cell gate electrode 340 may be understood as being provided in plurality.

[00124] The cell gate electrode 340 may extend in a second horizontal direction X on opposite sidewalls of the channel region 330c. The cell gate electrode 340 may include a first sub-gate electrode 340P1 opposing a first sidewall of the channel region 330c, and a second sub-gate electrode 340P2 opposing a second sidewall opposite to the first sidewall of the channel region 330c. As one channel region 330c is disposed between the first sub-gate electrode 340P1 and the second sub-gate electrode 340P2, the semiconductor device 300 may have a dual-gate transistor structure. However, example embodiments are not limited thereto. The second sub-gate electrode 340P2 may be omitted, and only the first sub-gate electrode 340P1 opposing the first sidewall of the channel region 330c may be formed to implement a single-gate transistor structure.

[00125] The cell gate electrode 340 may include doped polysilicon, a metal, a conductive metal nitride, a conductive metal silicide, a conductive metal oxide, or a combination thereof. For example, the cell gate electrode 340 may be formed of doped

polysilicon, Al, Cu, Ti, Ta, Ru, W, Mo, Pt, Ni, Co, TiN, TaN, WN, NbN, TiAl, TiAlN, TiSi, TiSiN, TaSi, TaSiN, RuTiN, NiSi, CoSi, IrO_x, RuO_x, or a combination thereof, but is not limited thereto.

[00126] The cell gate dielectric 350 may surround a sidewall of the channel region 330c, and may be interposed between the channel region 330c and the cell gate electrode 340. For example, the entire sidewall of the channel region 330c may be surrounded by the cell gate dielectric 350, and a portion of the sidewall of the cell gate electrode 340 may be in contact with the cell gate dielectric 350. In other example embodiments, the cell gate dielectric 350 may extend in an extension direction of the cell gate electrode 340, that is, a second horizontal direction X, and only two sidewalls opposing the cell gate electrode 340 among sidewalls of the channel region 330c may be in contact with the cell gate dielectric 350.

[00127] In an example, the cell gate dielectric 350 may be formed of a silicon oxide film, a silicon oxynitride film, a high-k film having a dielectric constant higher than that of a silicon oxide film, or a combination thereof. The high-k film may be formed of a metal oxide or a metal oxynitride. For example, the high-k film usable as the cell gate dielectric 350 may be formed of HfO_2, HfSiO, HfSiON, HfTaO, HfTiO, HfZrO, ZrO_2, Al_2O_3, or a combination thereof, but is not limited thereto.

[00128] The lower structure LS' may further include a plurality of second lower insulating patterns 332 disposed on the plurality of first lower insulating patterns 322. The second lower insulating patterns 332 may extend in a first horizontal direction, and the channel region 330c may be disposed between two adjacent second lower insulating patterns 332 among the plurality of second lower insulating patterns 332.

[00129] The lower structure LS' may further include a first buried layer 334 and a second buried layer 336 disposed in a space between two adjacent channel regions 330c

between the two adjacent second lower insulating patterns 332. The first buried layer 334 may be disposed on a bottom portion of the space between two adjacent channel regions 330c, and the second buried layer 336 may be formed to fill a remaining portion of the space between the two adjacent channel regions 330c on the first buried layer 334. An upper surface of the second buried layer 336 may be disposed on a level the same as that of an upper surface of the upper source/drain region 330d, and the second buried layer 336 may cover an upper surface of the cell gate electrode 340. Alternatively, the plurality of second lower insulating patterns 332 may be formed of a material layer continuous with the plurality of first lower insulating patterns 322, or the second buried layer 336 may be formed of a material layer continuous with the first buried layer 334.

[00130] The lower structure LS' may further include contact structures 360c electrically connected to the upper source/drain regions 330d on the channel regions 330c, and insulating isolation patterns 363c between the contact structures 360c. Each of the contact structures 360c may include a barrier layer 359a and a metal layer 359b on the barrier layer 359a. The lower structure LS' may further include an etch-stop layer 367c covering the contact structures 360c and the insulating isolation patterns 363c. For example, the etch-stop layer 367c may cover an entirety of each respective upper surface of the insulating isolation patterns 363c and at least a portion of each respective upper surface of the contact structures 360c.

[00131] The semiconductor device 300 according to an example embodiment may further include an upper structure US' on the lower structure LS'.

[00132] The upper structure US' may further include a capacitor CAP and at least one supporter layer 372. The capacitor CAP may be a capacitor of a memory cell storing data in a DRAM device. The capacitor CAP may be referred to as a data storage structure. The capacitor CAP may include first electrodes 380, a second electrode 390

on the first electrodes 380, and a dielectric layer 385 between the first electrodes 380 and the second electrode 390. The dielectric layer 385 and the second electrode 390 may be substantially the same as the dielectric layer (85 in FIGS. 2, 3A and 3B) and the second electrode (90 in FIGS. 2, 3A and 3B) described above. The first electrodes 380 may be in contact with and electrically connected to the contact structures 360c, may pass through the etch-stop layer 367c, and may extend upward. Each of the first electrodes 380 may have a pillar shape, but example embodiments are not limited thereto. For example, each of the first electrodes 380 may have a cylindrical shape.

[00133] The first electrodes 380 may be the same as one of the various first electrodes 80, 180, and 280 described with reference to FIGS. 1 to 9.

[00134] The at least one supporter layer 372 may include a lower supporter layer 372a and an upper supporter layer 372b disposed on different levels. The lower supporter layer 372a and the upper supporter layer 372b may be in contact with upper regions of the first electrodes 380, and may prevent the first electrodes 380 from collapsing. The lower supporter layer 372a may be in contact with the first electrodes 380 on a level lower than that of the upper supporter layer 372b, and may prevent deformation such as bending of the first electrodes 380. The at least one supporter layer 372 may include an insulating material such as silicon nitride. In the capacitor CAP, the dielectric layer 385 may be disposed along the first electrodes 380 and surfaces of the at least one supporter layer 372 in contact with the first electrodes 380.

[00135] In the top view illustrated in FIG. 1, the opening 72o of the at least one supporter layer 72 may have a shape in which the opening 72o exposes a portion of a side surface of each of the first electrodes 80 (e.g., four first electrodes), but example embodiments are not limited thereto. FIG. 12 is a schematic top view illustrating a modification of a semiconductor device according to an example embodiment.

[00136] In a modification, referring to FIG. 12, the opening 72o of the at least one supporter layer 72 illustrated in FIG. 1 may be modified into an opening 72o' of at least one supporter layer 72' exposing a portion of a side surface of each of the first electrodes 80 (e.g., three first electrodes), as illustrated in FIG. 12.

[00137] Next, an example of a method of forming a semiconductor device according to an example embodiment will be described with reference to FIGS. 13 to 15.

[00138] Referring to FIG. 13, a lower structure LS may be formed. The lower structure LS may be the lower structure LS described with reference to FIGS. 1 and 2, or the lower structure LS' described with reference to FIGS. 10 and 11. For example, the transistors TR, the bit lines 25, and the contact structures 42 may be included, as described with reference to FIGS. 1 and 2.

[00139] A lower mold layer 68a, a lower supporter layer 72a, an upper mold layer 68b, and an upper supporter layer 72b sequentially stacked on the lower structure LS may be included. The lower mold layer 68a and the upper mold layer 68b may be formed of the same material, for example, silicon oxide.

[00140] An etching process may be performed to form openings 73 exposing the pad portions 49L of the contact structures 42 while passing through the upper supporter layer 72b, the upper mold layer 68b, the lower supporter layer 72a, the lower mold layer 68a, and the etch-stop layer 67.

[00141] Referring to FIG. 14, first electrodes 80 may be formed in the openings 73. The first electrodes 80 may be formed as one of the first electrodes 80, 180, 280, and 380 described with reference to FIGS. 1 to 11. For example, forming the first electrodes 80 may include forming a material layer of the second material region 80b conformally covering the openings 73 described with reference to FIGS. 3A and 3B, forming a material layer of the first material region 80a described with reference to

FIGS. 3A and 3B on the material layer of the second material region 80b, and planarizing the material layer of the first material region 80a and the material layer of the second material region 80b by performing an etch-back and/or chemical mechanical planarization process.

[00142] Referring to FIG. 15, openings passing through the upper supporter layer 72b, the upper mold layer 68b, and the lower supporter layer 72a may be formed, and the upper mold layer 68b exposed by the openings and the lower mold layer 68a may be removed to form an opening 82. Accordingly, the first electrodes 80 supported by the supporter structures 72a and 72b may be formed on the lower structure LS.

[00143] Referring back to FIGS. 1 and 2, a dielectric layer 85, conformally formed along the surfaces of the first electrodes 80 and the supporter structures 72a and 72b on the lower structure LS, may be formed. Subsequently, a second electrode 90 filling the opening 82 may be formed on the dielectric layer 85.

[00144] According to example embodiments, a semiconductor device may include a first electrode, a second electrode, and a dielectric layer between the first electrode and the second electrode. The first electrode, the dielectric layer, and the second electrode may be included in a capacitor capable of storing data in the semiconductor device, such as a DRAM. The first electrode may include a first element, a second element, and nitrogen (N). A degree of stiffness of a first nitride material including the first element may be higher than a degree of stiffness of a second nitride material including the second element. The first electrode may include a region in which a concentration of the first element decreases or remains the same and a concentration of the second element increases in a horizontal direction, away from a side surface of the first electrode. Here, the first nitride material including the first element may be a material having stiffness capable of minimizing deformation of the first electrode, and the

second nitride material including the second element may be a material capable of increasing capacitance of the capacitor. Accordingly, it is possible to provide the capacitor including the first electrode capable of increasing capacitance while minimizing deformation, thereby increasing a degree of integration of the semiconductor device.

[00145] The various and beneficial advantages and effects of example embodiments are not limited to the above description, and will be more easily understood in the course of describing specific example embodiments.

[00146] While example embodiments have been shown and described above, it will be apparent to those skilled in the art that modifications and variations could be made without departing from the scope of example embodiments as defined by the appended claims.

What is claimed is:

1. A semiconductor device comprising:

a lower structure;

first electrodes spaced apart from each other on the lower structure;

a second electrode on the first electrodes; and

a dielectric layer between the first electrodes and the second electrode,

wherein each of the first electrodes include a first element, a second element, and nitrogen (N),

a degree of stiffness of a first nitride material including the first element is higher than a degree of stiffness of a second nitride material including the second element,

each of the first electrodes includes a region in which a ratio of a concentration of the first element in the region to a concentration of the second element in the region decreases in a horizontal direction, away from a side surface of each of the first electrodes, and

the horizontal direction is parallel to an upper surface of the lower structure.

2. The semiconductor device of claim 1, wherein the concentration of the second element in the region increases in the horizontal direction, away from the side surface of each of the first electrodes.

3. The semiconductor device of claim 1 or claim 2, wherein

the first element is Ti,

the second element is Nb,

the first nitride material including the first element is TiN, and

the second nitride material including the second element is NbN.

4. The semiconductor device of any one of claims 1 to 3, wherein each of the first electrodes includes:

the region, which comprises a first region including the first element, the second element, and the nitrogen (N); and

a second region not including the second element, and including the first nitride material including the first element.

5. The semiconductor device of any one of claims 1 to 4, further comprising:

at least one supporter layer having an opening,

wherein the at least one supporter layer and the first electrodes are in contact with each other,

the second electrode is on the at least one supporter layer and the first electrodes, and

the dielectric layer is between the second electrode and the at least one supporter layer and between the second electrode and the first electrodes.

6. A semiconductor device comprising:

a lower structure;

a first electrode on the lower structure;

a second electrode on the first electrode; and

a dielectric layer between the first electrode and the second electrode,

wherein the first electrode includes a first region including at least a titanium

(Ti) element, a niobium (Nb) element, and a nitrogen (N) element, and

in the first region of the first electrode, a concentration of the Nb element increases in a horizontal direction, away from a side surface of the first electrode.

7. The semiconductor device of claim 6,

wherein the first electrode further includes a second region between the first region and the side surface of the first electrode,

wherein the second region does not include the Nb element, and includes the Ti element and the N element,

wherein the second region includes a lower portion and an upper portion on a sidewall of the first region and extending upward from an edge region of the lower portion, and

wherein the dielectric layer includes a portion in contact with an upper surface of the first region and an upper surface of the second region.

8. The semiconductor device of claim 6 or claim 7,

wherein the first region includes:

a first sub-region in which first TiN layers and first NbN layers are alternately stacked in the horizontal direction; and

a second sub-region in which second TiN layers and second NbN layers are alternately stacked in the horizontal direction,

wherein each of the first TiN layers has a first horizontal thickness,

wherein each of the first NbN layers has a second horizontal thickness smaller than the first horizontal thickness,

wherein each of the second NbN layers has a third horizontal thickness greater than the second horizontal thickness, and

wherein the first TiN layers and the second TiN layers have substantially equal horizontal thicknesses.

9. A semiconductor device comprising:

a lower structure;

a first electrode on the lower structure;

a second electrode on the first electrode; and

a dielectric layer between the first electrode and the second electrode,

wherein the first electrode includes a first region including at least three elements,

the first region of the first electrode includes a first sub-region and a second sub-region, wherein the first sub-region is between, in a horizontal direction, the second sub-region and a side surface of the first electrode,

the first sub-region includes first layers and second layers alternately stacked in the horizontal direction,

the second sub-region includes third layers and fourth layers alternately stacked in the horizontal direction,

the first layers and the third layers include a same first material,

the second layers and the fourth layers include a same second material, and

a horizontal thickness of each of the second layers is smaller than a horizontal thickness of each of the fourth layers.

10. The semiconductor device of claim 9, wherein

the first region of the first electrode further includes a third sub-region,

the second sub-region is between the first sub-region and the third sub-region; and

the third sub-region includes fifth layers and sixth layers alternately stacked in the horizontal direction,

the fifth layers include the first material,

the sixth layers include the second material, and

a horizontal thickness of each of the sixth layers is greater than a horizontal thickness of each of the fourth layers.