

100

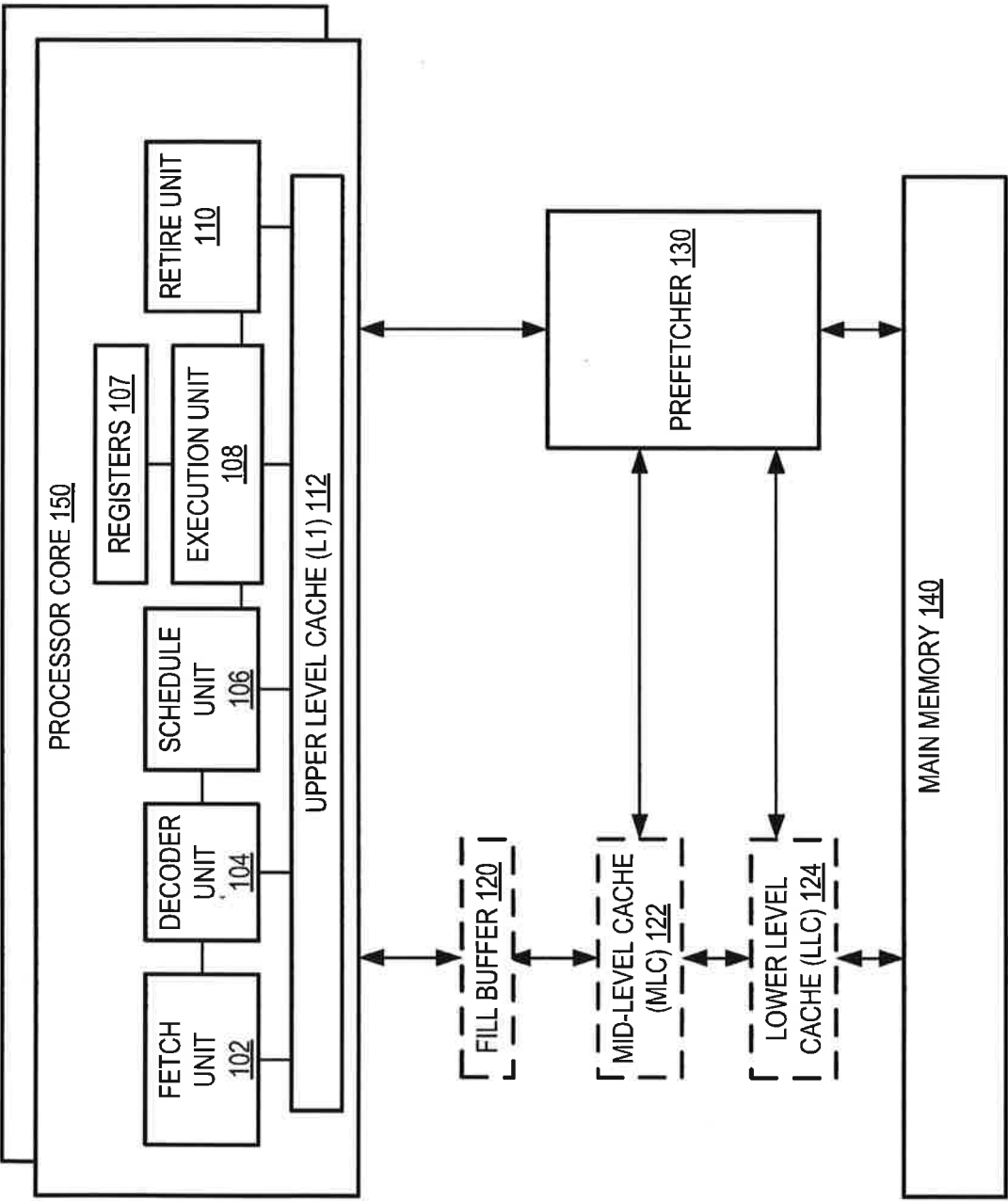


FIG. 1

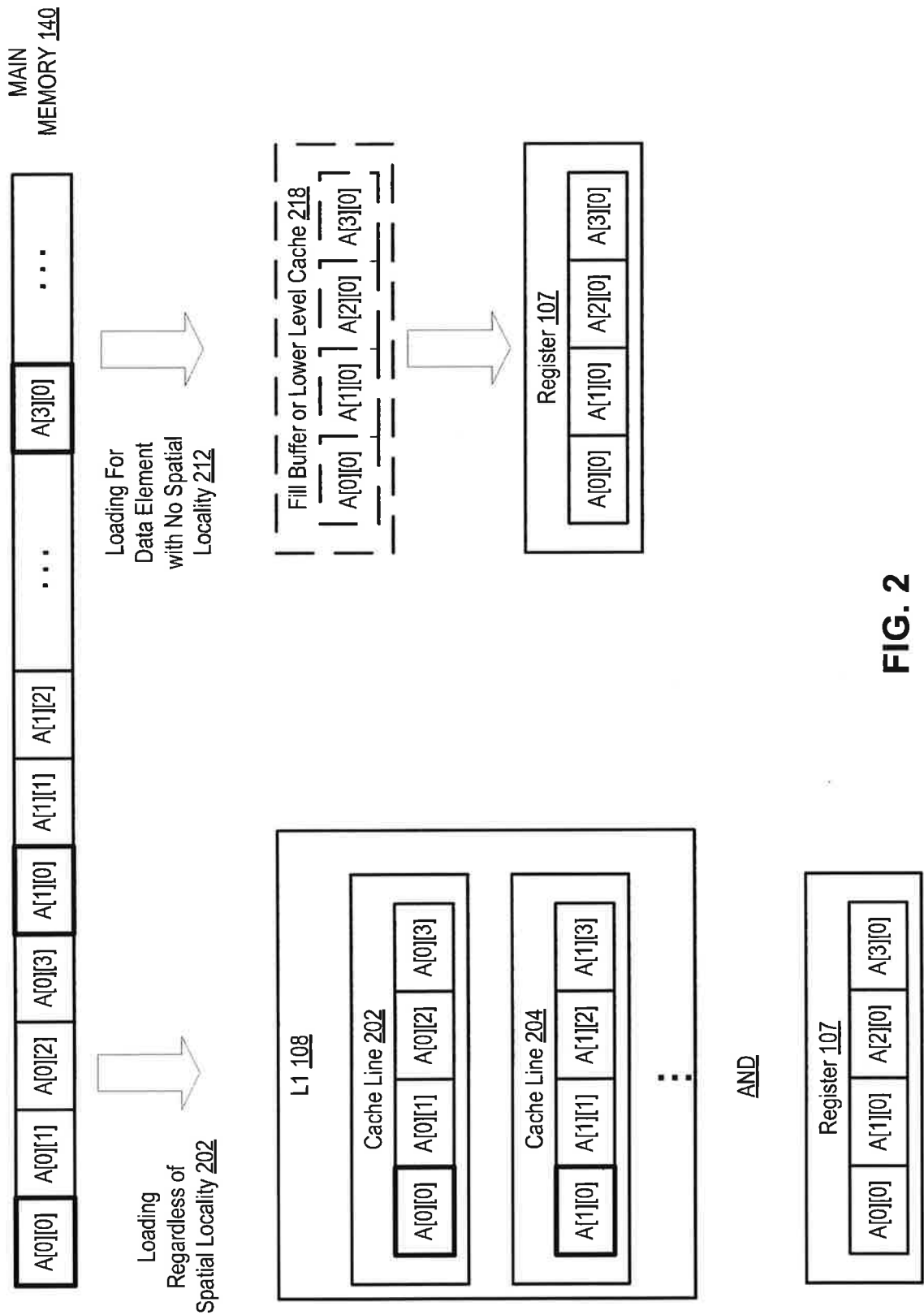


FIG. 2

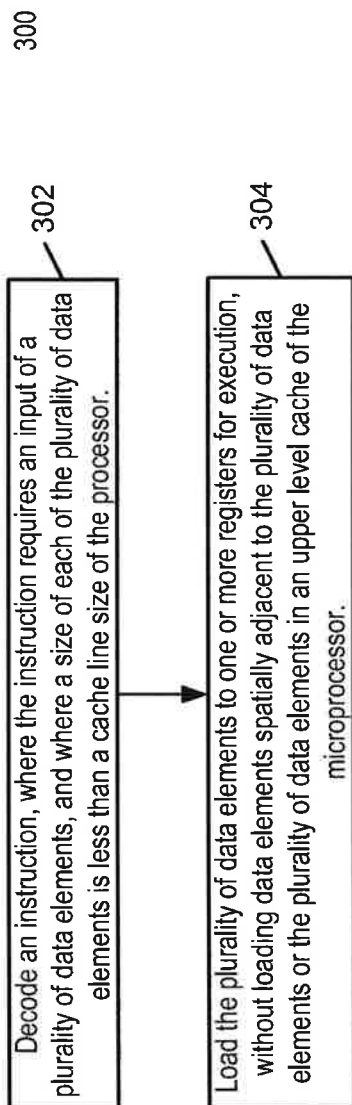


FIG. 3A

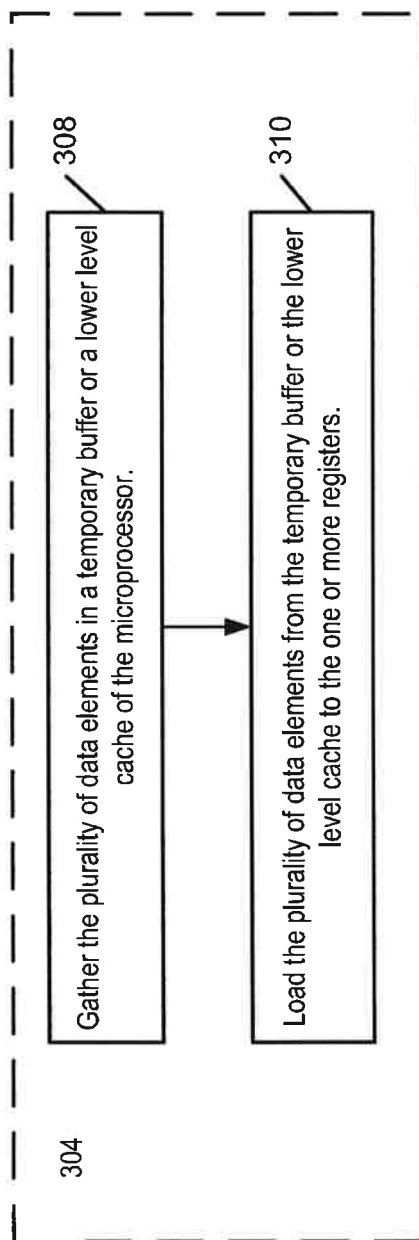


FIG. 3B

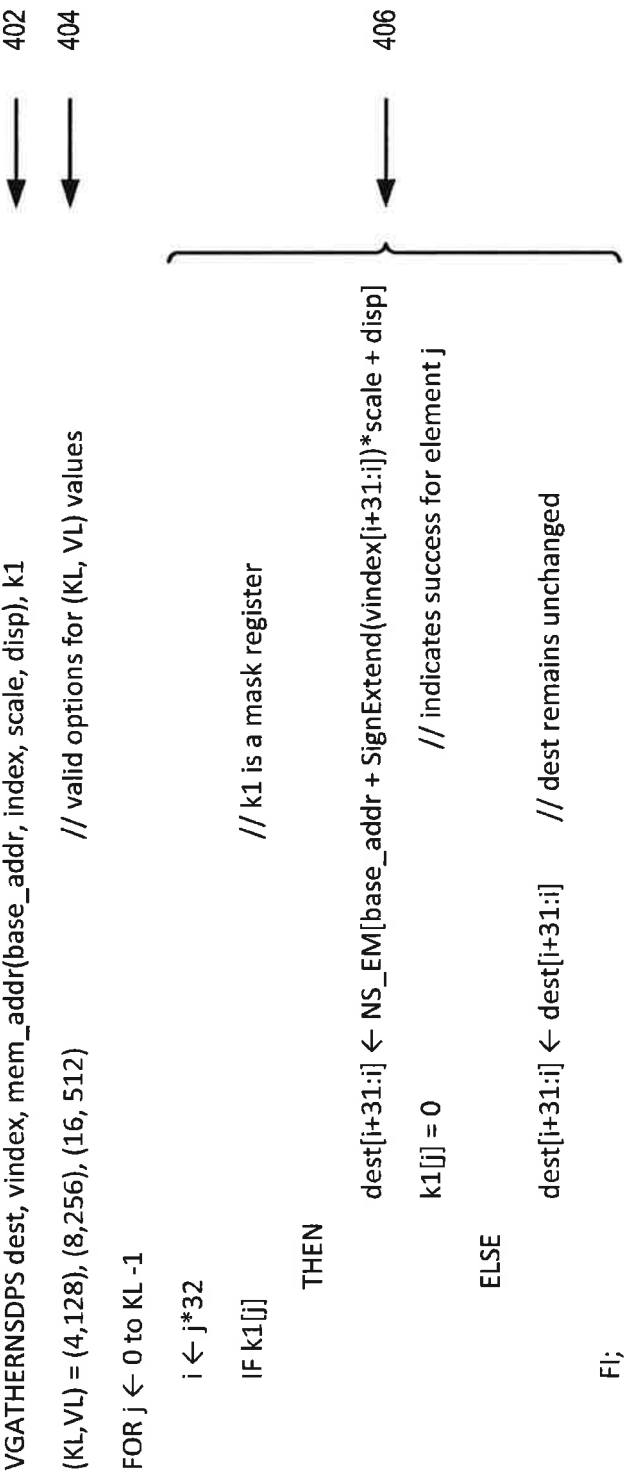


FIG. 4A

```

VMOVSTRIDENS DPS dest, stride, base_mem_addr, k1
(KL, VL) = (4, 128), (8, 256), (16, 512)    // valid options for (KL, VL) values
FOR j ← 0 to KL-1
    I ← j*32
    IF k1[j]
        // k1 is a mask register
        THEN
            dest[i+31:i] ← NS_EM[base_mem_addr + SignExtend(stride)]
            k1[j] = 0
            // indicates success for element j
        ELSE
            dest[i+31:i] ← dest[i+31:i]    // dest remains unchanged
    FI;
END FOR

```

452
454
456

FIG. 4B

Figure 5A



CORE 590

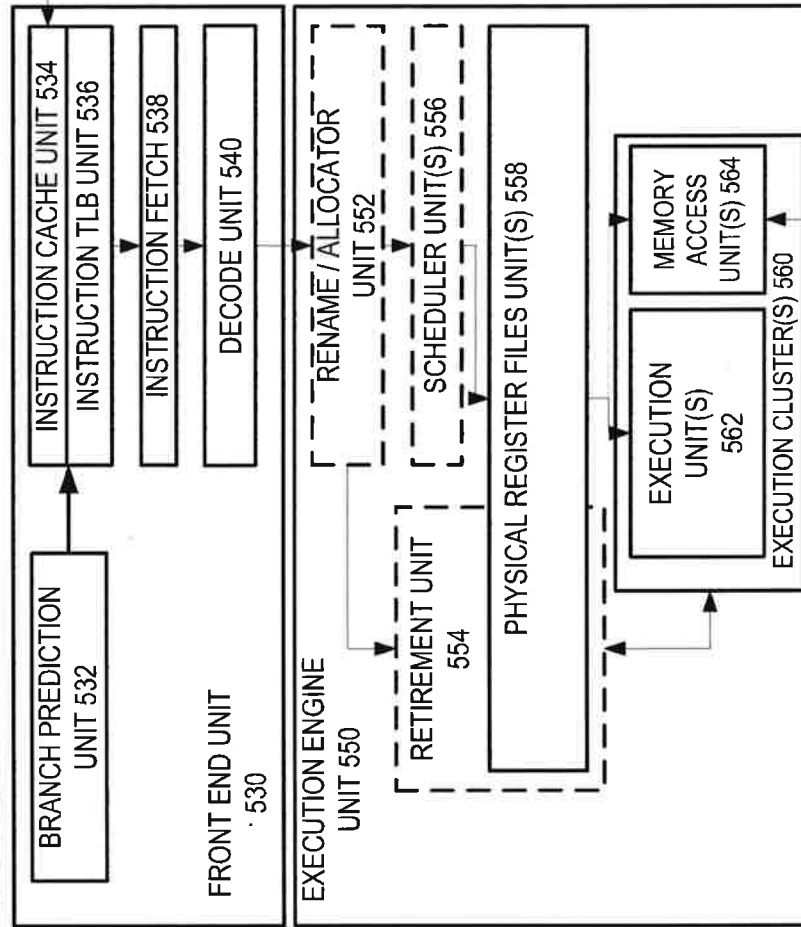
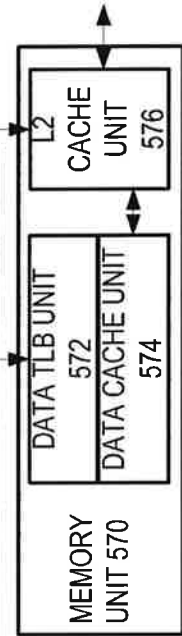


Figure 5B



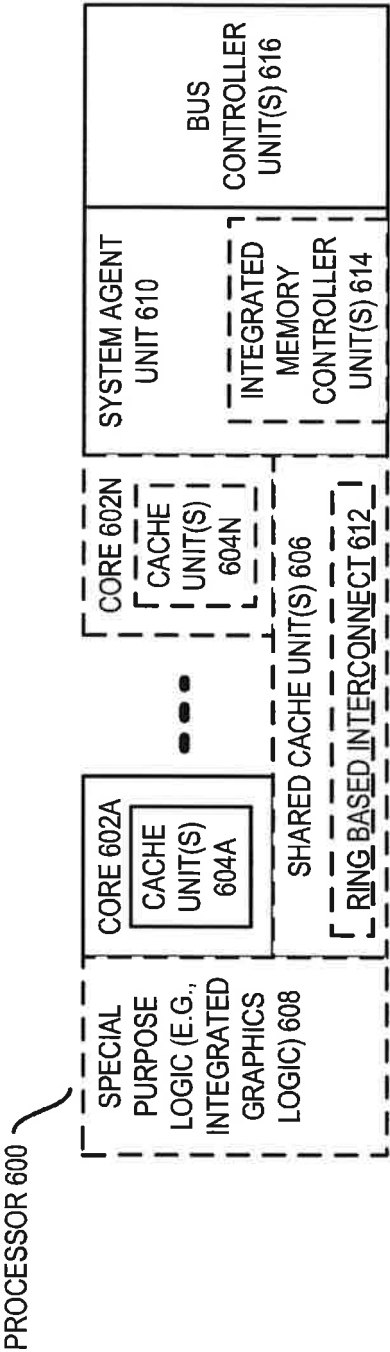


Figure 6

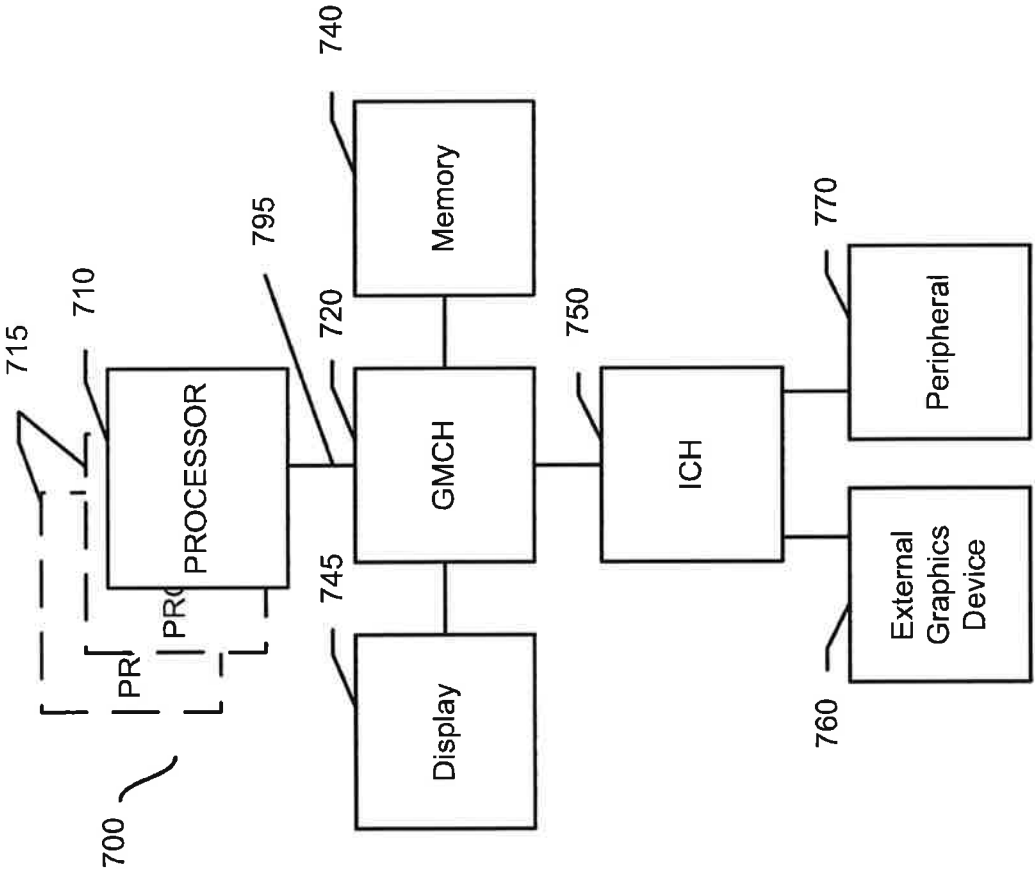


FIG. 7

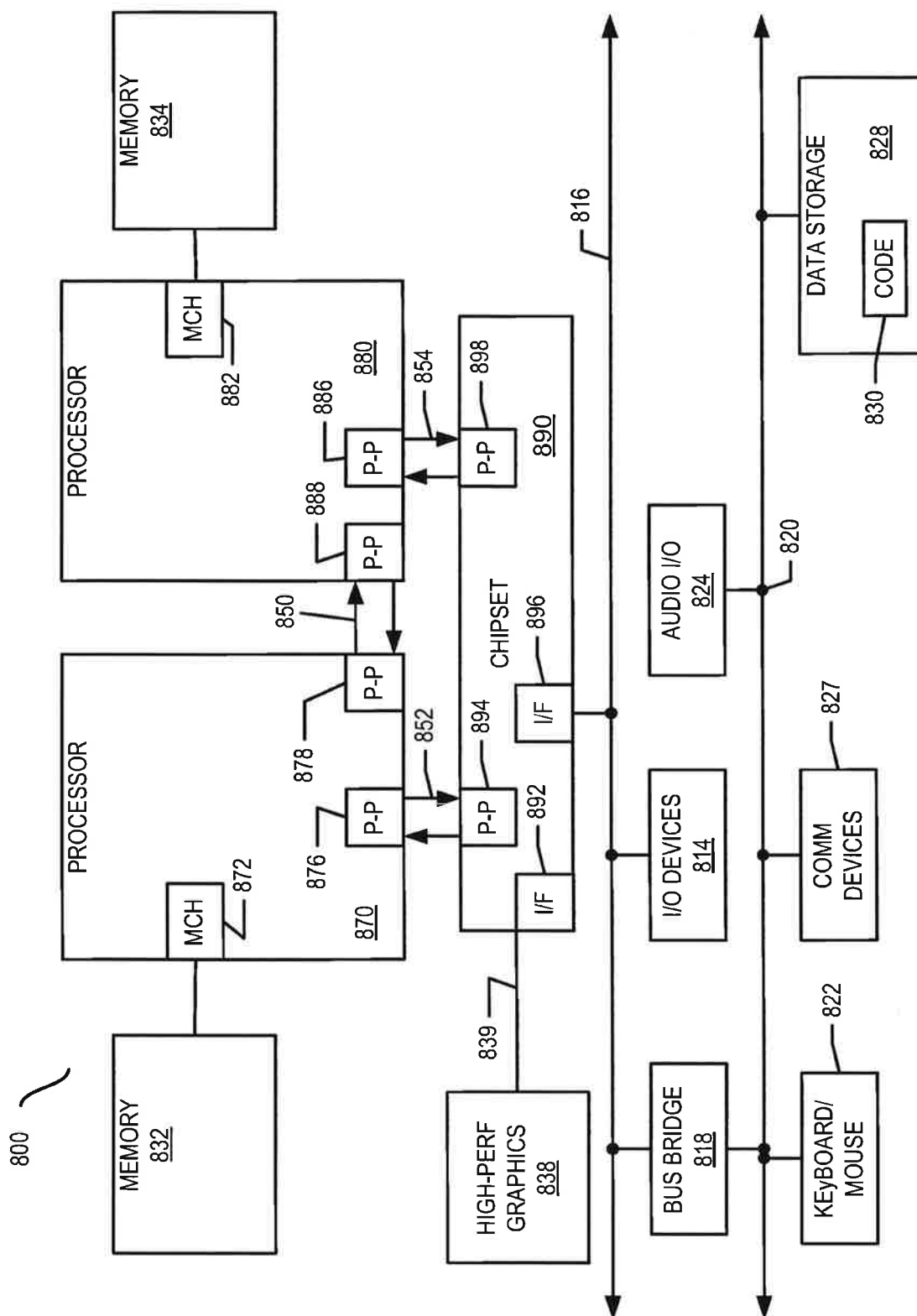


FIG. 8

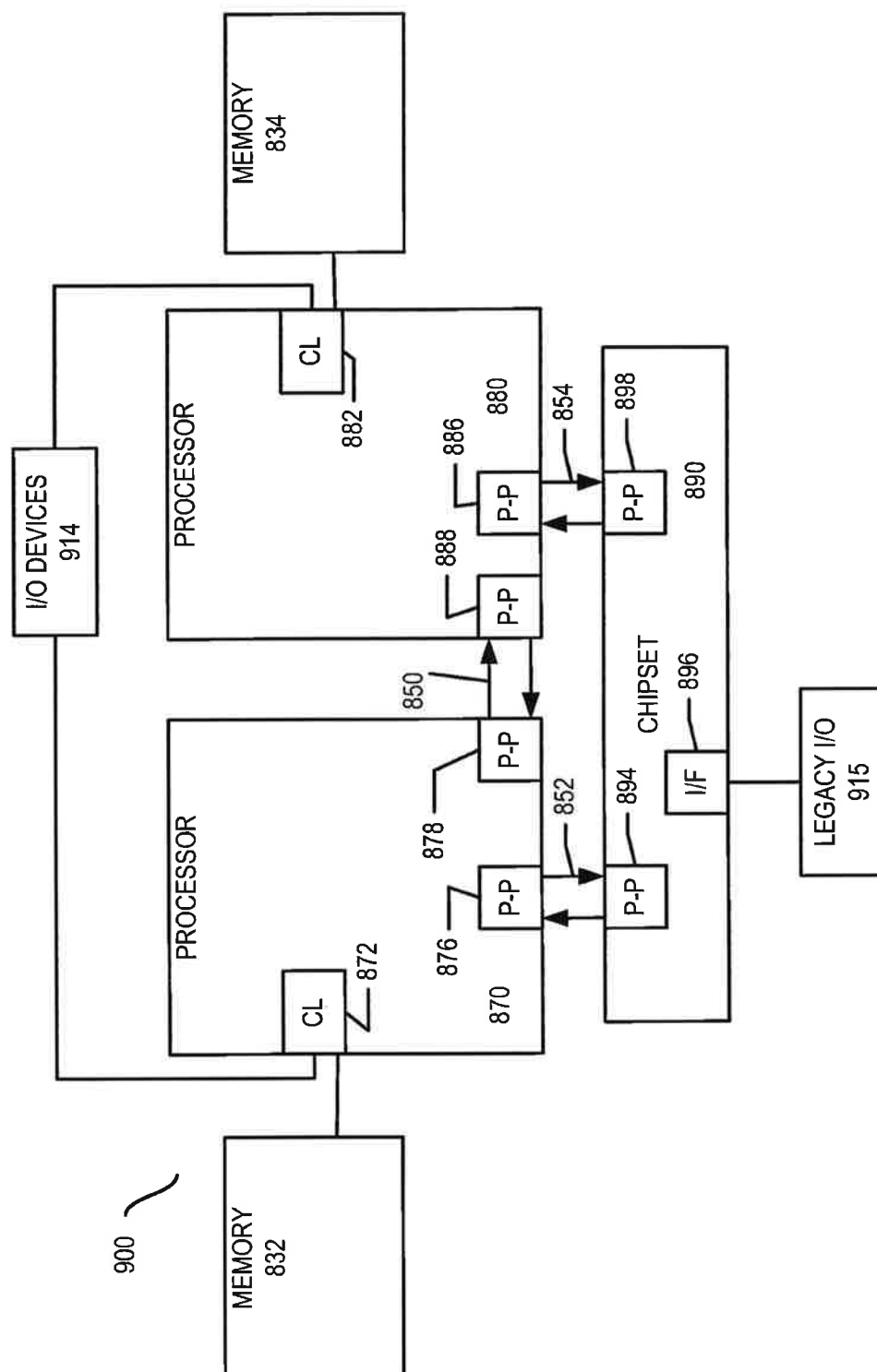


Figure 9

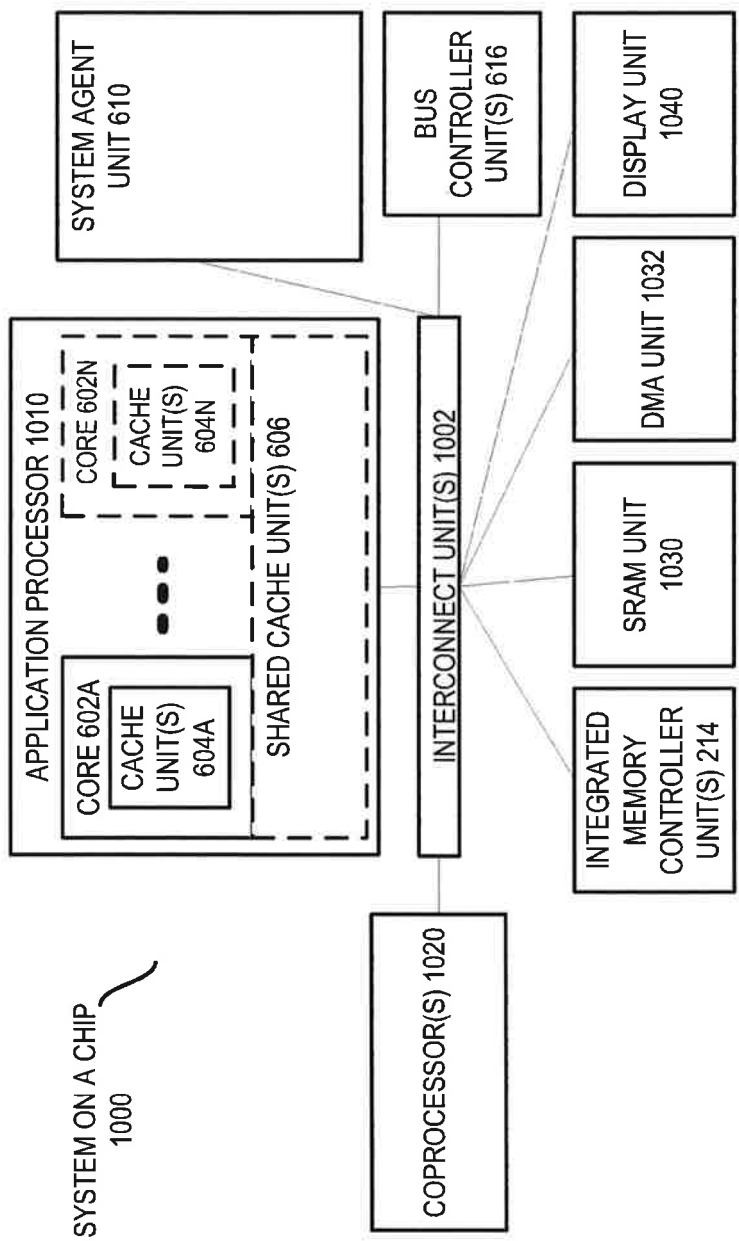
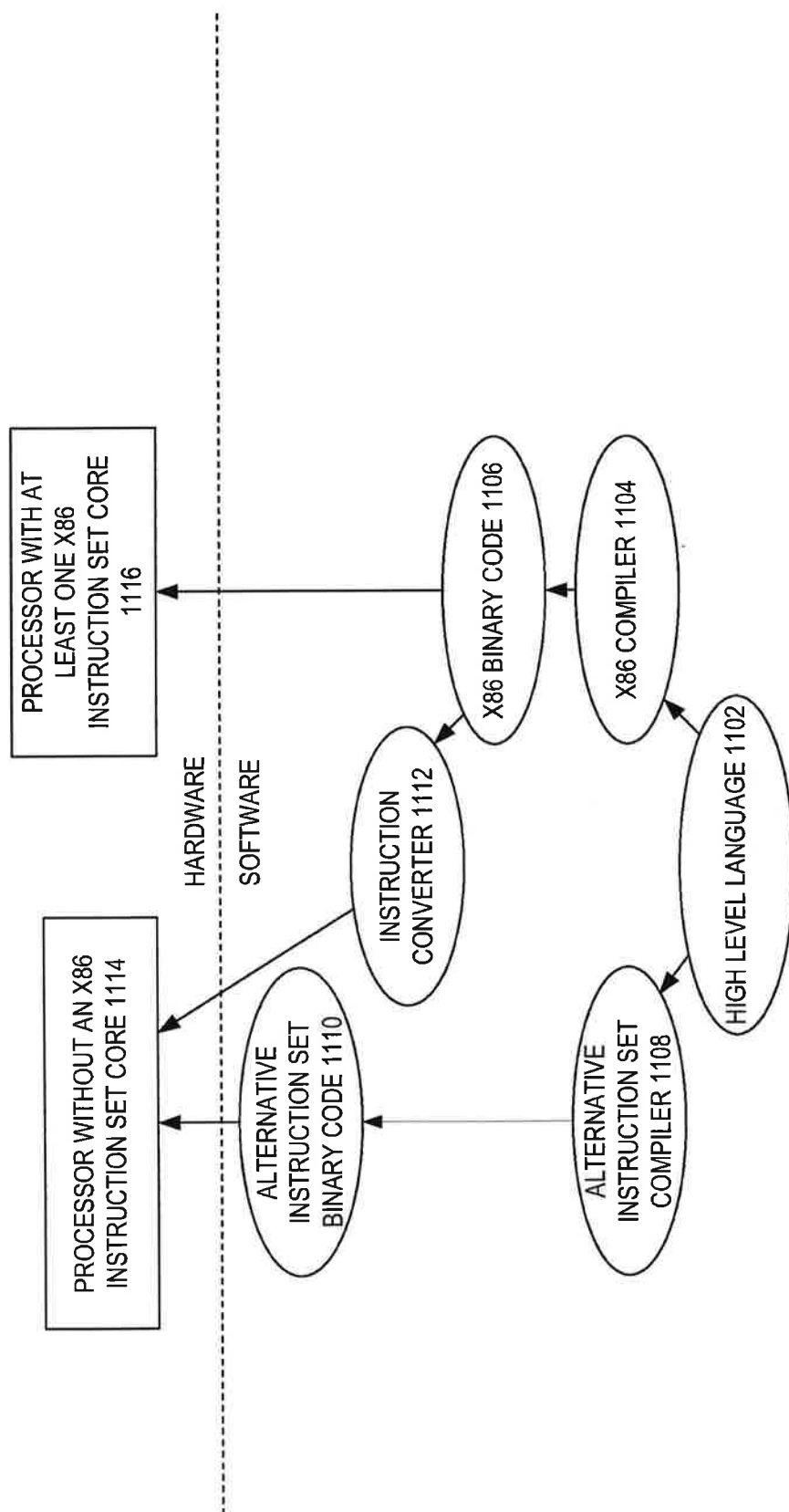
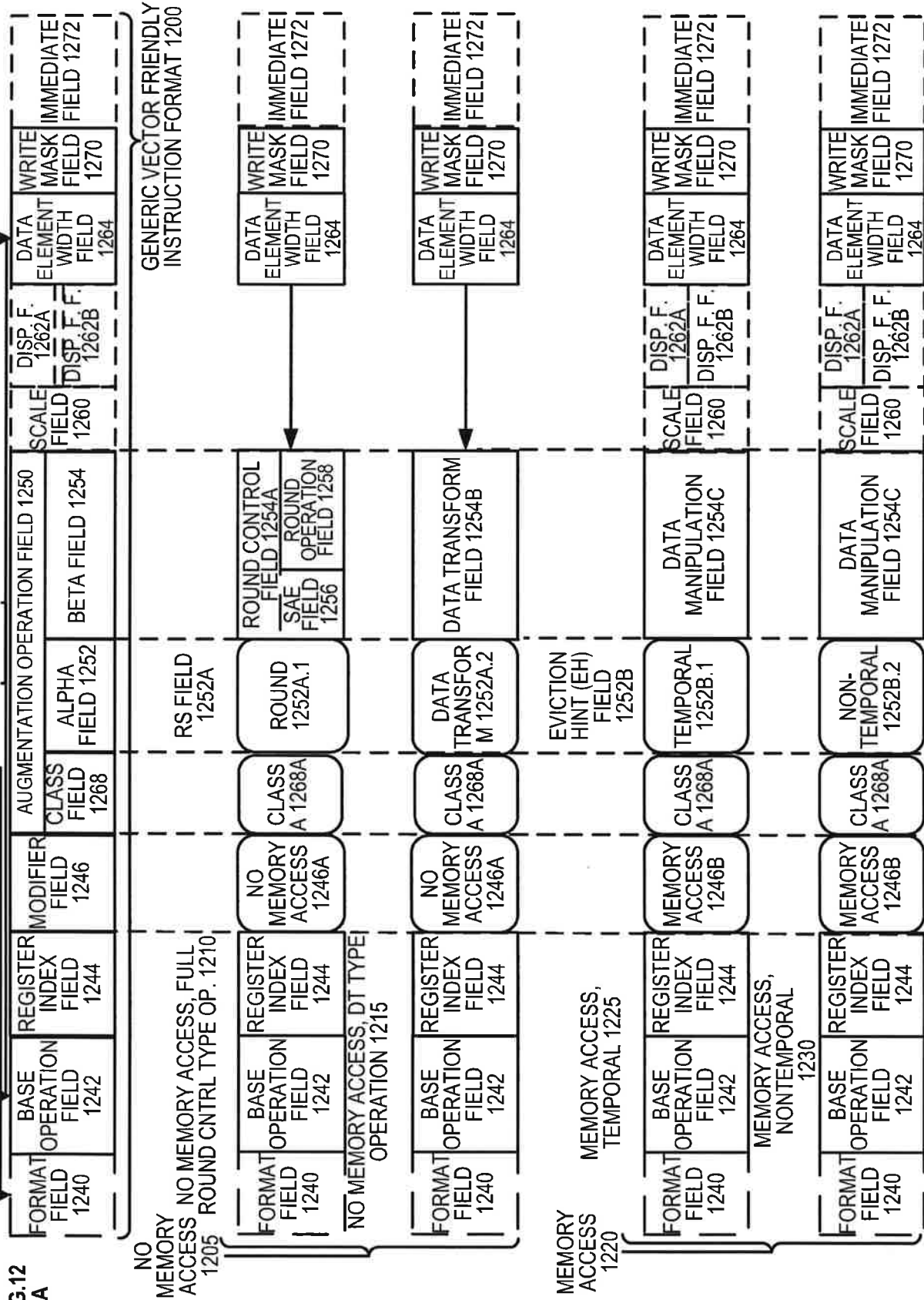
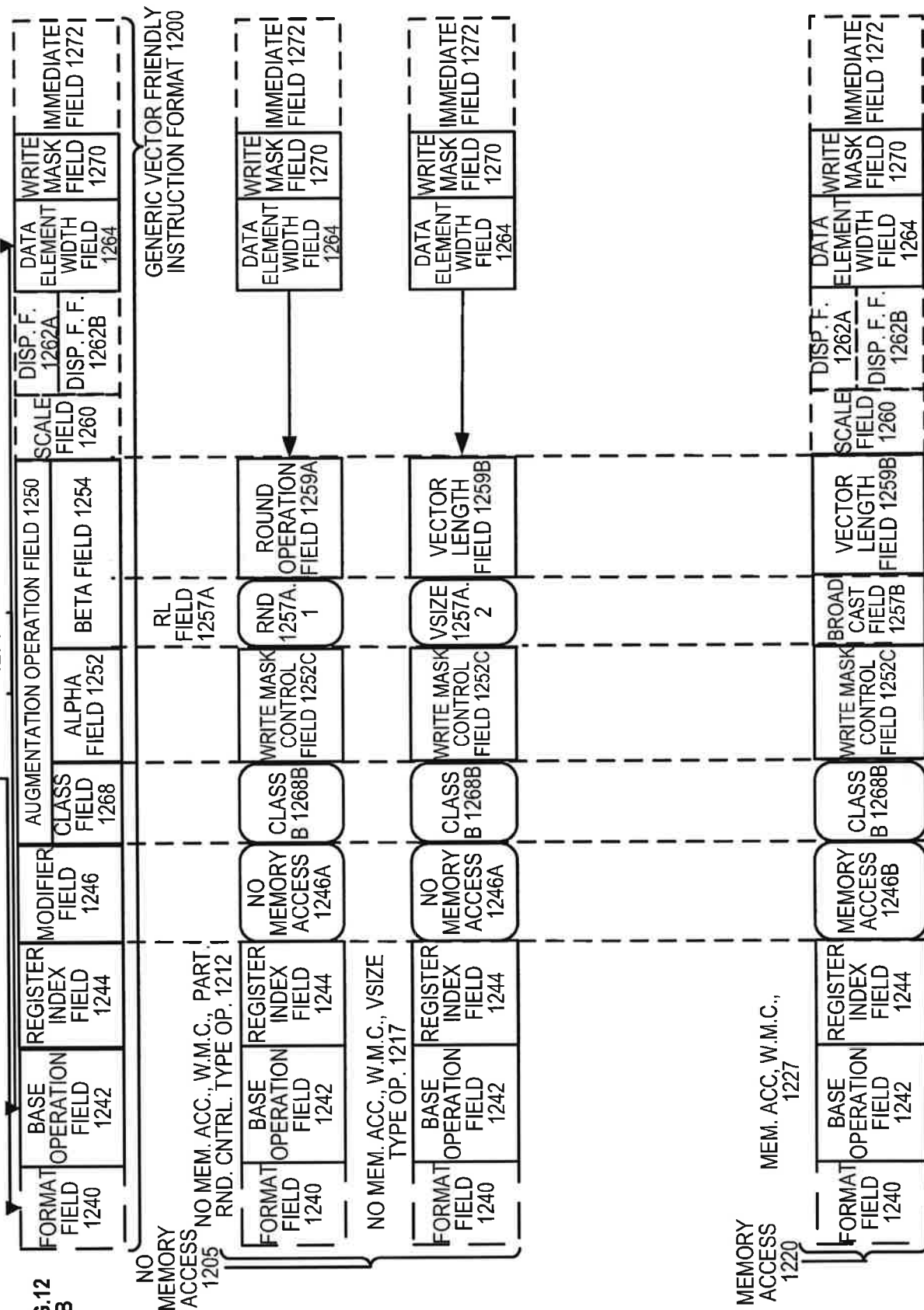


Figure 10

**FIG. 11**

FULL OPCODE FIELD
1274FIG. 12
A

FULL OPCODE FIELD
1274FIG. 12
B

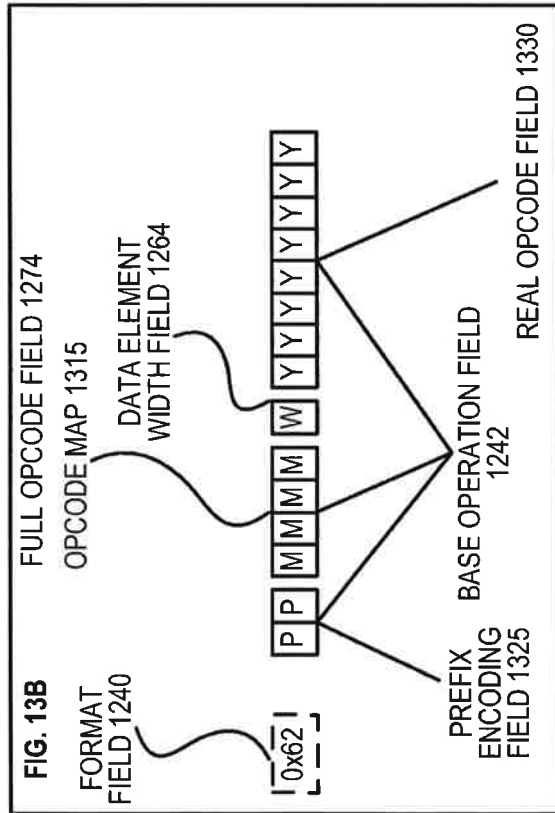
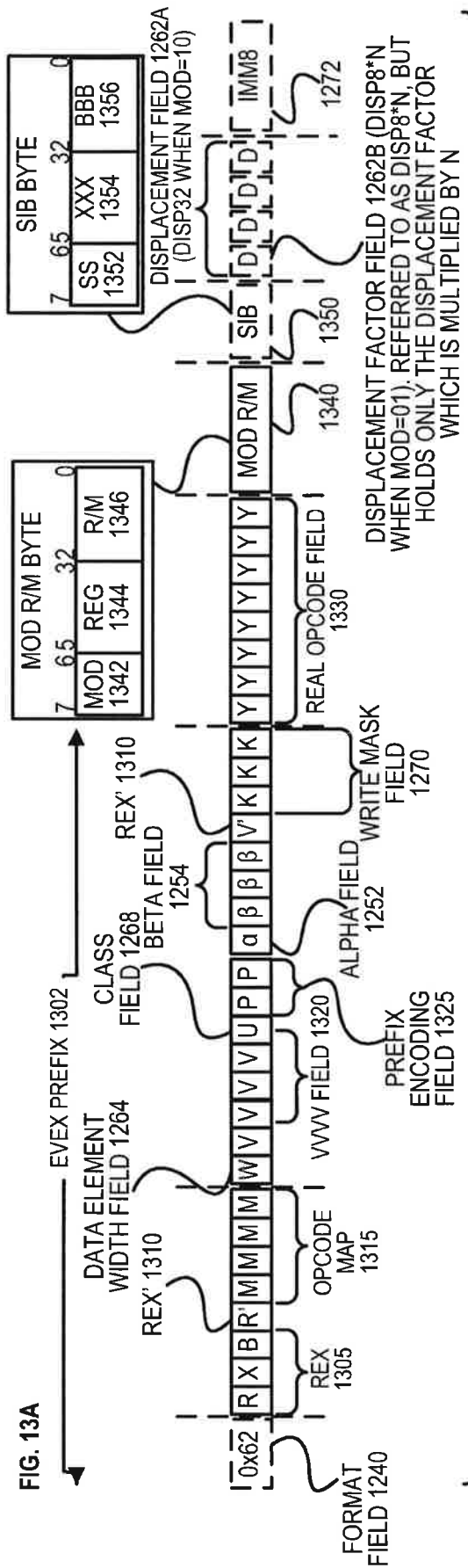
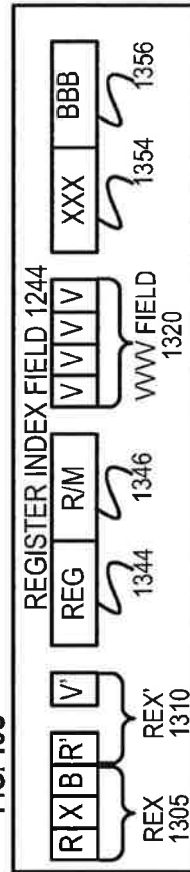
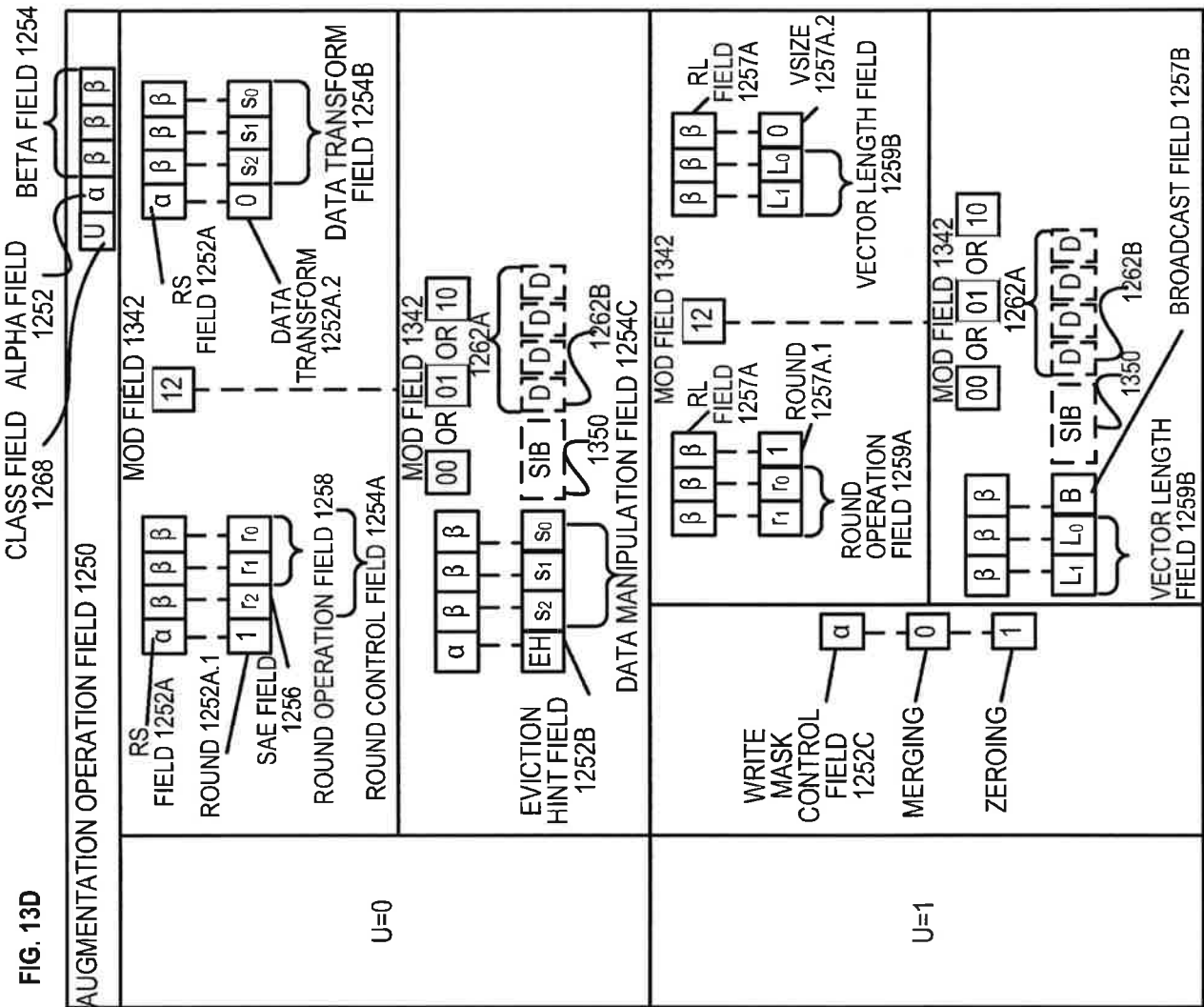


FIG. 13C





REGISTER ARCHITECTURE 1400

FIG. 14

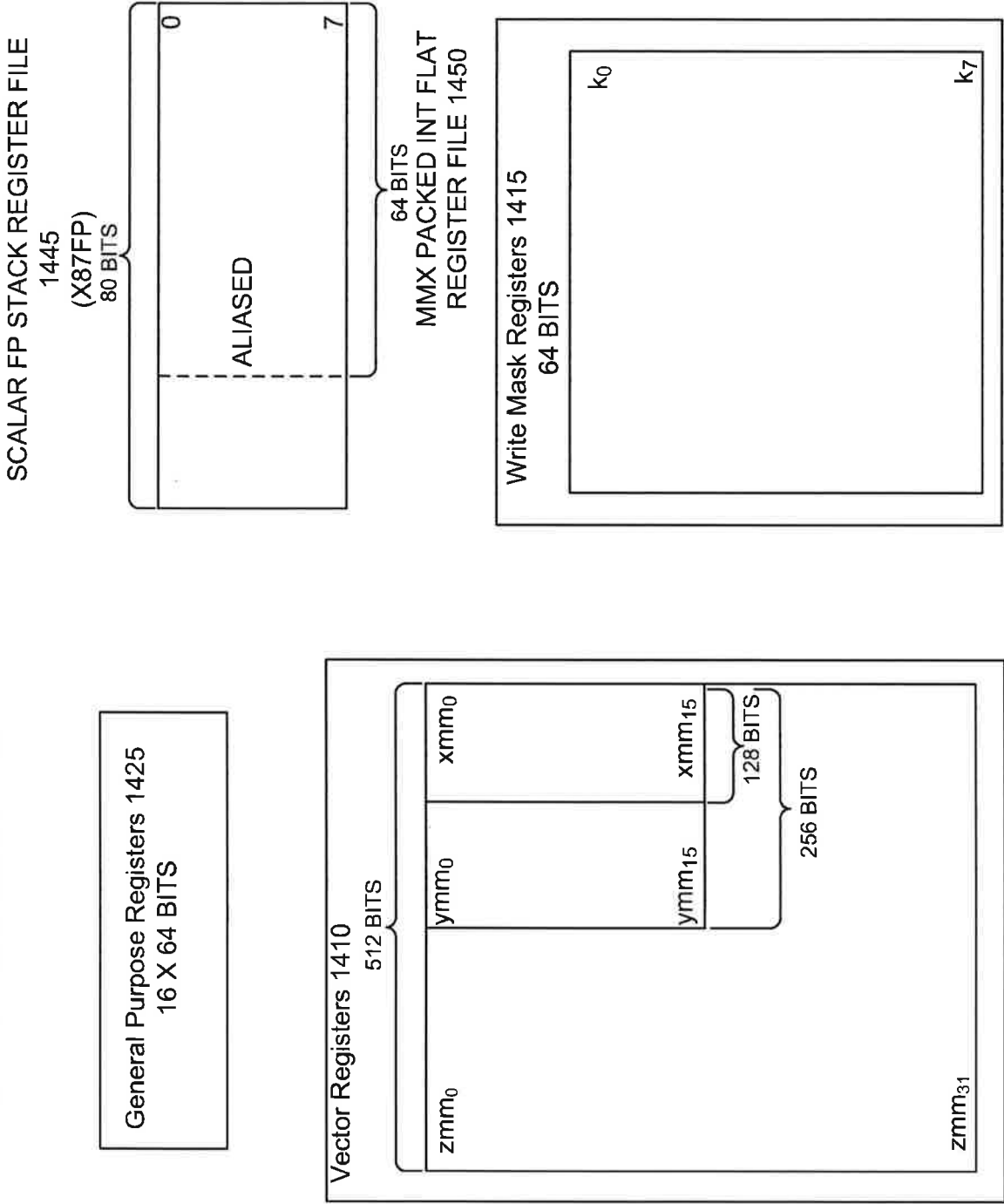


FIG. 15A

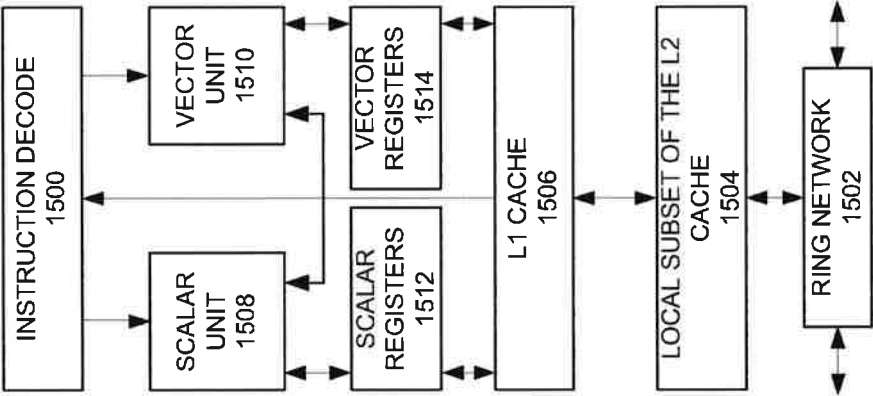


FIG. 15B

