

WHAT IS CLAIMED IS:

1. A method of packaging a semiconductor device, comprising:
 - providing a first insulation layer comprising stacked prepreg layers;
 - forming a metallic protective layer on a first surface of the first insulation layer;
 - forming a first alignment mark on the first insulation layer;
 - forming an accommodation cavity in the first insulation layer according to the first alignment mark;
 - forming a second alignment mark on a second surface of the first insulation layer;
 - attaching a carrier plate on the first surface of the first insulation layer through a thermal release tape layer;
 - temporarily fixing the semiconductor device on the thermal release tape layer within the accommodation cavity according to the second alignment mark;
 - placing a semi-cured second insulation layer over the second surface of the first insulation layer, and laminating and curing the second insulation layer;
 - removing the carrier plate and the thermal release tape layer; and
 - forming a re-distribution layer on the second insulation layer, the re-distribution layer being electrically connected with the semiconductor device.
2. The method according to claim 1, wherein the first insulation layer is formed by laminating and curing the stacked prepreg layers.
3. The method according to claim 1, wherein a thickness of the metallic protective layer is smaller than 1 μm .
4. The method according to claim 1, wherein the metallic protective layer is made of copper.

5. The method according to claim 1, wherein the metallic protective layer is formed by a sputtering process.

6. The method according to claim 1, wherein the first alignment mark comprises plural fiducial holes.

7. The method according to claim 6, wherein the plural fiducial holes are four fiducial holes which are respectively located adjacent to the four corners of the first insulation layer.

8. The method according to claim 6, wherein the plural fiducial holes run through the first insulation layer and the metallic protective layer.

9. The method according to claim 1, wherein the accommodation cavity runs through the first insulation layer and the metallic protective layer.

10. The method according to claim 1, wherein the second alignment mark is arranged around the accommodation cavity.

11. The method according to claim 1, wherein the first alignment mark, the accommodation cavity and the second alignment mark are formed by laser drilling or mechanical drilling.

12. The method according to claim 1, wherein after the step of forming the accommodation cavity, the method further comprises steps of:

performing a desmearing process to remove contaminant retained in the accommodation cavity and roughen the second surface of the first insulation layer; and

removing the metallic protective layer.

13. The method according to claim 1, wherein before the step of placing the second insulation layer over the second surface of the first insulation layer, the method further comprises a step of attaching at least one first tape on the second surface of the first insulation layer to cover a first side of the first alignment mark.

14. The method according to claim 13, wherein after the step of removing

the carrier plate and the thermal release tape layer, the method further comprises steps of:

- attaching at least one second tape on the first surface of the first insulation layer to cover a second side of the first alignment mark;

- placing a semi-cured third insulation layer on the first surface of the first insulation layer to cover the second tape;

- laminating and curing the third insulation layer; and

- removing the first tape and the second tape, so that a semi-finished package structure is produced.

15. The method according to claim 14, wherein the step of forming the re-distribution layer comprises steps of:

- forming at least one via corresponding to at least one conducting terminal of the semiconductor device in the second insulation layer by a laser drilling or mechanical drilling process, and forming at least one through-hole in the semi-finished package structure and near the semiconductor device by a laser drilling or mechanical drilling process, wherein the through-hole runs through the second insulation layer, the first insulation layer and the third insulation layer;

- forming a metal layer on a part of the second insulation layer, a part of the third insulation layer and an inner surface of the through-hole, and filling the metal layer in the via;

- forming a fourth insulation layer on two opposite surfaces of the semi-finished package structure, and exposing a part of the metal layer; and

- forming at least one conductive pattern on a part of the metal layer, and allowing the at least one conductive pattern to be electrically connected with the corresponding conducting terminal of the semiconductor device.

16. The method according to claim 1, wherein the semiconductor device comprises a power switch.