

High frequency AC/AC converter with power factor correction.

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The present invention relates to apparatus for converting an AC line voltage of low frequency into a high frequency output AC voltage and, more particularly, to a low cost miniaturized electronic ballast circuit for operation of electric discharge lamps.

In prior art electronic ballast circuits, a separate power factor correction circuit is employed in order to obtain a high power factor. Fig. 1 depicts a conventional half-bridge electronic ballast where a boost converter is used for power factor correction. An electromagnetic interference filter (EMI) is coupled to the terminals of a low frequency AC line voltage, for example, 50 Hz or 60 Hz, and is used to filter out the high frequency noise generated by the high frequency operation of a boost converter and a half-bridge DC/AC inverter coupled in cascade to form the electronic ballast circuit. The line voltage is rectified by a full bridge rectifier D1-D4 to produce a pulsatory DC voltage. In the boost converter stage, which is coupled to the output of the rectifier circuit, the current flow through the inductor L is monitored by a reference current generated from the rectified line voltage by means of the control circuit CCA so that the current waveform is shaped to be the same as and to be in phase with the rectified voltage waveform. This is done by controlling the ON duty ratio and/or the frequency of the MOSFET switch Q0.

The boost converter receives the pulsating DC voltage from the bridge rectifier D1-D4. When the switching transistor Q is turned on, a current flows from the rectifier bridge through the inductor L and the transistor Q so that electromagnetic energy is stored in the electromagnetic field of the inductor. When the transistor Q is switched off, the electromagnetic energy in the inductor is transferred to the storage capacitors Ce1 and Ce2 as a result of a current that flows via the inductor L and the blocking diode D. This represents the conventional mode of operation of a boost converter.

The output of the boost converter is a DC voltage across capacitors Ce1 and Ce2 coarsely regulated by the control circuit A. This DC voltage is then inverted into a high frequency AC voltage by the high frequency half-bridge DC/AC inverter coupled to the output of the boost converter so that a regulated output power can be obtained for the load. Since the input power of the boost converter possesses a low frequency component (100 Hz or 120 Hz) and the output power of the half-bridge DC/AC inverter is a regulated high



frequency power, an energy storage capacitor, here shown as capacitors Ce1 and Ce2, is placed between the boost converter stage and the half-bridge inverter stage so as to balance the input power and the output power.

Depending on the manner in which the current flow through the inductor L is controlled during each switching period, the operation mode of the boost converter can be classified into two categories, i.e. Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). In CCM, the high frequency ripple of the current through the inductor L can be made small so that the stress on the EMI filter can be reduced. A drawback of this control method is that the duty ratio of the switching MOSFET Q0 has to vary with the rectified line voltage, thus resulting in a rather complex control circuit. In the DCM, the peak values of the current through the inductor L automatically follow the waveform of the rectified line voltage if the on time of the MOSFET is constant. Therefore, the control circuit can be greatly simplified. This advantage is the main reason why DCM is usually adopted in the boost converter stage for power factor correction in low-power applications.

An important disadvantage of the electronic ballast circuit of Fig. 1 is that the requirement of a separate power factor correction (PFC) stage and a separate DC/AC inverter stage increases the cost and size of the overall ballast device. One prior art attempt to reduce the circuit complexity is described in U.S. Patent 4,564,897 (1/14/86) in which a smoothing (i.e. power factor correction) circuit and an inverter circuit share a common switching element and the control circuit thereof. This U.S. patent is hereby incorporated by reference and discloses a power supply which employs a relatively small inductor while providing a relatively high power factor. The high frequency AC output voltage has a relatively low line-frequency ripple component which makes it suitable for operation of a discharge lamp. However, this power supply has a serious problem in that it is very difficult to regulate the inverter output at a desired stable level in the event of a variation in the input AC voltage or in the case of varying load requirements.

U.S. Patent 5,182,702 (1/26/93) describes an inverter device which attempts to solve some of the disadvantages of the prior art by providing a simpler control circuit for the overall system. This inverter device includes a full wave rectifier supplying a pulsating DC voltage from an input AC voltage to a smoothing (power factor correction) circuit. The power factor correction circuit includes an inductor, a smoothing capacitor and a switching element for chopping the pulsating DC voltage through the inductor into a smooth DC voltage at the capacitor. An inverter is provided which has a switching element common

to the power factor correction circuit and operative to switch the DC voltage to apply a high frequency voltage to a load circuit including a load, an inductance and a capacitor. The inductance and capacitor define a resonant circuit providing the load with an oscillating current composed of first and second opposite flowing currents. The oscillating current flows
5 for a nominal on-time determined by a circuit constant of the resonant circuit. A controller detects the termination of the second current and excites the common switching element at a time dependent thereon so as to start the flow of the first current. The controller includes a timer for separately controlling the actual on-time for the flow of the first current within the nominal on-time. This makes it possible to regulate the accumulated DC voltage on the
10 smoothing capacitor at a desired level by controlling the actual on-time period of the common switching element. This circuit also has certain disadvantages which limits its use in practical applications.

15 It is therefore an object of the present invention to provide a low cost miniaturized electronic ballast circuit or high frequency AC/AC converter having improved operating characteristics and which is not subject to the limitations of the prior art.

It is a further object of the invention to provide a simple and compact high frequency AC/AC converter circuit having a high power factor and low current
20 distortion.

It is another object of the invention to provide an electronic ballast circuit which requires only one control circuit and fewer switching transistors than the electronic ballast circuit shown in Fig. 1.

It is a further object of the invention to provide an electronic ballast
25 circuit with a superior lamp ignition characteristic to that of the prior art inverter device.

A still further object of the invention is to provide an electronic ballast circuit or high frequency AC/AC converter that produces a more sinusoidal waveform and substantially reduces the level of voltage spikes generated across the diodes of the full-wave rectifier at the input of the electronic ballast circuit or high frequency converter.

30 Another object is to provide an electronic ballast circuit including a high frequency DC/AC inverter part utilizing a resonant LC circuit that improves the circuit performance and makes for greater flexibility in circuit design.

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It is a further object of the invention to combine the functions of the PFC boost converter and the high frequency DC/AC inverter into a single combination AC/AC inverter with input power factor correction.

It is yet another object of the invention to use a pulse width modulation (PWM) technique which results in a very simple control circuit for the electronic ballast.

The foregoing and other objects and advantages of the invention are achieved, inter alia, by combining the separate functions of the input PFC boost converter and the high frequency DC/AC inverter into a single stage high frequency AC/AC inverter with power factor correction thereby providing power factor correction and a high frequency DC/AC inverter operating characteristic.

Since there are two separate stages in the prior art system shown in Fig. 1, two separate control circuits (CCA) and (CCB) are required. The combination circuit of the present invention combines both the power factor correction stage and the high frequency inverting stage into a single stage so that one power stage and its corresponding control circuitry are no longer required and the circuit cost is thereby reduced.

In an embodiment according to the invention a high-frequency converter apparatus comprises:

first and second input terminals for connection to a source of supply voltage for the converter,

output means including a resonant circuit for connection to a load to be driven by the converter,

a first series circuit including an inductor means, a rectifier element, and a first semiconductor controlled switching device coupled to said input terminals.

In a preferred embodiment according to the invention a high frequency converter apparatus comprises a pair of input terminals for connection to a 60 Hz AC line voltage or the like which are further connected to a pair of input terminals of the high frequency AC/AC converter with power factor correction via an electromagnetic interference filter and a diode bridge rectifier circuit. The second input terminal is connected to a common line of the high frequency converter. Preferably a first switching field effect transistor (FET) is connected to a first junction point between the diode and the storage capacitor and to the common line. A second switching FET is connected to a second junction point between the storage and isolation capacitors and to the common line. The transformer secondary winding is coupled to the load (e.g. a discharge lamp) and a single control circuit receives a feedback signal from the load circuit to control the switching of the first and

second field effect transistors at a high frequency. A third capacitor is coupled across the transformer secondary winding and forms an LC resonant circuit with the second inductor.

Two distinct control techniques can be employed in accordance with the present invention. One is constant duty ratio control and the other is duty ratio sweeping control. These control techniques will be described in greater detail in connection with the detailed description of the drawings.

The foregoing and other objects and advantages of the present invention will become apparent from the following detailed description thereof when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block schematic diagram of a conventional electronic ballast circuit with input PFC,

Fig. 2 is a block schematic diagram of a first embodiment of the invention,

Fig. 3 is a graphical representation of the relationship of the normalized line current waveform over a half cycle as a function of the normalized energy storage capacitor voltage (Gain) using a constant duty ratio control scheme,

Fig. 4 is a block schematic diagram of a control circuit for constant duty ratio control,

Fig. 5 provides a time diagram of the signals present in the constant duty ratio control circuit of Fig. 4,

Fig. 6 is a time diagram showing the variation of duty ratio (D) over a half line period T_1 ,

Fig. 7 is a graph of the ratio of maximum and minimum duty ratio for duty ratio sweep control,

Fig. 8 is a block schematic diagram of a part of a control circuit for duty ratio sweep control,

Fig. 9 is a block schematic diagram of a second embodiment of the invention,

Fig. 10 is a block schematic diagram of a third embodiment of the invention in which the resonant circuit is connected to the MOSFET Q1, and

Fig. 11 is a block schematic diagram of a fourth embodiment of the invention showing a half-bridge connection of the resonant circuit.

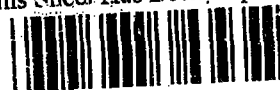


Fig. 1 shows a conventional electronic ballast circuit with input PFC, which consists of a boost converter 1 that provides the power factor correction function and a high frequency half bridge DC/AC inverter 2 that supplies a high frequency energizing current to the load (discharge lamp) 3. A first control circuit CCA controls a switching FET Q in the boost converter and a second control circuit CCB controls the high frequency switching FETs Q11 and Q21 in the high frequency inverter. This conventional circuit has been described above and therefore will not be further discussed. The requirement of a separate PFC stage and a separate HF DC/AC inverter increases the cost and size of the overall ballast system shown in Fig. 1.

Referring now to Fig. 2, there is shown a block schematic diagram of a basic arrangement in accordance with a first embodiment of the present invention. A pair of input terminals 4, 5 supply a 60 Hz (50 Hz) AC line voltage to an electromagnetic interference filter 6. The output of the electromagnetic interference filter is in turn connected to input terminals of a bridge rectifier circuit 7 which produces a pulsating DC voltage at its output terminals 8, 9. Terminal 8 is positive with respect to terminal 9.

Terminals 8 and 9 are connected to the input lines of the combination PFC boost converter-high frequency DC/AC inverter 10. A series circuit consisting of a power factor correction inductor 11, blocking diode 12, energy storage capacitor C_e and DC blocking isolation capacitor C_b , a resonant inductor 13 and the primary winding of an output transformer T is connected to the supply terminals 8 and 9.

A first switching MOSFET Q1 is connected between a junction point 14 and the common line 9. This switching element is common to both the boost converter circuit part and the high frequency inverter circuit part of the combination circuit 10. A second switching MOSFET Q2, which is only a part of the HF inverter circuit part, is connected between a junction point 15 and the common line 9. Diodes 16 and 17 are connected in parallel with the switching transistors Q1 and Q2, respectively. Small capacitors are connected in parallel with the diodes 16 and 17. These diodes and capacitors may be inherent components of the MOSFET devices Q1 and Q2.

The secondary winding of transformer T is connected to a load illustrated as a resistor R_L . In one preferred embodiment of the invention, the load is one or more discharge lamps and the combination PFC converter/HF inverter constitutes an electronic ballast circuit for the discharge lamp(s). A resonant capacitor 20 is connected across the secondary winding of transformer T and in parallel with the load R_L .



A voltage clamp diode D1 is connected between the junction of inductor 11 (L_{in}) and diode 12 (D_{in}) and the common return line 9.

A single control circuit 18 has first and second output lines coupled to respective control electrodes of the switching transistors Q1 and Q2 in order to control the high frequency switching thereof. The control circuit is itself controlled as a function of the load voltage, which is schematically represented by the input control line 19.

The two MOSFETs Q1 and Q2 are turned on and off alternately by the control circuit 18 at a fixed duty ratio D, which is defined as the on-time of the switching device Q1 over one switching period T_s , i.e. $D = T_{on}/T_s$. Inductor 11 (L_{in}), diode 12 (D_{in}), MOSFET Q1, body diode 17 of MOSFET Q2, and energy storage capacitor C_e form a boost converter for power factor correction. The half-bridge DC/AC inverter consists of MOSFETs Q1, Q2, the energy storage capacitor C_e , DC blocking isolation capacitor C_b , resonant inductor 13 (L_r), isolation transformer T, and resonant capacitor 20 (C_r).

For the boost converter part of the circuit, the duty ratio of MOSFET Q1 is fixed during each line period in order to avoid large low frequency (120 Hz or 100 Hz) ripple at the output. Therefore, it is preferable that the operation mode of the boost converter be DCM. Regulation of the output voltage V_{ce} of the boost converter, which is produced across the capacitor C_e , is achieved by controlling the duty ratio of MOSFET Q1. This control method is termed constant duty ratio control and a detailed description of the operation of the control circuit will be given below. When transistor Q1 is turned on, the rectified line voltage is applied to the inductor 11 (L_{in}). Thus, its current is linearly increased from zero as follows:

$$i_{in} = \frac{|V_{in}|}{L_{in}} t \quad (1)$$

where $|V_{in}|$ represents the rectified line voltage at the bridge rectifier output terminals 8, 9 during the on-time interval of transistor Q1. The voltage $|V_{in}|$ can be considered to be constant over a high frequency switching cycle. Energy is stored in the inductor L_{in} when transistor Q1 is on. The peak current is obtained as follows:

$$i_{in} = \frac{|V_{in}|}{L_{in}} xDT_s \quad (2)$$



where D is the duty ratio and T_s is the switching period. Equation (2) indicates that the peak values of the inductor current i_{in} follows the waveform of $|V_{in}|$ since both T_s and D are constant. When switching transistor Q1 is turned off, the inductor current i_{in} continues to flow via the body diode 17 of MOSFET Q2. Therefore, the voltage across L_{in} is given by:

$$V_{Lin} = |V_{in}| - V_{ce} \quad (3)$$

The inductor current charges the capacitor C_e and the energy stored in L_{in} during the on period of transistor Q1 is transferred to capacitor C_e . Thus, the inductor current is linearly discharged as follows:

$$i_{in} = \frac{|V_{in}|}{L_{in}} x D T_s - \frac{V_{ce} - |V_{in}|}{L_{in}} x (t - t_{off}) \quad (4)$$

where t_{off} is the instant of time when transistor Q1 is turned off. When the current reaches zero, it stays at zero ideally due to the presence of diode 12. The voltage across the inductor 11 will be equal to zero ideally, resulting in a voltage of $V_{ce} - |V_{in}|$ across the diode 12. However, due to the presence of the reverse recovery current and the junction capacitance of the diode 12, an undesirable oscillation appears in the voltage of the diode 12. This oscillation not only causes extra power loss in the diode 12 (D_{in}) but also causes excessive voltage stress of this diode which may shorten the diode lifetime. A diode D_{11} is therefore added between the junction of inductor 11 and diode 12 and the common return line 9 in order to clamp the maximum diode voltage to the voltage V_{ce} of the storage capacitor C_e . This method is effective but it is not optimum simply because the diode voltage is not clamped to its steady state value $V_{CE} - |V_{in}|$. Therefore, some small oscillation still remains. The current i_{in} flowing through the inductor 11 has a triangular waveform. Its average current over one switching period is obtained as follows from analysis:

$$I_{in} = \frac{D^2 T_s V_{ce}}{2L_{in}} \frac{|V_{in}| / V_{CE}}{1 - |V_{in}| / V_{CE}} \quad (5)$$

With the high-frequency harmonics filtered by the EMI filter, the line current is equal to the average current I_{in} . Therefore, line current i_{line} is obtained as follows from (5) with the substitution of $|V_{in}| = V_m \sin \omega t$ considering the rectification:

$$(6)$$

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$$i_{line} = \frac{D^2 T_s V_{ce}}{2L_{in}} \frac{\frac{1}{M_p}}{1 - \frac{1}{M_p} |\sin WT|} \cdot \sin WT \text{ where,}$$

$$M_p = \frac{V_{ce}}{V_m}$$

(7)

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It can be seen that the current i_{line} is basically a sine wave current with distortion introduced by the term

$$1 - \frac{1}{M_p} |\sin WT|$$

10

when the duty ratio D is fixed. Fig. 3 shows the graphical representation of the line current over one line period. With the normalization by

$$\frac{D^2 T_s V_{ce}}{2L_i} \frac{1}{M_p}$$

15 taking M_p as a parameter. From Fig. 3, it is seen that as M_p is made larger, the sine wave is closer to the line current, resulting in a higher power factor and a lower THD (total harmonic distortion). However, higher M_p results in higher V_{ce} , which will increase the voltage stress of the FETs Q1 and Q2. Therefore, there is a trade-off between the stress of the FETs and the converter performance.

20

In the half-bridge DC/AC inverter part of the circuit, due to the switching action of transistors Q1 and Q2, a square wave voltage without a DC component is applied to the resonant circuit consisting of inductor 13 and capacitor 20 (L_r , C_r), and the isolation transformer T. The resonant circuit is closely tuned to the fundamental harmonic of the square wave voltage V_{ab} so that the voltage across the resonant capacitor 20 (C_r) is

25 substantially a high frequency sine wave. Thus, high frequency power will be supplied to the load RL.

e 30

If the high frequency DC/AC inverter part of the circuit is designed so that the resonant frequency of the resonant circuit is lower than the switching frequency, zero-voltage switching of the switching transistors Q1 and Q2 can be obtained if a small dead time interval is provided for the gate control signals. During the dead time interval, both MOSFETs are turned off. The current through the resonant inductor will charge the drain-source capacitor of one transistor and will discharge the drain-source capacitor of the other





transistor. Therefore, the drain-source voltage increases gradually after a MOSFET is turned off and falls to zero before the MOSFET is turned on. Thus, the circuit provides zero-voltage switching of the transistors Q1 and Q2.

A block diagram of the constant duty ratio control circuit and the timing relations for the signals of the control circuit are shown in Fig. 4 and Fig. 5, respectively. The switching frequency is determined by the oscillator 21 which generates a sawtooth wave signal B as shown in Fig. 5. The output voltage of the inverter 10 is fed back to the primary side of the transformer T through an additional winding 22 of the same isolation transformer T and then is rectified by a rectifier 23 to obtain a DC voltage. This DC voltage and the energy storage capacitor voltage V_{ce} are fed to the inverting (-) terminal of an error amplifier 24 via resistors R1 and R2, respectively. A feedback resistor R3 is coupled between the output and inverting input of the error amplifier.

These voltages are compared with a reference voltage V_{ref} presented to the non-inverting (+) terminal of the error amplifier from a terminal 25 so as to generate an error voltage signal A at the output of the error amplifier. Strictly speaking, the error amplifier comprises all of the elements within the box 45 shown in dashed lines. The signals A and B (see Fig. 5) are fed to the non-inverting (+) and inverting (-) terminals of a voltage comparator 26 to generate a PWM (Pulse Width Modulated) output signal C having the waveform shown in Fig. 5. An inverter 27 is employed to produce the complementary output waveform DD (see Fig. 5) of signal C.

The signal C is also applied to a voltage differentiator circuit 28 to generate a sequence of pulse signals E to trigger two monostable multivibrators 29 and 29A. Multivibrator 29 is a mono-stable one triggering on a positive flank. Multivibrator 29A is a mono-stable one triggering on a negative flank. The monostable multivibrators are used to generate the dead time intervals t_d in Fig. 5 for zero-voltage switching when the signals F and G respectively of their complementary outputs are combined with the signals C and DD, respectively, via respective AND gates 30 and 31 as shown in Fig. 4. The outputs H and I of the AND gates 30 and 31, respectively, are the desired control signals for the switching devices Q1 and Q2, as shown in Fig. 5. The control signal I for the switching device Q2 requires a voltage level shift circuit 34. Driving circuits 32 and 33 are employed to provide enough power to drive the switching devices Q1 and Q2, respectively.

In the case of a high line voltage or a light output load, the output voltage V_0 and the energy storage capacitor voltage V_{ce} will increase, resulting in a decrease of the signal A at the output of the error amplifier. From Fig. 5, it can be seen that the duty ratio

of control signal H will be reduced if signal A decreases. Therefore, the output voltage and the energy storage capacitor voltage are reduced to compensate the increasement, resulting in a constant output voltage. In the case of a low line voltage or a heavy output load, the voltage V_0 and the energy storage capacitor voltage V_{ce} will decrease. The output signal A of the error amplifier then will increase, resulting in an increase of the duty ratio of control signal H. Thus, V_0 and V_{ce} are kept constant.

The control circuit of Fig. 4 also includes a protection circuit and a soft-start circuit. The storage capacitor voltage V_{ce} at terminal 35 is applied to the non-inverting input (+) of a comparator 36 having its inverting input (-) connected to a terminal 37 which supplies a voltage limit reference voltage. The terminal 38 supplies a signal voltage proportional to the current I_{Q1} in the switching transistor Q1 (Fig. 2) to the non-inverting input (+) of a further comparator 39. The inverting input (-) of the comparator 39 is coupled to a terminal 40 which supplies a current limit reference voltage (for transistor Q1).

The outputs of comparators 36 and 39 are coupled to the reset input of a flip-flop 50 via an OR gate 42. The Q output of the flip-flop 50 is coupled to the AND gates 30 and 31, while the $\bar{Q}$ output is coupled to a soft-start circuit 41. A pair of series connected resistors R4 and R5 are connected between a supply voltage terminal V_{cc} and ground. A parallel circuit of a FET 43 and a capacitor C_s are coupled across resistor R5 and with the gate of the transistor coupled to the output of the OR gate. A diode 44 is connected between the output of error amplifier 24 and the node between resistors R4 and R5.

When the circuit is first turned on, the soft-start capacitor C_s is slowly charged up from zero through the resistors R4, R5 and the voltage source V_{cc} . The duty ratio of control signal H is also slowly increased from zero to its steady state value, resulting in a soft-start procedure.

When the energy storage capacitor voltage V_{ce} or low-side switching device current I_{Q1} exceeds its limit, the output of the OR gate 42 goes high to reset the flip-flop 50 to a low level. The AND gates 30 and 31 are then closed. No signal will be applied to the gates of FETs Q1, Q2. The power converter will be shut down. At the same time, the $\bar{Q}$ output of the flip-flop 50 goes to a high level, turning on the field effect transistor 43. The voltage across the soft-start capacitor C_s is discharged to zero through the transistor making the circuit ready for the next soft-start.

The constant duty ratio control circuit is relatively simple and provides a high power factor ($> .99$) and a low THD ($< 10\%$). However, these features are obtained





at the cost of a high storage capacitor voltage V_{ce} , which also results in high voltage stress in the power MOSFETs.

A second control scheme, that is, duty ratio sweeping control is introduced to overcome the above problems. As can be seen from (6), a sinusoidal line current i_{line} can be obtained if the duty ratio is swept as follows over half a line period:

$$D = D_{max} \sqrt{1 - \frac{1}{M_p} |\sin WT|} \quad (8)$$

A plot of duty ratio D over half a line period is shown in Fig. 6 together with the line voltage waveform RLV , being the rectified line voltage. The duty ratio reaches a minimum when the line voltage is at its peak:

$$D_{min} = D_{max} \sqrt{1 - \frac{1}{M_p}} \quad (9)$$

To reduce the current stress, the inductance of the power factor correction inductor L should be chosen so that its current reaches zero just prior to the turn on of FET Q1. In this case, the voltage conversion ratio can be obtained as in a CCM boost converter.

$$M_p = \frac{1}{1 - D_{min}} \quad (10)$$

Therefore, the following is obtained from (9) and (10):

$$D_{min} = 1 - \frac{1}{M_p} \quad (11)$$

$$D_{max} = \sqrt{1 - \frac{1}{M_p}} \quad (12)$$

Fig. 7 shows the maximum and minimum duty ratios as a function of M_p .

The circuit for duty ratio sweeping control according to (8) is similar to that of the constant duty ratio control circuit except that an extra function for the duty ratio sweep is added. This sweep function is accomplished by means of a square-root calculation stage 46 and a duty ratio sweeping range control circuit 47 as shown in Fig. 8.

In Fig. 8, the rectified line voltage $|V_{in}|$ is applied to the square-root calculation stage 46 from a terminal 48 and to a low pass filter consisting of a resistor R_f and



a capacitor C_f which provide a voltage proportional to the amplitude of the rectified line voltage V_m . A voltage V_{R7} which is proportional to the storage capacitor voltage V_{ce} is also obtained through a resistor divider consisting of resistors R6 and R7 coupled to a terminal 49 which provides the voltage V_{ce} . The voltage V_{R7} across resistor R7 is then divided by the voltage V_m in the divider circuit 50 in order to obtain a signal K proportional to M_p . Hence, a signal L at the output of the square-root calculation stage exhibits a square root waveform as expressed by the right side of equation (8). The signal L is coupled via resistor R1 to the inverting terminal of the error amplifier 24 in the control circuit diagram of Fig. 4 so as to control the duty ratio of the control signal H. By introducing duty ratio sweeping control over each line period T_1 , a high input power factor and low THD can be obtained while keeping the voltage V_{ce} low to reduce the switch stress. However, the use of duty ratio sweeping control results in an increase of the low frequency ripple in the output voltage. In lighting applications, such low frequency voltage ripple is represented by a parameter called crest factor, which is defined as the peak voltage divided by the rms value of the output voltage. As long as the value of the crest factor is less than 1.7, the presence of low frequency ripple in the output voltage is acceptable.

As discussed above, the converter circuit of Fig. 2, with or without the clamp diode D11, contains an undesired oscillation in the diode voltage (V_{Din}) of blocking diode 12.

A more effective method of removing the unwanted oscillation is to clamp the diode voltage V_{Din} as shown in Fig. 9. In this embodiment, the inductor 11 (L_{in}) is connected between the negative terminal 9 of the full bridge rectifier 7 and a ground line. The voltage clamping diode D11 now is connected between the terminal 9 and the source terminal of the switching device Q2. In the circuit shown in Fig. 9, the diode 12 voltage will increase from zero and the inductor voltage will increase to zero from a negative value after the diode D_{in} is turned off. When the inductor voltage V_{Lin} reaches zero and becomes positive, the clamp diode D11 conducts because the MOSFET Q2 is on and the positive voltage of V_{Lin} biases the diode D11 positively. Therefore, the inductor voltage is clamped at zero, which is its steady state value when $i_{Lin} = 0$. Consequently, the diode voltage V_{Din} equals to $V_{ce} - |V_{in}|$, its steady state value when it is in the off state. Thus, there is no oscillation produced in the converter circuit of Fig. 9. Aside from the foregoing description, the converter circuit of Fig. 9 operates in a similar manner to that of Fig. 2.

Another embodiment of the invention is shown in Fig. 10. This circuit is similar to that of Figs. 2 and 9 except for the manner in which the resonant circuit consisting

of L_r , C_b , C_r , T and RL is connected to the switching MOSFET Q1. In Fig. 10, the inductor 11 is again connected in the return line, as in Fig. 9. The energy stored capacitor C_e is no longer in series circuit with the capacitor C_b and the inductor 13 (L_r), but is still connected between the cathode of diode 12 (D_{in}) and the transistor Q2. The clamp diode D11 is
5 connected as in Fig. 9.

Fig. 11 shows another embodiment of the invention comprising a half-bridge connection of the resonant circuit of the overall converter circuit. The energy storage capacitor C_e is now made up of two separate storage capacitors C_{e1} and C_{e2} . These two storage capacitors are connected in series between the cathode of diode 12 (D_{in}) and the FET
10 Q2. The two energy storage capacitors C_{e1} and C_{e2} act as a voltage divider, too.

In Fig. 2, Fig. 9, Fig. 10 and Fig. 11, the N-channel FET Q2 can be replaced by a P-channel FET with its source grounded. In this case, the voltage level shift circuit 34 in the control circuit of Fig. 4 can be eliminated. The operation remains the same.

If isolation is not required, the isolation transformer can be removed.

15 In view of the fact that the power factor correction boost converter and the high frequency DC/AC inverter share a switching transistor and the control circuit, the invention requires fewer components so that both the cost and size of the overall circuit are reduced while the power factor is high and the current distortion is low. The zero-voltage switching of both of the MOSFETs reduces switching losses and EMI noise. Since the PWM
20 technique can be used to regulate the line variation and power factor correction is inherent in this circuit, the control circuit can be very simple. The duty ratio sweep control varies the duty cycle so as to make the input current waveform more sinusoidal, another attractive feature of the invention. The reactive power is kept low by choosing a duty ratio of approximately 0.45, resulting in a small size and reduced conduction loss. The system also
25 substantially reduces or completely eliminates the oscillation in the diode voltage (V_{Din}) for all practical purposes.

It is to be understood that the above described embodiments are merely illustrative of the principles of the invention and that other arrangements may be devised by those skilled in the art without departing from the spirit and scope of the invention.

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CLAIMS:

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1. A high frequency converter apparatus comprising:
first and second input terminals for connection to a source of supply
voltage for the converter,
output means including a resonant circuit for connection to a load to be
5 driven by the converter,
a first series circuit including an inductor means, a rectifier element, and
a first semiconductor controlled switching device coupled to said input terminals,
characterized in that the converter further comprises
a storage capacitor means and an isolation capacitor means coupled to said
10 rectifier element and to said output means, respectively,
a second semiconductor controlled switching device coupled to said
storage capacitor means,
first and second diode means coupled across said first and second
semiconductor controlled switching devices, respectively, and
15 a control circuit responsive at least to a voltage developed across the
storage capacitor means and having output means coupled to control electrodes of the first
and second semiconductor controlled switching devices so as to alternately trigger the first
and second semiconductor controlled switching devices on and off in mutually exclusive time
intervals, said first semiconductor switching device forming a power factor correction
20 converter part of the apparatus and also forming a high frequency DC/AC inverter part of
the apparatus.
2. A converter apparatus as claimed in claim 1 further comprising a voltage
clamp means coupled to at least one of said rectifier element and said inductor means in a
manner so as to clamp the voltage of the rectifier element to a steady state value.
- 25 3. A converter apparatus as claimed in claim 2 wherein said voltage clamp
means comprises a diode coupled to a node between the inductor means and rectifier element
and to one of said input terminals.
4. A converter apparatus as claimed in claim 1, 2 or 3 wherein said storage
capacitor means, said isolation capacitor means and said output means are connected in a



second series circuit across the first semiconductor switching device and with the second semiconductor switching device coupled to a junction point between said storage capacitor means and said isolation capacitor means.

5. A converter apparatus as claimed in claim 1 or 2, wherein said storage capacitor means is sub-divided into first and second capacitor means and with the first capacitor means, said isolation capacitor means and said output means connected in a second series circuit across the first semiconductor switching device and with the second capacitor means coupled between the second semiconductor switching device and a junction point between the first capacitor means and the isolation capacitor means.
- 10 6. A converter apparatus as claimed in claim 1 or 2 wherein said rectifier element is connected to the first input terminal and the inductor means is connected to the second input terminal,
- said isolation capacitor means and said output means are connected in a second series circuit between the rectifier element and the inductor means, and
- 15 said storage capacitor means is connected between the second semiconductor switching device and a junction point between the rectifier element and the isolation capacitor.
7. A converter apparatus as claimed in claim 2, 5 or 6 wherein said rectifier element is connected to the first input terminal and the inductor is connected to the second input terminal, and further comprising:
- 20 a voltage clamp comprising a diode coupled to one main electrode of the second semiconductor switching device and to said second input terminal thereby to clamp the voltage of the rectifier element.
8. A converter apparatus as claimed in any of the preceding claims wherein
- 25 said output means comprises:
- a second inductor means and a first winding of an isolation transformer connected in series to the isolation capacitor means, and
- a further capacitor coupled to a second winding of the isolation transformer, said second inductor and said further capacitor forming a part of said resonant
- 30 circuit.
9. A converter apparatus as claimed in one of more of the preceding claims wherein said control circuit further comprises an oscillator and means controlled by the oscillator and at least said storage capacitor means, voltage for generating first and second switching voltages for application to the respective control electrodes of the first and second





semiconductor controlled switching devices via the output means of the control circuit to produce zero-voltage switching of said semiconductor switching devices at a constant duty ratio.

10. A converter apparatus as claimed in any of the claims wherein said

5 control circuit further comprises;

a duty ratio sweeping range control circuit responsive to a voltage determined by the supply voltage and said storage capacitor means voltage,

a square root circuit controlled by the voltage determined by the supply voltage and an output voltage of said duty ratio sweeping range control circuit,

10 an oscillator, and

means responsive to an output signal of the oscillator and an output signal of the square root circuit for generating first and second switching voltages for application to the respective control electrodes of the first and second semiconductor controlled switching devices via the output means of the control circuit so as to switch the first and second
15 semiconductor switching devices with a variable duty cycle.

This Sheet Has Been Replaced

